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SNM Analysis of 6T SRAM at 32NM and 45NM Technique

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OBJECTIVE OF THE CHAPTER

In this paper we analyze the effect of SNM dependent on different parameter in read mode and write mode. We analyze SNM of different modulation like cell ratio (CR), voltage supply (Vdd), word line (WL) and bit line (BL) by spice tools using BPTM Low Power model in different technologies. We define the read margin to characterize the SRAM cells read stability. Many researchers use only 45nm technology, but we are scaling down the technologies which is more stability for the circuit. Actually stability of SRAM cell only depends on the static noise margin (SNM) and SNM is effect the stability of SRAM cell during read operation of SRAM cells.

1. BACKGROUND AND RELATED WORK

SRAMs, are widely used in electronic systems [1]. SRAM cell read stability are major concerns in CMOS technologies. Actually stability of SRAM cell only depends on the static noise margin (SNM). Till now we have been using only 45nm technology, which is Welsh for stability and performance of cell. We continue to scale down the device dimension because device should be small [2] [8]. Now a days circuit designer has focused on lower supply voltage, but lower supply voltage can reduce the static noise margin and static noise margin is proportional to the performance of SRAM cell so performance of SRAM cell is also reduced. In this project we scaled down the technology and variation of different parameter such as cell ratio (CR), voltage supply (Vdd), word line (WL) and bit line (BL). It has been most beneficial of performance of cell and size will reduced as much as possible.

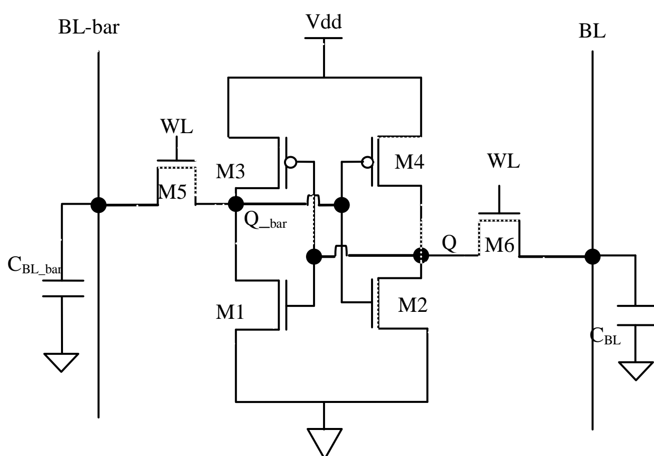

Figure 1. 6T SRAM cell

2. METHODOLOGY AND IMPLEMENTATION

2.1 Static Noise Margin and Derivation

Static noise margin of SRAM cell depends on the cell ratio (CR) [9] supply voltage [10] and pull up ratio [11]. High value of SNM is required for the high stability of SRAM cell. Both read margin and write margin are also affected by the static noise margin of SRAM cell.

In this section, Butterfly method for measuring static noise margin is introduced. It is the maximum amount of noise voltage that can be tolerated in 6T SRAM cell while still maintaining the correct In this section, Butterfly method for measuring static noise margin is introduced. It is the maximum amount of noise voltage that can be tolerated in 6T SRAM cell while still maintaining the correct. The two output curves are rotated according to X-Y coordinates which results in butterfly structure [3]

The CMOS model which is use to calculate SNM

$$I_D = \frac{1}{2}\beta(V_{GS}-V_T)^2$$

$$I_D = \beta V_{DS}(V_{GS}-V_T-\frac{1}{2}V_{DS})$$

In the saturated and linear regions, respectively

$$SNM_{6T} = V_T - \left(\frac{1}{K+1}\right)\left\{\frac{VDD-(2r+1)/(r+1)VT}{1+\frac{r}{k(r+1)}} \cdot \frac{VDD-2VT}{1+k\frac{r}{q}+\sqrt{\frac{r}{q}}(1+2k+\frac{r}{q}k^2)}\right\}$$

Where

$$r = \text{ratio} = \frac{\beta d}{\beta a}$$

$$q = \frac{\beta p}{\beta a}$$

V_T= threshold voltage

$$k = \left(\frac{r}{r+1}\right)\left(\left\{\sqrt{\frac{r+1}{r+1-(Vs)2/(Vr)2}} - 1\right\}\right.$$

$$Vs = V_{DD} - V_T$$

$$V_r = V_s - \left(\frac{r}{r+1}\right)V_T$$

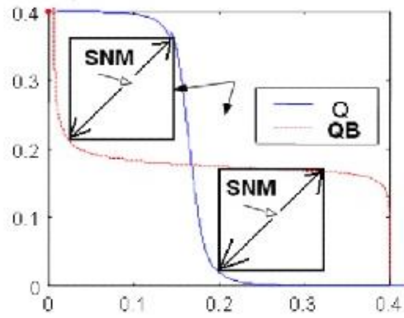

Figure 2. Calculation of snm after rotation

2.2 Cell Ratio (Cr)

In this section static noise margin is calculated by varying the cell ratio of transistors. Cell ratio is the ratio of sizes of driver transistor to the access transistor. As the cell ratio increases by increasing the size of driver transistor, Static noise margin of memory cell also increases which results in increase of current in a memory cell [4].

Cell Ratio (CR)= (W1/L1) / (W6/L6)

2.3 Pull Up Ratio (Pr)

In this section, static noise margin is calculated by varying the Pull up ratio of transistors. Pull up ratio is the ratio of sizes of load transistor to the access transistor. As the Pull up ratio increases by increasing the size of driver transistor, Static noise margin of memory cell also increases which results in increase of current in a memory cell [4].

Pull up Ratio (PR) = (W4/L4) / (W5/L5)

3. RESULTS & DISSCUSSION SNM DEPENDENCES

This section explores the different parameters on which the SNM is dependent. The factor are supply voltage (Vdd), cell ratio (CR), word line (WL), and bit line(BL) read and write condition.

3.1 SNM DEPENDENCES ON Vdd

The 32nm and 45nm dependent of supply voltage (Vdd). We use PTM Low Power model to determine SNM of these technology on spice tools from [5]. Vdd modulation table and graph shown in below

Vdd	45nm	32nm
0.1	2.3820 E-02	2.8434 E-02
0.2	2.9003 E-02	3.5215 E-02
0.3	4.6991 E-02	5.1374 E-02
0.4	1.2413 E-01	1.2185 E-01
0.5	1.7661 E-01	1.7891 E-01
0.6	1.3070 E-01	1.3526 E-01
0.7	8.9641 E-02	9.3843 E-02
0.8	1.1309E-01	1.0257 E-01
0.9	1.8632 E-01	1.7402 E-01
1	2.5815 E-01	2.4592 E-01

Vdd modulation during read mode-,CR=3,BL=1,BLB=1

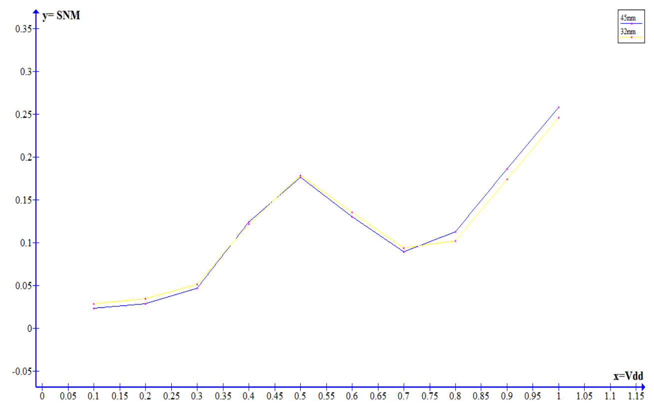

Figure 3. Output waveform of Snm at different voltage at read mode

Vdd	45nm	32nm
0.1	1.8316 E-02	2.3102 E-02
0.2	2.2123 E-02	1.6880 E-02
0.3	5.3659 E-02	4.6873 E-02
0.4	7.9085 E-02	7.2914 E-02
0.5	9.1660 E-02	8.6651 E-02
0.6	1.2861 E-01	1.1673 E-01
0.7	1.5672 E-01	1.4580 E-01
0.8	1.8518E-01	1.7322 E-01
0.9	2.1941 E-01	2.0602 E-01
1	2.5815 E-01	2.4592 E-01

Vdd modulation during write mode-,CR=3,BL=BLB=WL=Vdd

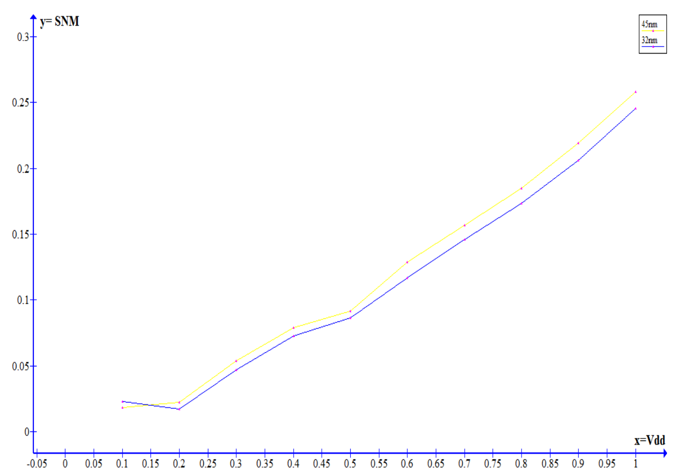

Figure 4. Output waveform of Snm at different voltage at write mode

3.2 SNM Dependences on Cell Ratio (CR)

The cell ratio has very little impact on SNM during Sub threshold read. The CR modulation on 32nm and 45nm to finding SNM on read and write condition. These effects depend on the technology and make the general SNM modeling more complicated see [5,6].

CR	45nm	32nm
1	2.0686E-01	2.9392 E-01
1.5	2.3018 E-01	2.1407 E-01
2	2.3975 E-01	2.2808 E-01
2.5	2.5001 E-01	2.3921 E-01
3	2.5815 E-01	2.4592 E-01
4	2.7001 E-01	2.5704 E-01

CR efect on SNM during read Mode- BL =1,V_{DD}=1 ,WL1 ,CR=

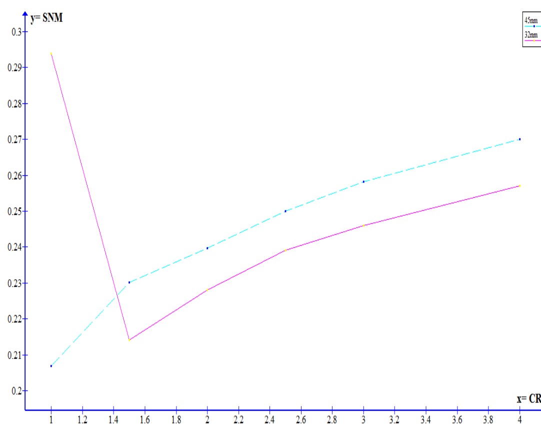

Figure 5. Output waveform CR efect on SNM during read Mode

CR	45nm	32nm
1	5.0378E-01	5.3432 E-01
1.5	4.7268 E-01	4.9962E-01
2	4.5457 E-01	4.7974 E-01
2.5	4.4267 E-01	4.6674 E-01
3	4.3424 E-01	4.5755 E-01
4	4.2308 E-01	4.4540 E-01

Effect of CR on SNM During write Mode- BL=0,VDD=1 ,WL=0 BLB=1 ,CR=3

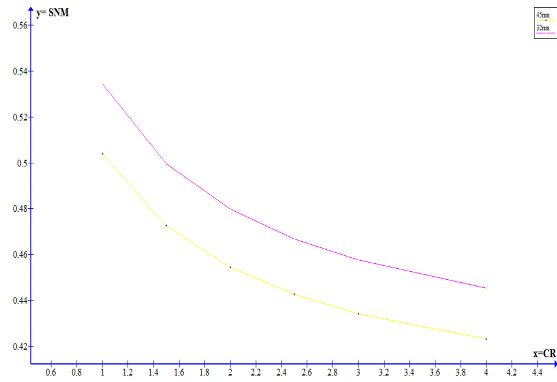

Figure 6. Output waveform CR efect on SNM during write Mode

3.3 SNM Dependences on Word Line (WL)

We modulate word line to finding snm of these technology.

WL(V)	45nm	32nm
0.1	4.0818 E-01	3.9697 E-01
0.2	4.0817 E-01	3.9696 E-01
0.3	4.0808 E-01	3.9683 E-01
0.4	4.0707 E-01	3.9546 E-01
0.5	4.0042 E-01	3.8678 E-01
0.6	3.8041 E-01	3.6376 E-01
0.7	3.4998 E-01	3.3282 E-01
0.8	3.1729E-01	3.0194 E-01
0.9	2.8679 E-01	2.7280 E-01
1	2.5815 E-01	2.4592 E-01

World line modulation during read mode- V_{DD}=1,CR=3,BL=1,BLB=1

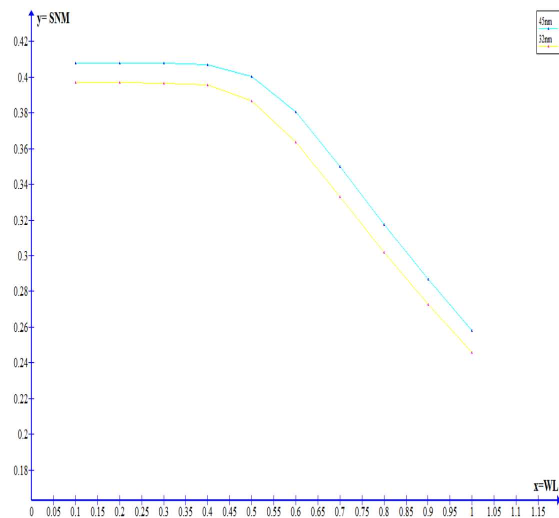

Figure 7. Output waveform World line modulation during read mode

WL(V)	45nm	32nm
0.1	4.0817 E-01	3.9696 E-01
0.2	4.0809 E-01	3.9693 E-01
0.3	4.0776 E-01	3.9647 E-01
0.4	4.0354 E-01	3.9188 E-01
0.5	4.0057 E-01	3.9197 E-01
0.6	4.0166 E-01	3.9244 E-01
0.7	4.1781 E-01	4.0095 E-01
0.8	4.2278E-01	4.0896 E-01
0.9	4.2465 E-01	4.1186 E-01
1	4.2557 E-01	4.5755 E-01

World line modulation during write mode- V_{DD}=1,CR=3,BL=1,BLB=0

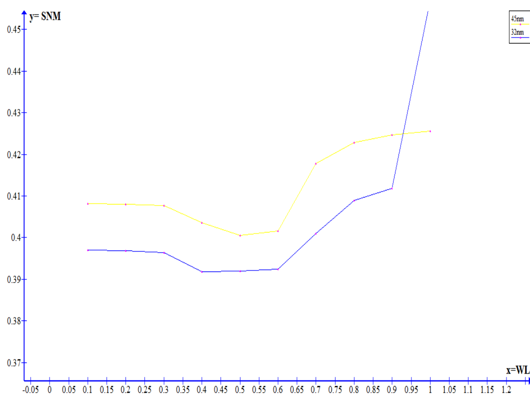

Figure 8. output waveform World line modulation during write mode

3.4 SNM DEPENDENCES ON BIT LINE

All of the above technique finding snm by modulation of bitline (BL) in read and write mode.table and graph shown in below:

BL(V)	45nm	32nm
0.1	3.3689 E-01	3.2832 E-01
0.2	2.9729 E-01	2.8981 E-01
0.3	2.7863 E-01	2.7123 E-01
0.4	2.7264 E-01	2.6433 E-01
0.5	2.6964 E-01	2.6059 E-01
0.6	2.6717 E-01	2.5744 E-01
0.7	2.6484 E-01	2.5446E-01
0.8	2.6258 E-01	2.5157 E-01
0.9	2.6036 E-01	2.4873 E-01
1	2.5825 E-01	2.4592E-01

Bit Line Modulation During Read Mode- VDD=1,CR=3,WL=1

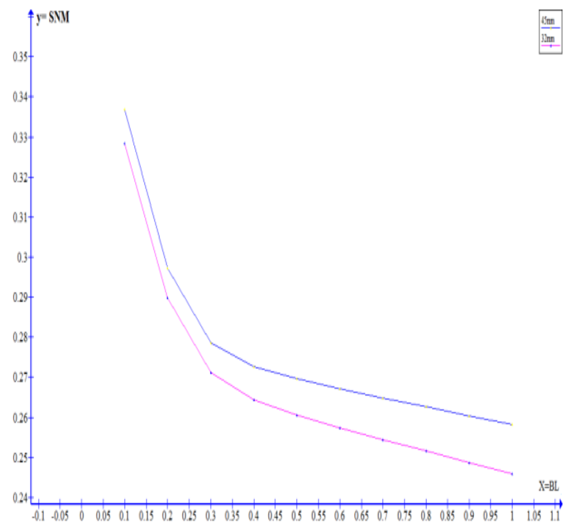

Figure 9. output waveform bit line modulation during read mode

BL(V)	45nm	32nm
0.1	4.0450 E-01	4.3609 E-01
0.2	4.1761 E-01	4.4927 E-01
0.3	4.2407 E-01	4.5651 E-01
0.4	4.2656 E-01	4.5972 E-01
0.5	4.2810 E-01	4.6175 E-01
0.6	4.2941 E-01	4.6350 E-01
0.7	4.3064 E-01	4.6515E-01
0.8	4.3185 E-01	4.6677 E-01
0.9	4.3305 E-01	4.6837 E-01
1	4.3424 E-01	.6997E-01

Bit Line Modulation During write Mode- V_{DD}=1,CR=3,WL=1 BLB=0

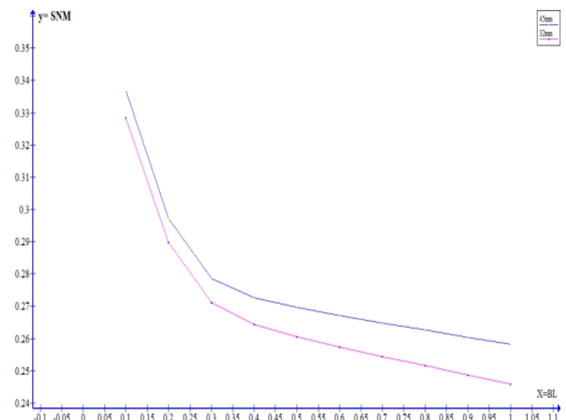

Figure10. output waveform bit line modulation during write mode

4. INTERPRETATIONS

Read and Write Ability of 6T SRM Cell

There are three types of mode of SRAM cell are read mode, write mode and hold mode. In the hold mode word line (WL) should be '0'. In order to hold its data properly, the cross-coupled two inverters in the cell must sustain bi-stable operating points. From [14] the SNM is a common measure of the ability for the cell inverters to maintain their state. The SNM equals the minimum noise voltage present at each of the data storage nodes necessary to flip state of the cell. The Conventional 6T SRAM cell is more sensitive to noise during read mode. When the cell is in the read mode, the WL is connected to Vdd while the BL and BLB are precharged to Vdd. The data '0' store node rise to a certain voltage higher than the ground, according to the voltage dividing across the driver transistor and access transistor.

5. CONCLUSION

In this paper, we have analyzed SNM during read state and write state modulation of cell ratio, voltage supply ,word line and bit-line in 22nm ,32nm and 45nm. As the different technique is now a days a prime concern in the realization of the performance of a CMOS circuit. In this paper SNM of SRAM dependences various parameter in read and write mode.

6. REFRENCE

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