Power and Area Efficient FLASH ADC Design using 65nm CMOS Technology

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ABSTRACT
This paper presents a design of a high speed Comparator design using 65nm digital CMOS technology on Cadence Virtuoso Design Tool. The proposed FLASH ADC Design consists of fully differential topology. The first stage provides a Voltage Divider circuit and the second stage is Comparator Design having high sampling frequency tolerance, and the high efficient common drain circuit provides high driving capability with relatively low power dissipation. It is used in more application for bandwidth and power and a high resolution is available for analog-to-digital converters (ADCs). Under 1 V supply voltage, the simulation results show that the proposed FLASH ADC Design is having a differential topology along with latching circuit.

Keywords
Analog to Digital convertor(ADC), common mode feedback (CMFB) circuits, Complementary metal oxide semiconductor (CMOS),Voltage full scale range(VFSR), Differential non linearity (DNL), Least significant bit (LSB),Most significant bit (MSB),TSPCR(True Single-Phase Clock register).

1. INTRODUCTION
As the CMOS technology is continuously scaling down, the design of ultra-high speed wired or wireless communication system is becoming possible. However, the advanced digital CMOS technology a challenging aspect for analog designers when designing mixed-signal systems. Operational amplifier, which is one of the key in analog modules, could achieve wider bandwidth due to the scaled transistor model, but when we consider a frequently decreased gain proportionally limited signal swing, poor synchronizing etc. For effectively increase operational amplifier's gain and output voltage swing, multi-stage fully differential operational amplifier design is required. The operational amplifier with three or even more stages are cascaded with the Nested- Miller compensation or the Reversed Nested-Miller compensation that shows higher efficiency in the voltage gain enhancement, while they require additional large compensation capacitors compared to the basic two-stage operational amplifier, that will leads to a maximum die area and the limited slew rate [6][7].Besides, in addition to common mode feedback (CMFB) circuits, it would consume additional power. The traditional Comparator design using latching technique could provide adequate gain in Nano meter CMOS technology. Furthermore, for the high performance flash analog-to digital converter (ADC) in the Nanometer digital CMOS technology with low supply voltage, the requirements of high performance voltage divider bias circuit, the power efficient and high frequency samples tolerable comparator design and priority encoder deign along with latches. Targeting at the application in high performance ADCs, a Voltage divider circuit using CMOS Technology and a Comparator Design using latching Technique is presented in this paper [4]. The proposed design enables this ADC to achieve a good resolution, high speed and high slew rate and keep the power dissipation low

2. PRINCIPLE OPERATION OF FLASH ADC
The 3-bit Flash ADC architecture as shown in Fig.1. The standard Flash ADC consists of three parts: The resistive network, the comparators, and the priority encoder along with latches [1]. Each comparator compares the voltage difference between its positive input from sampled sine wave VIN and its reference voltage as negative input from the Resistive ladder and then generates a digital output called thermometer code which is the output of comparator.

The binary encoder generates corresponding 3-bit binary codes based on the comparator outputs. As shown in Fig.1. The encoder converts the thermometer code produced by the comparators to a binary code. As seen from the figure, the comparators all operate in parallel. Thus, the clock signal applied at a time for synchronization. Due to this, the conversion speed is limited .The speed of operation of FLASH ADC depends mainly on the speed of the comparator or the sampler. Due to this, the Flash ADC is capable of high conversion speed and doing operation for single clock pulse.

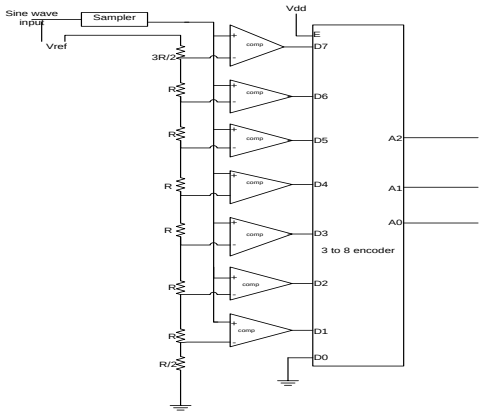


Fig 1: Flash ADC Architecture

3. CONVENTIONAL WORK

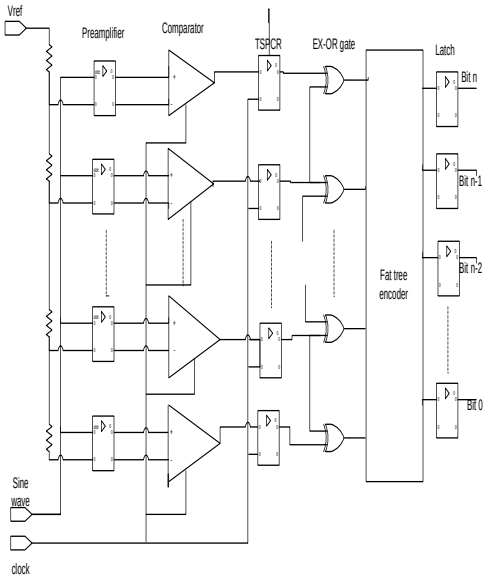


Fig 2: ADC Design

3.1 Resistive Averaging Technique:

Resistive averaging technique is often used in flash ADC, which can reduce the random offset of the preamplifiers and to reduce the nonlinearity of the ADC [8]. In order to improve the analysis on the effect to linearity (INL and DNL, it is useful to replace the pre-amplifier with a controlled voltage source with limited output impedance [9]. The voltage source is composed of three parts: the reference voltage input sampled sine wave and along with offset voltage applied at the input of the pre-amplifier. Therefore, by ignoring the nonlinearity of the amplifier, the superposition principle can be used to analyze the simplified linear circuit when the impact of reference voltage and input voltage are not taken into consideration.

3.2 Comparator Design

The schematic diagram of pre-latch comparator design having input stage of fully differential topology. In this design, two latches consisted of positive feedback to improve gain. The speed of the amplifier depends on recovery speed on latch circuit on M5-M8.All pMOS transistors and nMOS transistors having a proper width to achieve high driving capability. The total delay can be minimized with high gain and appropriate bandwidth. Applying a clock pulse ,as input voltage is more than the reference voltage ,output plus pin gives maximum pulse width depends on slew rate of the circuit).The output minus pin is complement to output plus pin signal. The TSPCR is used to generate clock to synchronize the comparator and encoder design.

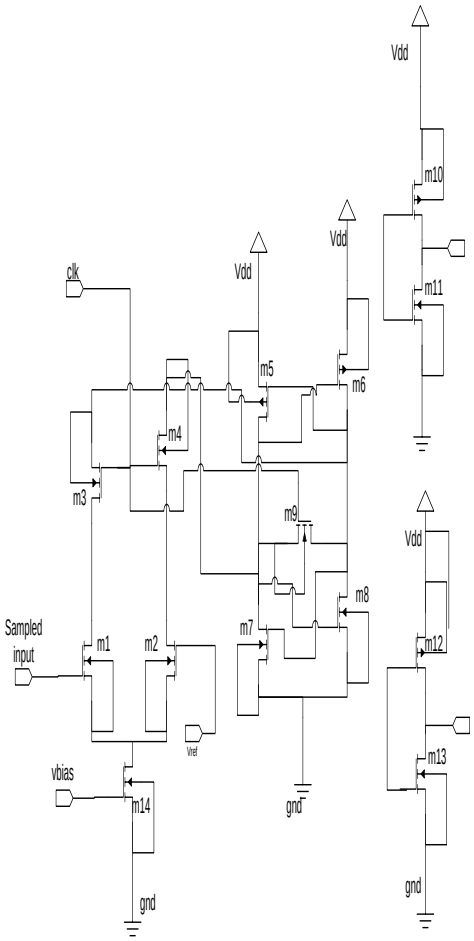


Fig 3: Comparator Design

3.3 Fat Tree Coding

The encoder changes the thermometer code generated by comparators into binary code which is easy to understand, and there are mainly three suitable encoders to convert thermometer code into binary code for flash ADC. They are ROM/PLA, Fat Tree, and Wallace Tree. This design uses the Fat Tree encoder which is the fastest. First, change the thermometer code into one-hot code through Ex-OR gates, and then, change the one-hot code into binary code through Fat Tree encoder.

3.4 Simulation Results

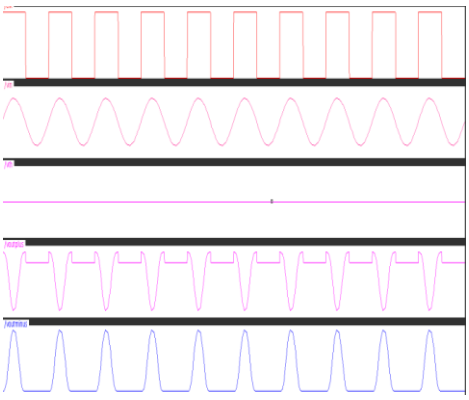


Fig 4: Comparator design simulation results using 60nm technology using cadence tool.

4. PROPOSED WORK

4.1 Sample and Hold Circuit

The sample and hold circuit of Fig:5 having a clock pulse. During the conducting phase of the switch, the signal on the capacitor charge up to the input signal, while in the quarantine (phase), the signal value remains fixed at its value at that moment of opening the switch. This moment is the theoretical sampling point in time. The T&H circuit can keep the signal at that level for a time period thus make allowable repeated use of the signal during the analog-to digital conversion. The track-and-hold switch is characterized by its on/off impedances. In a T&H circuit the on-resistance must be small and constant and the off impedance must be infinite. In the on-state the conductivity of a single MOS transistor as a switch depends on the MOSFET saturation voltage level. The dummy switches NM2 and NM4 as shown in Fig: 5 are single devices while the pass transistor NM3 consists of two parallel transistors for optimum cancellation. The control of the sample pulse edges requires careful balancing. If the "CLK" pulse switches off while the inverse clock pulse is not yet active, there will be a lot of switching glitches. If the inverse clock pulses become active while the "CLK" pulse is still active, the compensation charge will be supplied by the source and the whole method is ineffective. The occurrence of these two situations depends on the level of the input signal. The block box represents an inverter. The two pass transistors NM2 and NM4 having a width W/2 and the pass transistor NM3 in the middle having a width of W. The simulation results shown in Fig: 6.

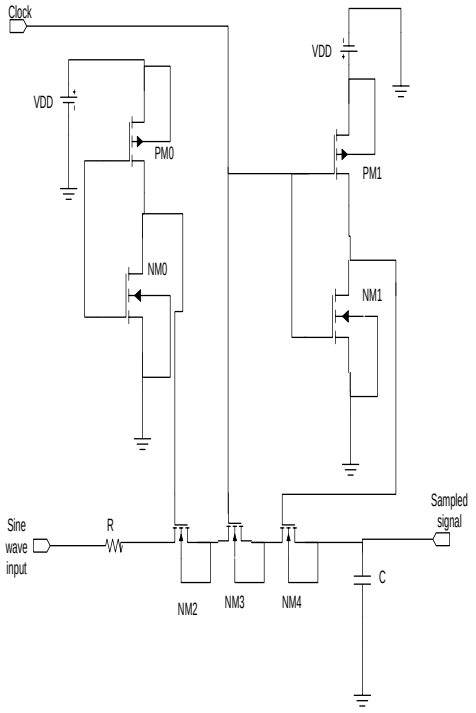


Fig 5: Sample ad Hold circuit immanent charge splitting can be compensated by dummy switches.

4.2 Voltage Divider Circuit

To obtain DC-bias voltages V_{out0}, V_{out1}, ---------- V_{outn}, where $V_{ss} < V_{out0} < V_{out1} <$ --------V_{DD}, voltage divider can be used. Basically, resistive ladders are scarcely used in MOS Technology, mainly because of the large-die area required with suitable-values. Here, instead MOSFET"s used in Totem pole configuration".

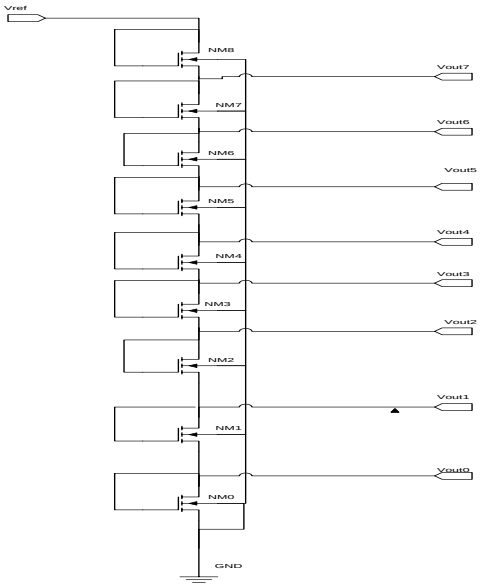


Fig 6: Voltage divider circuit

The condition for saturation of nMOS device

$$V_{ds} > V_{gs} - V_t \text{----------1}$$

is satisfied.

$$I_{dc} = K^1 (W/L)_{NM0} (V_{out0} - V_{t,NM0})^2$$

$$= K^1 (W/L)_{NM1} (V_{out1} - V_{t,NM1})^2$$

$$= K^1 (W/L)_{NM2} (V_{out2} - V_{out1} - V_{t,NM2})^2$$

$$= K^1 (W/L)_{NM2} (V_{out2} - V_{out1} - V_{t,NM2})^2 \text{ and so on}$$

$$= K^1 (W/L)_{NM,n+1} (V_{DD} - V_{out,n} - V_{t,NM,n+1})^2$$

Where K^1 represents $\mu_n C_{ox}$

$$|V_T| = |V_{T0}| + \gamma \{ 2 |\phi_p| + | V_{SB}|)^{1/2} - (2 |\phi_p|)^{1/2}\} \quad (2)$$

Where γ (body effect coefficient)= $\{(2.q.N_A \varepsilon_{si})^{1/2} / C_{ox}\}$

q=electron charge(C).

ϕ_p=Fermi potential. (Positive for nMOS and negative for pMOS.)

V_{SB}=substrate bias voltage (V).

V_{T0}=threshold voltage at zero body effect coefficient (V).

N_A=charge concentration (carriers/cm^3).

μ_n= mobility of electrons (cm^2/V-sec).

C_{ox}= gate-oxide capacitance per unit area (F/m^2).

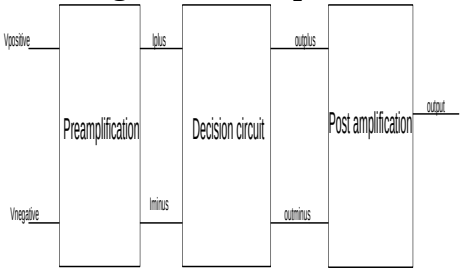
In the above circuit, body bias effect is zero. If we consider the body bias effect the effect of threshold voltage is given as follows (assume Vss is ground terminal).

The Threshold voltages $V_{T,NM0}$, $V_{T.NM1}$---------- are different for different devices:

$$V_{T,NM0} = V_T.$$

$|V_{T,NM1}| = |V_T| + \gamma \{ 2 |\phi_p| + | V_{out0}|)^{1/2} - (2 |\phi_p|)^{1/2}\}$ (3) $|V_{T,NM2}| = |V_T| + \gamma \{ 2 |\phi_p| + | V_{out1}|)^{1/2} - (2 |\phi_p|)^{1/2}\}$ (4) $|V_{T,NM,n+1}| = |V_T| + \gamma \{ 2 |\phi_p| + | V_{out,n}|)1/2 - (2 |\phi_p|)^{1/2}\}$ (5)

4.3 Block Diagram of Comparator Design



4.3.1 Specifications consider while designing Comparator:

4.3.1.1 Offset Voltage

For an ideal op-amp, if non-inverting terminal and inverting terminal are equal, then output voltage is zero. In reality, this is not exactly true, and a voltage $V_{0,off}$ is not equal to zero will occur at output for shorted inputs. Since, $V_{0,\ off}$ is usually directly proportional to the gain of a circuit; the effect that can be more conveniently described in terms of the input offset voltage $V_{in,off}$, defined as the differential input voltage needs to restore output voltage to zero in the practical devices[10,11].A resistive network as to be made to reduce offset voltage say offset compensation network.

4.3.1.2 Differential Nonlinearity

DNL error is defined as the difference between an real value step width and the ideal value of first LSB. For an ideal ADC, in which the differential nonlinearity coincides with DNL = zeroed LSB, for each analog step equals to 1LSB and the step values are spaced exactly 1LSB apart [12], here mostly N represents number of bits to indicate resolution of ADC. When its digital output increases (or remains constant) with an increasing input signal, by neglecting sign changes in the slope of the transfer curve.

$$LSB=(V_{ref})/2^N$$

The voltage full scale range is calculated using the formula:

$$Full\ sale=V_{ref}\text{-}1LSB$$

4.3.1.3 Resolution:

Resolution is the smallest analog increment corresponding to a 1 LSB converter code change. For converters, resolution is normally expressed in bits, where the number of digital bits or codes which is equal to 2^n. As an example, an 8-bit ADC decodes the analog signal into 2^8 = 256 digital outputs .

4.3.1.4 Slew Rate:

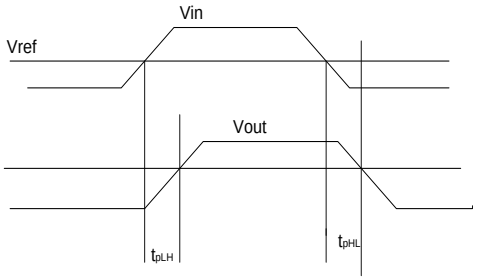
Slew rate is defined as the change in output voltage with respect to time. i.e.,

$$Slew\ rate=(d/dt)V_o$$

For a sine wave output, the maximum slew rate occurs is equivalent to $2*\Pi*f*V_{o,max}$.

4.3.1.5 Propagation delay:

The amount of time it takes the input signal with respect to reference voltage and simultaneously, the output changes from its state i.e., either logic '0' or logic '1'.



- t_{pLH} is the delay time when the input switches and crosses reference voltage Vr_{ef}, that can make a change the output from low to high.
- t_{pHL} is the delay time when the crosses reference voltage, that can make a change the output from high to low.
- The average of t_{pLH} and t_{pHL} gives the propagation delay of comparator design. There are different aspects to reduce the propagation delay. The propagation delay normally varies with respect to amplitude of the input signal. Maximum amplitude of input signal will results a smaller delay time. Generally, the propagation delay can be reduced by cascading several stages of low gain amplifiers.

4.3.2 Pre amplification:

In order to improve the speed of the comparator and reduce the offset error caused by comparator, preamplifiers could be used. The Pre- amplification circuit is a CMOS differential amplifier consists of active loads. The transconductance sets the gain of an amplifier. The difference between the two inputs of the latch comparator would get bigger after the input signal amplified through the pre-amplifier. So, the latch comparator can compare faster. The design has used the low-gain, high bandwidth amplifier shown in Fig: 7 are cascaded, and the total delay can be minimized with high gain and appropriate bandwidth. The current mirror circuits are used as loading circuits i.e., PM0, PM2 and PM1, PM3.

$$Where\ g_{m,NM0}=g_{m,NM1}=g_m.$$

$$I_{0+}+I_{0-}=I_{ss}.$$

4.3.3 Decision Circuit:

The basic comparator design is::Here, for an n-bit use 2^n-1 differential amplifiers are used as comparators in Flash-ADC architecture. Firstly, try to implement a complex type of differential amplifier. But this element was not easy enough to understand for beginners. We consequently decided to prefer a basic design to realize our ADC. This decision made us loose several advantages as an improved gain, or power savings that would have benefit to our ADC precision and efficiency. When the input signal voltage is less than the reference voltage, the comparator output is at logic '0'.when the input signal voltage is higher than the reference voltage, the comparator output is at logic '1'. The comparators give the 2^n-1 levels of outputs in terms of reference voltage. The basic circuit diagram as shown in Fig 7.The input stage serves to amplify the differential signal and allows some common mode rejection .The load impedances is increase by putting current mirrors of pMOS devices PM0,PM1,PM2,PM3.The second stage is fed with the amplified signal to generate a digital decision. The intermediate amplification nodes separate the pre-amplifier

from the latch NM4 and NM5. The circuit makes a positive feedback by cross coupled NM4 and NM5 nMOS transistors say *latching*. To improve high driving capability based on mobility of charge carriers of holes and electrons, the width and length of pMOS and nMOS transistors are designed variable as shown in Table 1:

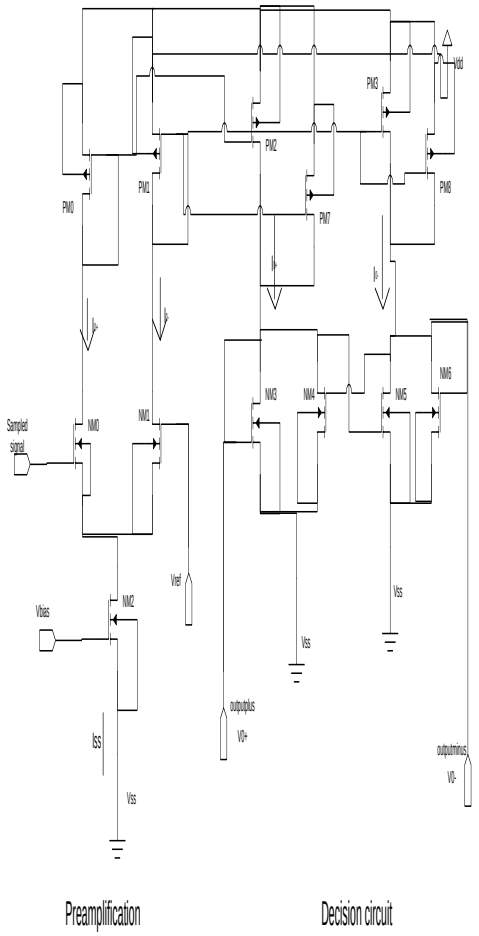


Fig 7: Comparator Design using 65nm CMOS Technology using cadence tool.

When V_{0+}>V_{0-} :-

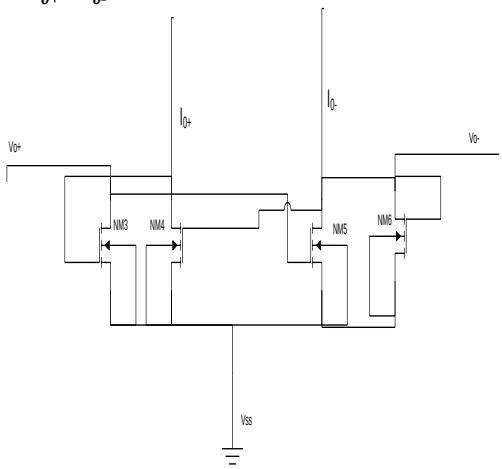


Fig 8: Decision circuit

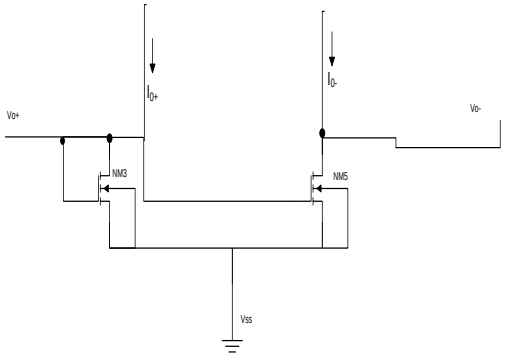


Fig 9: Equivalent circuit when V_{0+}>V_{0-}

Here,NM3 and NM5 are ON and NM4 and NM6 are OFF as shown in above figure 9.Here, all nMOS transistors having equal length and width. Under these circumstances, if V_{0+} is equal to V_{dd} then V_{0-} is equal to Vss.

When V_{0+}<V_{0-}:-

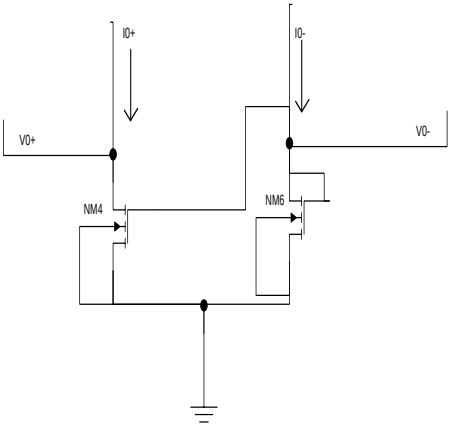
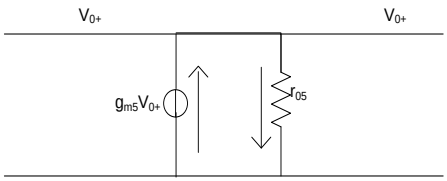


Fig 10: Equivalent circuit when V_{0+}<V_{0-}

Here,NM4 and NM6 are ON and NM3 and NM5 are OFF as shown in above figure 10.Here, all nMOS transistors having equal length and width. Under these circumstances, if V_{0+} is equal to Vss then V_{0-} is equal to $-V_{dd}$.



Case 1:

Apply KCL law,

$$-I_{0+} + g_{m3} V_{0+} + V_{0+}/r_{03} = 0 \quad (1).$$

$$V_{0+}[g_{m3}+(1/r_{03})]=I_{0+}$$

$$V_{0+}=I_{0+}+[(1/g_{m3})//r_{03}]$$

$$[V_{0+}/ I_{0+}]=(1/g_{m3})//r_{03} \quad (2)$$

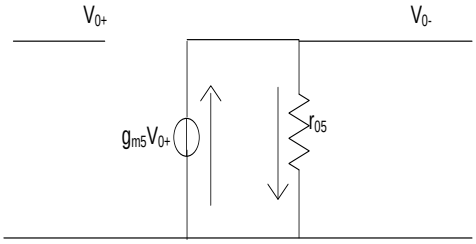
Here , $I_{0+}= I_{0+}$ because (W/L) of all nMOS are same. So, the transconductance of NM3 and NM5 are as follows:

$$g_{m3}=\mu_n C_{ox}(W/L)_{NM3}(V_{gs}-V_t)$$

i.e., here gate and drain are shorted. So, the nMOS NM3 is always in saturation. Let us consider channel length modulation effect,

$$g_{m3}=\mu_n C_{ox}(W/L)_{NM3}(V_{gs}-V_t)$$

$$g_{m3}=\mu_n C_{ox}(W/L)_{NM3}(V_{o+}-V_{t,NM3}) \quad (3)$$



Case 2

Similarly,

$$g_{m5}=\mu_n C_{ox}(W/L)_{NM5}(V_{o+}-V_{t,NM5}) \quad (4)$$

Here, as applying body effect is zero, the threshold voltage of NM3 and NM5 should be same. So,

From equations [3] and [4] then.,

$$g_{m5}= g_{m3}$$

Hence, from above figure from case-2:

$$V_{0-}=-g_{m5}r_{05}V_{0+} \quad (5)$$

$$Z_{in,V0+}=[V_{0+}/ I_{0+}]=(1/g_{m3})//r_{03} \quad (6)$$

$$Z_{in,V0-}=r_{05} \quad (7)$$

Here, from equation (5),$V_{0+}=V_{0-}$ with 180^0 phase shift.

4.3.4 Post amplification

Output Buffer:

In order to achieve high voltage gain along with limited input supply voltage, the output load must be as much as maximum. If such a stage is to navigate a low impedance load, then a source follower must be place after the decision making circuit to drive a load with negligible loss of the signal level i.e., the source follower can operate as a voltage buffer. In this proposed design the nonlinearity due to body effect can be eliminated by connected the body terminal or bulk is tied to the source terminal. The circuit diagram as shown in Figure 11:

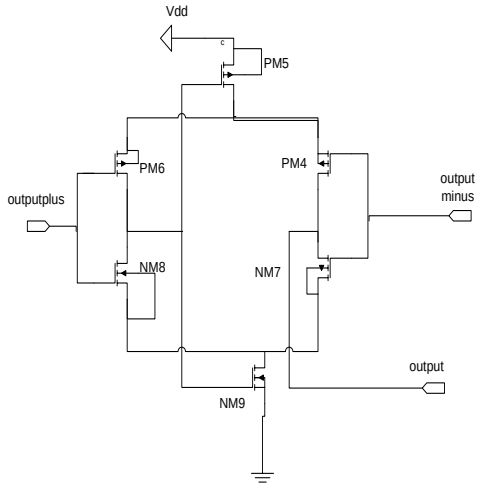


Fig 11: Common Drain schematic circuit

Table I: Transistor sizes

Transistor	*(W(um)/L(nm))*	*Transistor*	*(W(um)/L(nm))*
PM0	8.22/60	NM2	2/60
PM1	8.22/60	NM3	2/60
PM2	8.22/60	NM4	2/60
PM3	8.22/60	NM5	2/60
PM4	4/60	NM6	2/60
PM5	4/60	NM7	2/60
PM6	4/60	NM8	2/60
NM0	2/60	NM9	2/60
NM1	2/60	PM7	4/60
PM6	4/60	PM7	4/60

4.4 Encoder Design

Multiplexer is the building block of the decoding section. The Flash ADC is implemented using Thermometer code itself as select line because of considering speed and power consumption. The design are implemented using multiplexer 2*1.Here, each box is 2*1 mux. It offers better decoding speed and minimum power consumption compared to Fat Tree based decoder.2x1 multiplexers connected as a tree constitutes the decoder structure. These decoders provide a short critical path and small area. Depending upon the method of implementation of truth table, multiplexer (MUX) based decoder is of two types. First type of decoder uses output Binary code as multiplexer select lines and the second one uses thermometer code as select lines.

The width and length of pMOS and nMOS transistors are same as (2um/60nm).

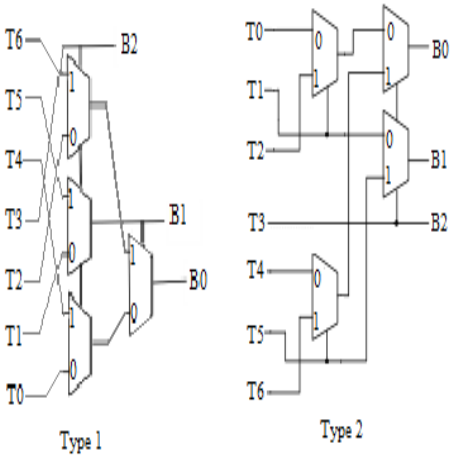


Fig 12: encoder design using2*1 mux with both types of select lines

5. SIMULATION RESULTS

5.1 Sample and Hold circuit

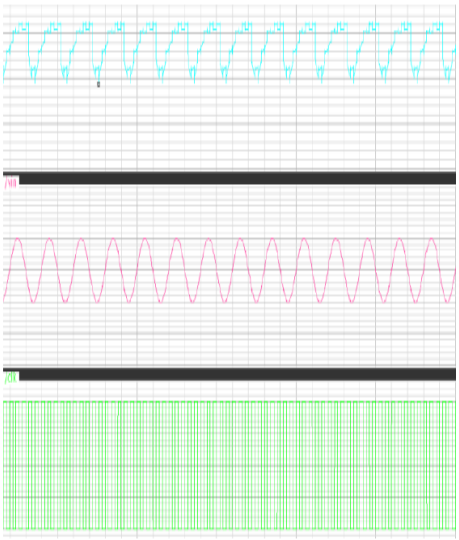


Fig 13: Sample and Hold Circuit of sampling frequency of 20M samples per sec

5.2 Comparator Design

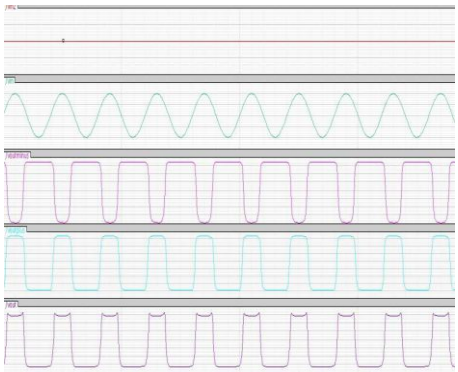


Fig 14: Comparator design using Cadence 65nm CMOS Technology

5.3 Output of FLASH ADC

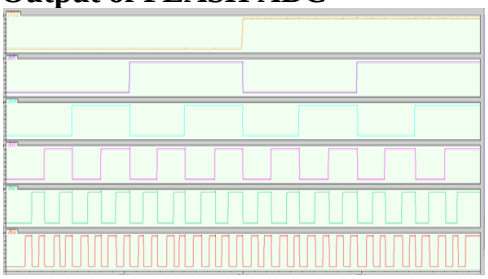


Fig 14: Output of FLASH ADC using transient analysis with input as pulse signal

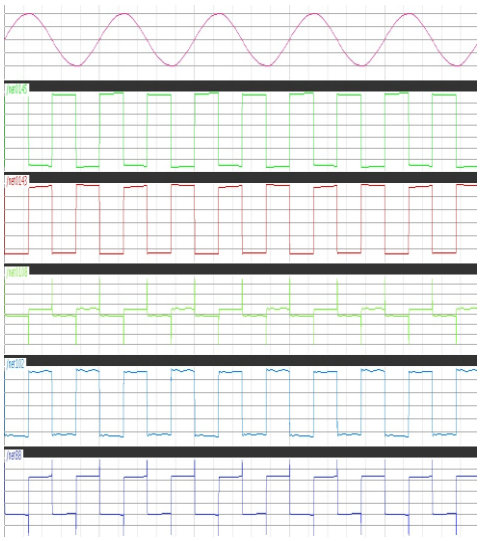


Fig 15: Output of FLASH ADC using transient analysis with input as sinusoidal signal

6. COMPARISON RESULTS

Performance Summary

Parameters	*Conventional work*	*Proposed work*
Technology	180nm CMOS	65nm CMOS
Resolution	7 bit	3 bit
Max.Sampling rate	1GS/s	1GS/s
Supply voltage	900mv	0.65-1 volt
Input range	280mV(p-p)	280mV(p-p)
Input Frequency(max)	97.8MHz	1G Hz
Offset Voltage(mV)	196.81	225.36
Slew rate	.256(V/µsec)	75.59(V/µsec)
Power consumption	494.2mW	249.5mW
LSB	7.87mV	28.7mV
DNL	-0.1 to +0.1 LSB	~0.5 to 0.5 LSB
Propagation delay	24.71(usec)	232.4(psec)

7. CONCLUSION

The proposed circuit is tested and verified in various aspects. The speed, resolution, supply voltage and clock frequency are considered. The circuit is able to resolve small difference in voltage as low as 5m volts when operating at 1V input power supply voltage, with clock frequency of more than 600MHz using cadence virtuoso on 65nm CMOS Technology. This circuit can be widely used in ADC, when ever speed is required.

8. FUTURE WORK

In order to continue our work on removal of offset voltage in comparator design and a sampler circuit design to work on GIGA samples per sec and to increase a high driving capability of sampling circuit and comparator design and Fat tree encoding to improve speed of Flash ADC design .The future work is switches to Bi-CMOS Technology.

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