Implementation of Multi Level Logic for Digital System

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ABSTRACT
A Multi Logic Memory cell have various logic between one and zero that's why fuzzy logic is also known as multiple-logic level, when the paper work was in plan originally plan was do something in Fuzzy Electronics. Lots of fuzzy systems is been developed already but from observing fuzzy flip-flops working the idea comes for the proposed work. Paper work propose designs of a new fuzzy memory cell(flip-flop) for four logic levels which can hold Logic 0, Logic 1, Logic 2 & Logic 3 total four fix logic .though fuzzy logic deals with approximate logic rather than fix proposed work has fix logic and it is the big difference between proposed work and fuzzy based memory cell. Proposed work also has design an Interfacing module between fuzzy memory with Digital) systems, just for make proposed four logic flip-flop compatible with existing binary logic based digital system application for proposed design that one can reduce the no. of wires required when to establish parallel interface with memory and also one can increase the speed or throughput of simple serial data transfer.

1. INTRODUCTION
Fuzzy Electronics logic also known as many-valued logic it works with theory that is approximate than fixed and rigid. Compare with with traditional logic theory, where binary sets have two valued logic, one or zero, fuzzy logic variables may have a value that lies in degree between 0 and 1. Fuzzy logic has been using to deals the concept of partial truth, where the truth value may range between fully true and fully false.

Binary logic system: Digital electronics circuits that have exactly two possible state either 0 or 1. There are some very simple logic gates that can compute almost everything. Also a different combination of logic gates gives us the Flip flops which can store of the data.'0' and '1' are logical concept of two possible conditions (true & false), for actual presentation of these, there are some standard logic families like ECL, TTL, CMOS etc.

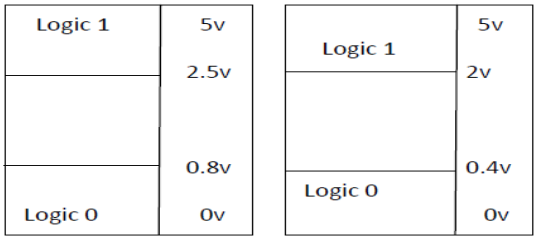

Figure 1 shows the how the logic '1' & '0' exist in the actually, it is in the form of some voltage ranges. **Multi Level Logic:** Fuzzy logic can have many logic between true and false, here paper work proposed a type of Fuzzy logic which has four logic levels Logic '0', Logic '1', Logic '2' & Logic '3' as showed in Figure 2.

Voltage range IN/Out	Multi level logic
0 to 1v	Logic '0'
1 to 3v	Logic '1'
3to 5v	Logic '2'
5 to 6v	Logic '3'

Table 1: The voltage range of our proposed multi level logic

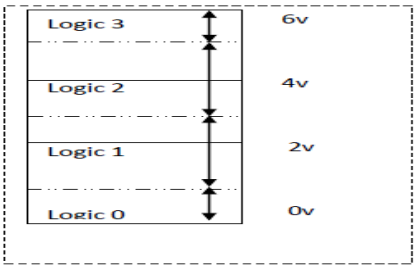

Fig 2: Multi Level Logic

Binary Logic V/S Multi Level Logic: Tables number 2, 3, 4 & 5 shown below to observe the difference between basic Digital binary Logic Gates & Multi level Logic Gate.

Binary AND logic		
Input		Output
0	0	0
0	1	0
1	0	0
1	1	1

Table 2: Binary AND Gate

Binary OR logic		
Input		Output
0	0	0
0	1	1
1	0	1
1	1	1

Table 3: Binary OR GATE

Four logic AND		
Input's		Output
0	0	0
0	1	0
0	2	0
0	3	0
1	0	0
1	1	1
1	2	1
1	3	1
2	0	0
2	1	1
2	2	2
2	3	2
3	0	0
3	1	1
3	2	2
3	3	3

Table 4: Multi Level Fuzzy AND Gate

As from new logic gate, one can also have multi logic level Flip Flop (Cell). A normal binary flip flop can hold only two logic level (i.e. '1' or '0') however proposed Multi Level FF can hold four logic levels. As known a register is a configuration of Flip flops and a configuration of registers is memory (Static RAM), for storing any decimal number range between 0 to 255. It is required to configure 8 Flip-flops in one register as shown in the figure 2, and it used by memory for store 1 byte

Four logic OR		
Input's		Output
0	0	0
0	1	1
0	2	2
0	3	3
1	0	1
1	1	1
1	2	2
1	3	3
2	0	1
2	1	1
2	2	2
2	3	3
3	0	3
3	1	3
3	2	3
3	3	3

Table 5: Multi level Logic OR Gate

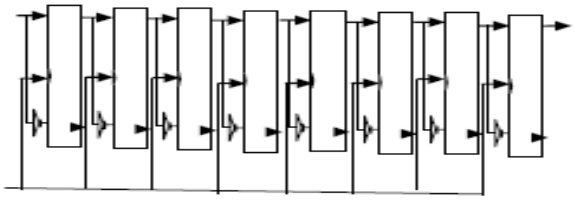

Fig 3: Binary FF based Register for storage of decimal range 0 to 255

But if concerns about Multi Level Register for storing the decimal number ranges between 0 to 255. There need of Multi Level proposed flip-flops only as shown in figure 3. Proposed memory cell will use to store 4 Multi Level logic (0 or 1 or 2 or 3).

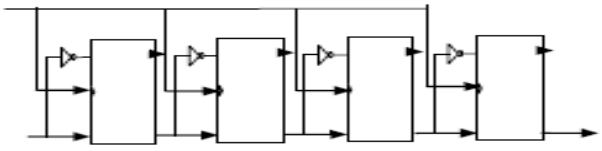

Fig 4: Multi Level Fuzzy Register for storage of decimal range 0 to 255

2. TOOLS & PLATFORM USE

Xilinx ISE 9.2i Software: This EDA tool supports the Integrated Software Environment (ISE).It also generate bit file (netlist file) so it can implement RTL code design on FPGA.

Tanner EDA: Tanner EDA provides a full line of software solutions for full custom design and also catalyzes innovation for the design, schematic and verification of analog and mixed signal (A/MS) integrated circuits (ICs).

3. RESULTS

Figure 5 shown below is the schematic design S-edit of proposed multi level logic AND gate designed by Tanner T-spice pro v6.02

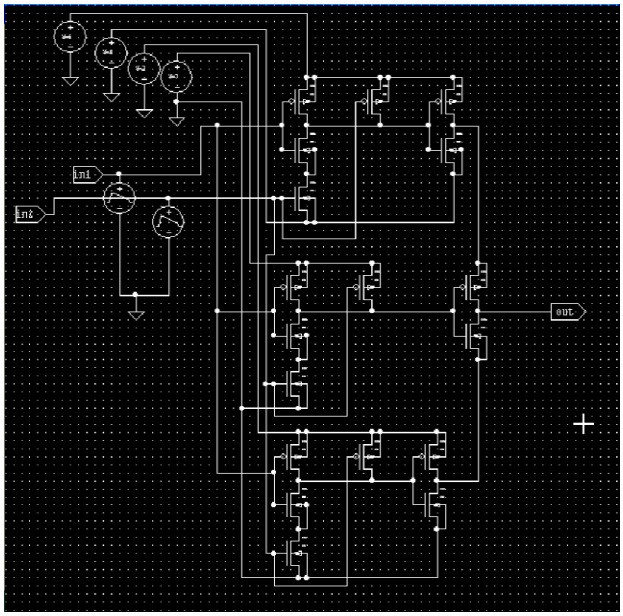

Figure 5: Multi level AND logic gate

Figure 6 is the simulation result generated using Tanner tool for the schematic shown in the figure 4.

Figure 7 is the S-edit schematic design of multi level logic OR gate designed by Tanner T-spice pro v6.02

Figure 8 is the simulation result generated using Tanner tool for the schematic shown in the figure 5.

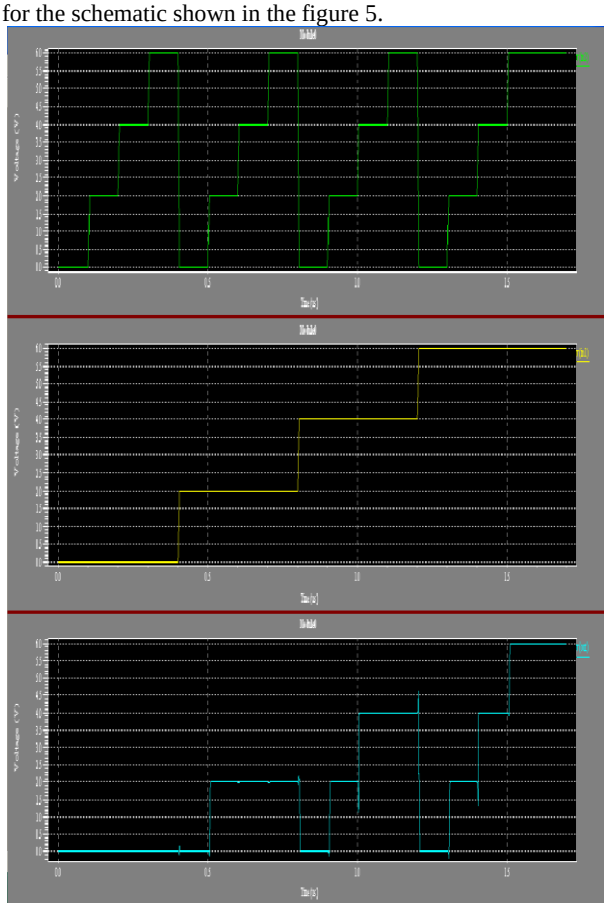

Figure 6 Simulation of Multi level AND Logic

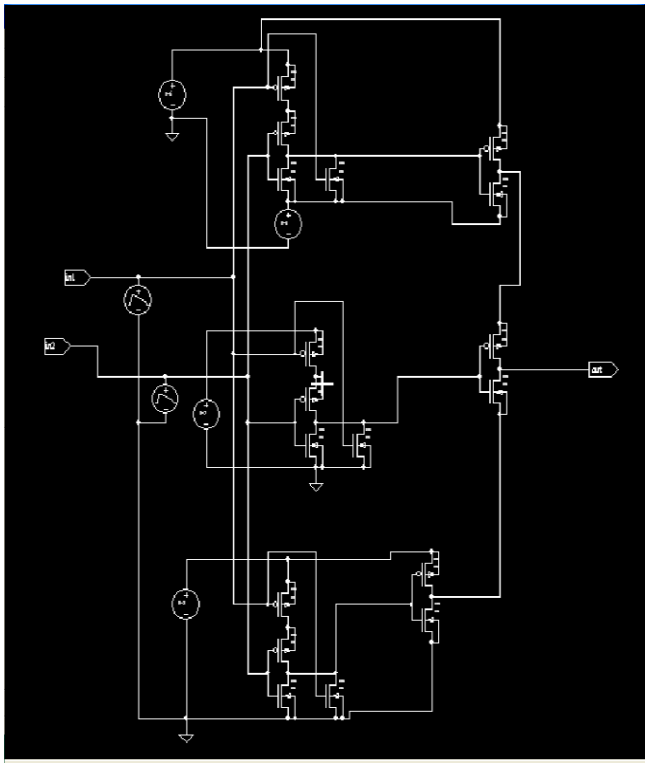

Figure 7 Multi Level OR Logic gate

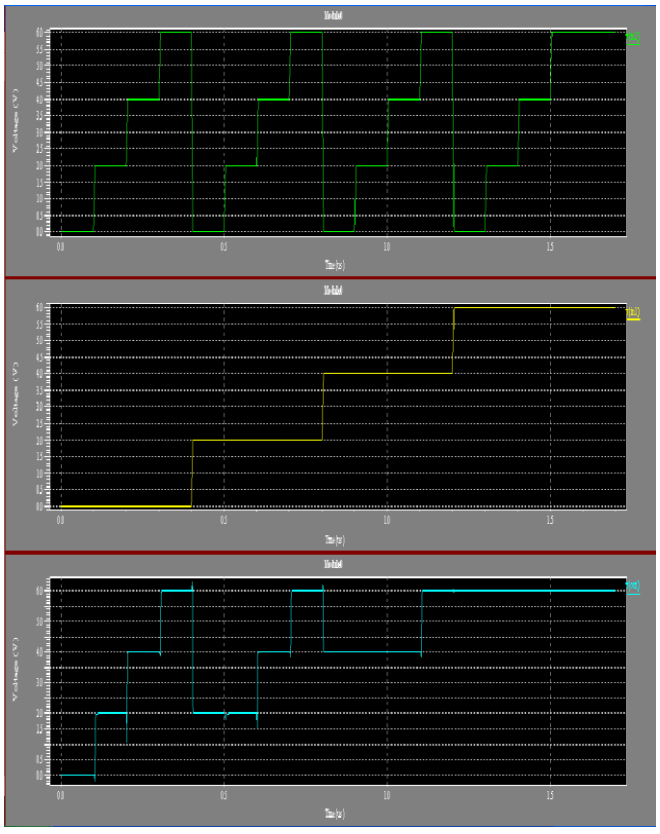

Figure 8 Simulation of multi level OR Gate

Results are been verified correctly and observed as was expected but there is only one problem of noise margin this logic proposed design provides noise margin of only 0.7 v.

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4. CONCLUSION

In here, proposed work concentrated on digital approaches, which results in multi valued logic gates. Proposed work slightly modified already done designs of the many valued AND gate & OR gate in an try to test them using digital components or using of the-shelf discrete components, the observed test results do not generates ideal outputs. So, future research may focus on the improvement on the realization of multi valued logic gates also the improvement on the realization of fix multi-valued logic gates. The proposed design observed results are verified in local environment with ideal transistor parameters and found good and expectable but still more precision can be done in future. The power consumption of the proposed design is 3.95 mW which is less as compare to previous designs and transient time is 157ms which give a good throughput for the proposed flipflop.

5. REFERENCES

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