PLC based Implementation of Fuzzy Controller for Boost Converter

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ABSTRACT

In this paper, the two-input fuzzy logic controller (FLC) and proportional –integral–derivative (PID) controller for boost converter output-voltage regulation are proposed by using Siemens Programmable Logic Controller (PLC). Here the output voltage has been used as a closed loop feedback to determine the output voltage error (e) and the change in error (Δe) as two inputs to the controller. The elements of the boost converter as inductance and capacitor have been selected to insure continues operating mode (CCM) and low output voltage ripple. The proposal is implemented by using Programmable Logic Controller (PLC) on 150 watts prototype and compare (FLC) with (PID) results. The experimental results show that the FLC has a good output voltage response compare with PID controller response.

General Terms

Fuzzy logic controller (FLC), Programmable Logic Controller (PLC), continues operating mode (CCM)

Keywords

Fuzzy logic controller (FLC); proportional –integral–derivative (PID) controller; Programmable Logic Controller (PLC),

1. INTRODUCTION

Dc-dc power converters are widely used in industrial and domestic applications. From control point of view, operation of these converters can be considered as a tracking issue, where the output voltage (Vo) is required to follow a reference command with low transient and low steady state error. The dc–dc converters provide a dc output voltage controlled with pulse width-modulation (PWM) switching technique. The two general methods to control switching operation are: 1) current-mode control and 2) voltage-mode control. The first method uses outer output voltage loop that senses the output voltage and inner current loop that senses the inductor current for feedback purposes. The second method uses a closed loop that senses the output voltage for feedback [1], [2]. In this paper, the close loop voltage feedback control method has been used due to its simplification. In the first step of the experimental procedure, the output voltage is measured and reduced to calculate the error and the change in error.

Recently, the fuzzy logic controller (FLC) as nonlinear controller to control power electronic converters design and implementation sides receiving increasing attention [3]-[9].Also, there are several researches study using of conventional proportional –integral–derivative (PID) controller [10] – [16]. The idea to have a fuzzy logic controller system in dc-dc converter is to ensure desired

voltage output can be produced efficiently as compared to proportional –integral –derivative (PID) system. To improve the converter's performance like providing less overshoot and a faster settling time fuzzy logic based controller is designed [17]. As a result, the linear controller could not perform adequately when subjected to large load variation. In addition, the linear controller may sustain difficulty in handling momentary input voltage reference change [16]. Therefore, the fuzzy logic controller (FLC) is used to overcome these constraints as non-linearity. The performance of closed loop circuit (with FLC) is better than the open loop circuit, where there are no overshoot and better settling time compared to open loop [18].

The aim of this paper is to design a fuzzy logic controller based on Programmable Logic Controller (PLC) and show the effect of the load variation on the system behavior and compare the results with PID controller results.

"Fig. 1," represents the block diagram of the system. In this system, the output voltage (Vo) has been scaled down to fit the analog input of the PLC (0-10V), this analog input has been used to calculate the error and the change in error then feed them to the control program (PID or FLC) that is written by using Structured Control Language (SCL) at the SIMATIC S7 CPUs . (SCL) is a high-level, PASCAL - based programming language. The FLC program determines the change in the duty cycle (ΔD) then duty ratio (D) of the MOSFET switching device. The change in the duty cycle (ΔD) is added to the previous duty ratio (D). The desired duty ratio (D) is applied to Pulse Width Modulation (PWM) generator, the generator output is applied to photo coupler driving the switching MOSFET transistor.
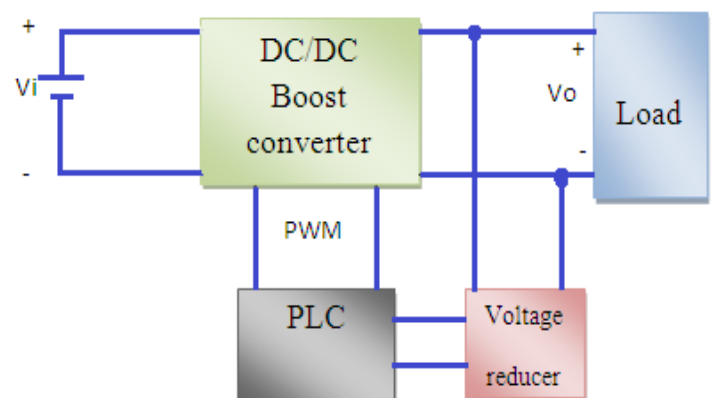

Fig 1: The block diagram of the system

2. BOOST CONVERTER COMPONENTS SELECTION

Fig. 2 shows the components of the boost converter electric circuit that is chosen as following sections.

2.1 Inductor

The selection of inductor (L) affects the operation mode of the boost converter. Small value of (L) causes discontinues mode of operation while large value of (L) ensure continuous mode of operation. The minimum value of the inductor that maintains continuous mode can be obtained as [19]:

$$L_{min} = \frac{R.D.(1-D)^2}{2f_s} \qquad (1)$$

Where, L_{min} is the minimum value of the inductor, fs is the switching frequency "Hz" and R is the output resistance (Ω).

$$V_o = \frac{V_i}{D} \qquad (2)$$

Using switching frequency fs 10 kHz, the maximum expected duty ratio 0.6 and maximum R value 15Ω, from equation 1:

L_{min}=0.072 mH.

L = 0.8 mH to insure continuous current mode operation.

2.2 Capacitor

While, capacitor value affects the ripple of the output voltage (Vo), to maintain an acceptable ripple value (ΔV), approximate expression for the required capacitance can be driven as [19]:

$$C_{min} = \frac{V_o.D}{f_s \Delta V_o.R} \qquad (3)$$

Where, Cmin is the minimum value of the capacitor.

Using switching frequency f_s 10 kHz, the maximum expected duty ratio 0.6, minimum R value 7.5Ω and ΔV value is 0.2V, from equation 3:

C_{min}= 1200 µF

C = 3300 µF to insure low output voltage ripple.

3. FUZZY LOGIC CONTROLLER

Here, two inputs and one output Fuzzy Logic Controller has been used. The first input is the voltage error, the second is the change in error and change in duty cycle (ΔD) is the output. The FLC is represented in Fig.3. The adapted membership functions of the inputs and output are shown in Fig.4 and Fig.5, rules as in Table. 1.
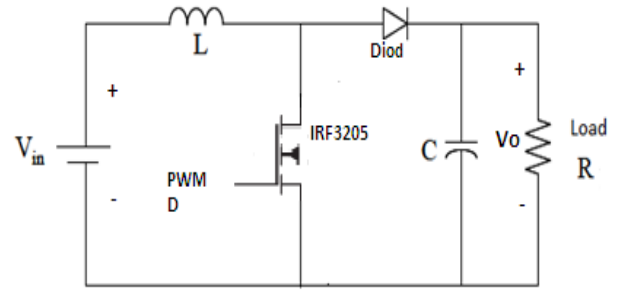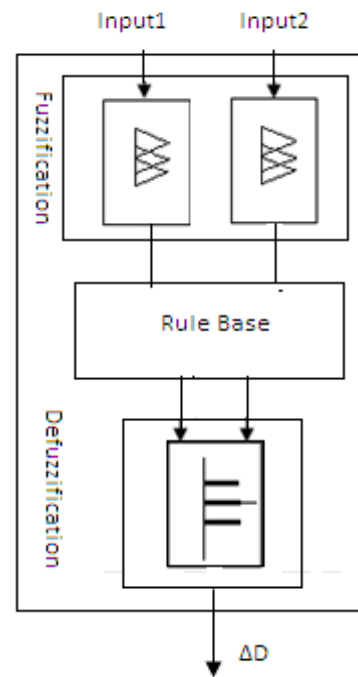

Fig 2: Power circuit of the boost converter.

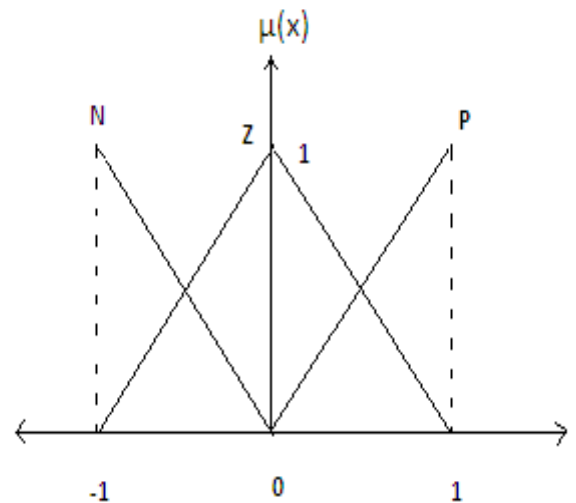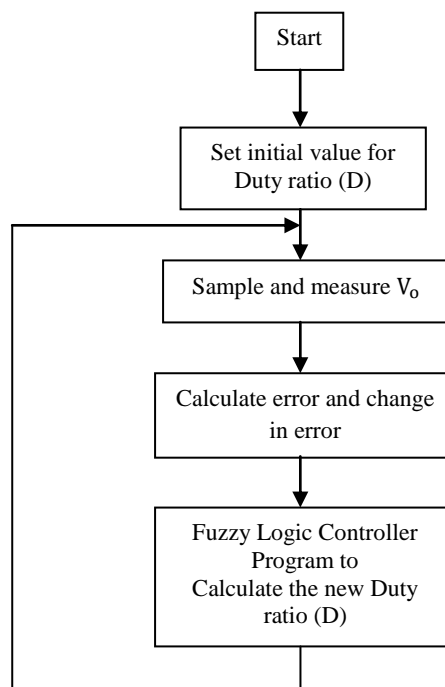Fig 3: Fuzzy Logic Controller Structure
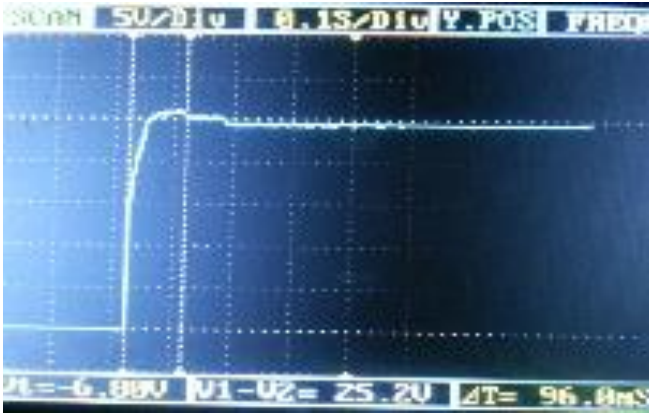

Fig 4: The membership functions set of the inputs.

Fig 5: The membership functions set of the output.

Table 1. Rules of duty change ∆D

∆e \ e	N	Z	B
N	N	N	N
Z	N	Z	P
P	Z	P	P

Where, N is Negative, Z is Zero and P is Positive.

 As example of the utilization of the table above the rule: IF (e is P) AND (∆e is Z) THEN(∆D is P). This rule states that when the error is (P) and the change in error is zero ,that's mean the output voltag is less than the designed voltage (Vref), but there is no change in the value of the output voltage, that's mean the duty cycle must be increased, therfore the new duty (D) must increase by positive (P) ∆D to increase output voltage. The defuzzification method that is used is weighted average method. This method is valid for symmetrical output membership functions as singleton [20]. Each membership function is weighted by its maximum membership value. The output is defined by

$$y = \frac{\sum \mu(x_i).x_i}{\sum \mu(x_i)} \qquad (4)$$

where μ(x_i) is the maximum of the ith membership function, x_i is the ith input value and y is the output function value.

Fig 6: PID Controller Structure

4. PID CONTROLLER

The PID controller is demonstreted in Fig. 6, the PID controller parameter are tuned to give the optimal performance; K_p. = 0.0001, K_i = 10.0 and K_d= 0.00021. The PID equation is:

$$\Delta D = K_p.e + \int K_i.e \ . \ dt + K_d \ . \ \frac{de}{dt} \qquad (5)$$

5. EXPEREMENTAL RESULTS

The proposed control systems are implemented in Programmable Logic Controller (PLC) and tested on the system as in Fig.7. The PLC program flow chart for (FLC) is as in Fig.8, when the system start-up, the duty ratio (D) is set to intial value and applied to MOSFET gate .The converter output voltage (Vo) is measured with sample time (1 msec and resolution of 12bit). Error (e), is the difference between the reference voltage (Vref) and output voltage (Vo), is calculated, also change in error (∆e) is the difference of the current error and previous error, then e and ∆e are applied to FLC program to find the new ∆D that's added to the previous duty ratio (D) to compensate the voltege error.

The PLC program flow chart for PID is as in Fig.8 but by replacing the Fuzzy Logic Controller with PID controller.

Fig 7: The proposed control system implementation.

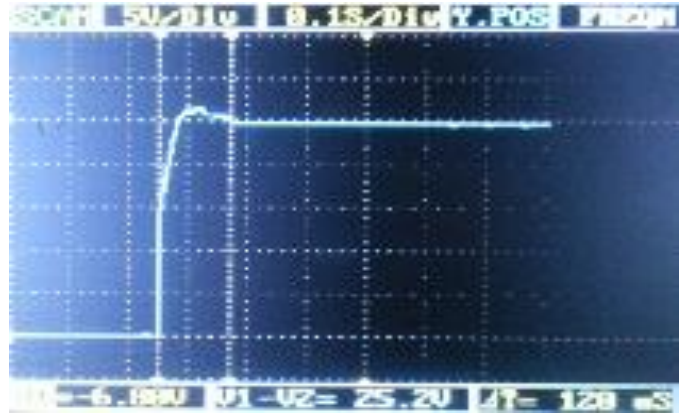**Fig 8: Flow chart of the PLC program.**

a. R=7.5Ω,Vin=12V&Vref=24V(5V/div&0.1s/div)

b. R=15Ω,Vin=12V&Vref=24V (5V/div&0.1s/div)

c: R=7.5Ω,Vin=12V&Vref=30V(10V/div&0.05s/div)

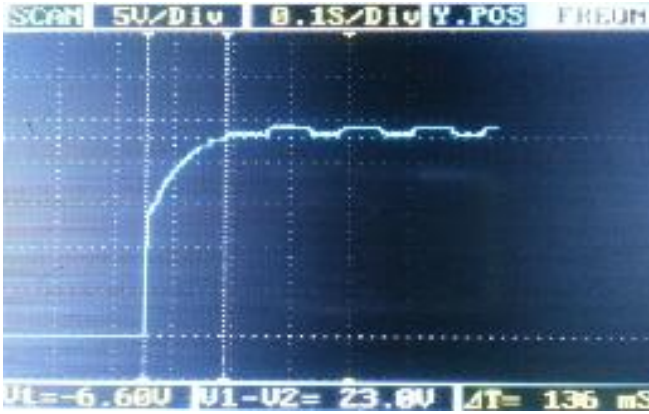**d: R=15Ω,Vin=12V&Vref=30V(10V/div&0.1s/div)**

e: R=7.5Ω,Vin=24V&Vref=30V(10V/div&0.1s/div)

f: R=15Ω,Vin=24V&Vref=30V(10V/div&0.1s/div)

Fig 9: Startup phase for different loads and different output and input voltages under Fuzzy Logic Controller technique

Fig.9.(a, b, c, d, e and f) represent the system start-up phases response under fuzzy logic controller technique for different loads with input voltages and output reference voltages as shown above. Fig.9.(a, b, c, d, e and f) which take approximately rise time 18 msec, 25 msec, 16 msec, 20 msec, 10 msec and 5 msec respectively and the settling times (with 5% error) are 136msec, 120msec, 26msec, 104msec, 160msec and 172msec respectively

with overshoot 4.16%, 8.33%, 0.0%, 23.33%, 70% and 100.07% respectively.

a: R=7.5Ω, Vin=12V&Vref=24V(5V/div&0.1s/div)
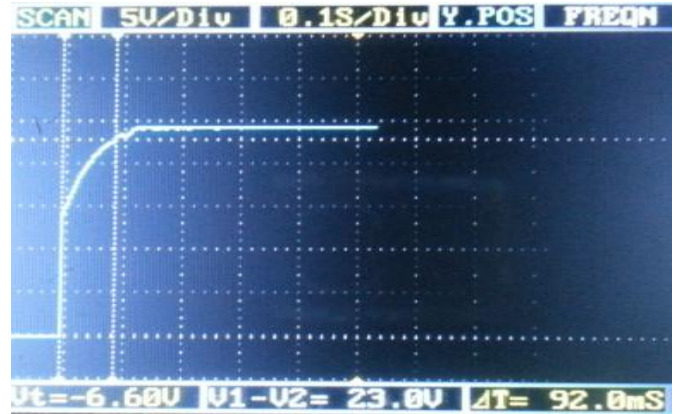
b: R=15Ω,Vin=12V&Vref=24V(5V/div&0.1s/div)

c: R=7.5Ω,Vin=12V&Vref=30V(5V/div&0.1s/div)
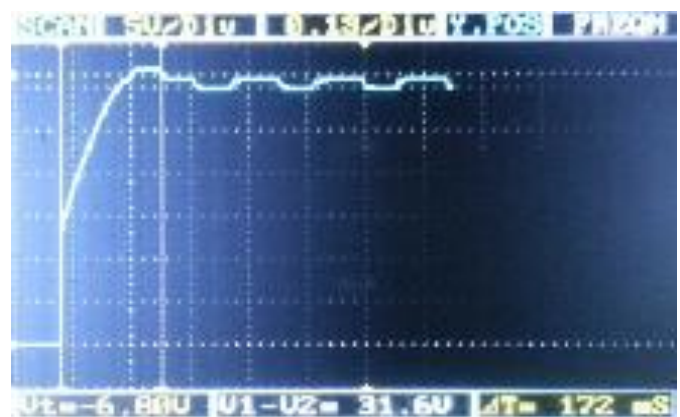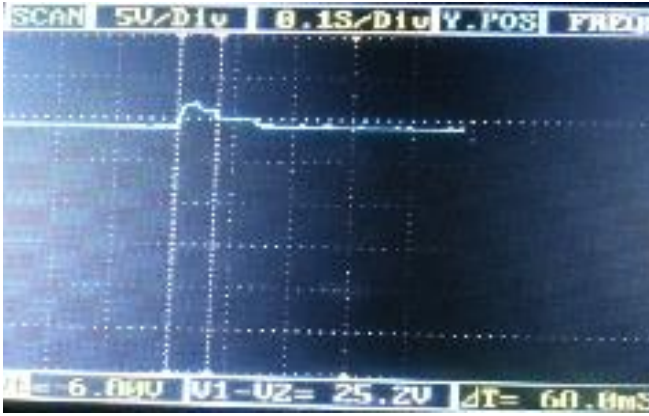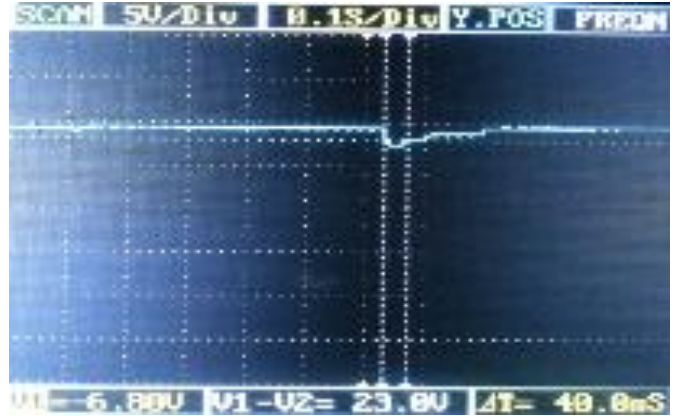
d: R=15Ω,Vin=12V&Vref=30V(5V/div&0.1s/div)
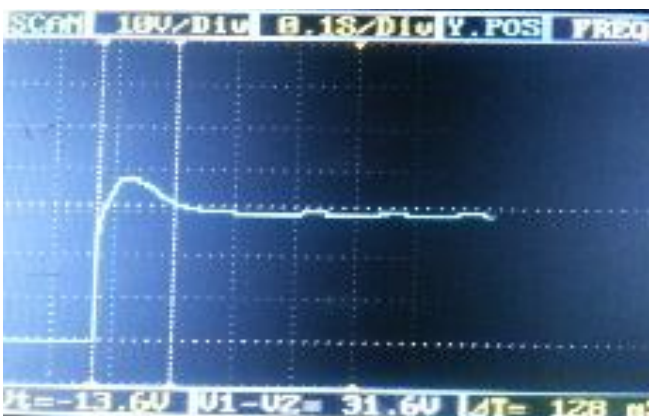
e: R=7.5Ω,Vin=24V&Vref=30V(10V/div&0.1s/div)
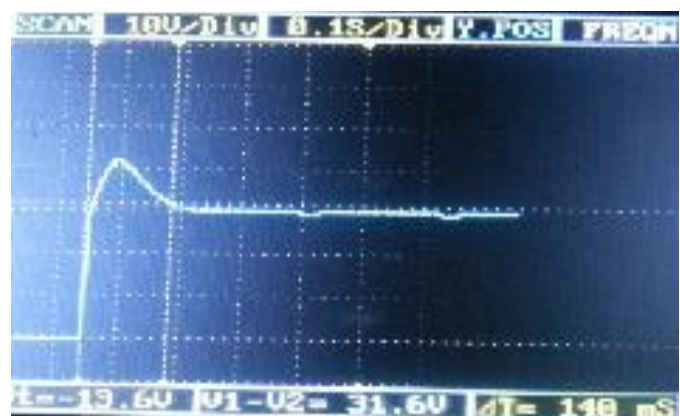
f: R=15Ω,Vin=24V&Vref=30V(10V/div&0.1s/div)

Fig 10: Startup phase for different loads and different output and input voltages under PID controller technique.

Fig.10.(a, b, c, d, e and f) represent the system start-up phases response under fuzzy logic controller technique for different loads with input voltages and output reference voltages (Vref) as shown above. Fig.10.(a, b, c, d, e and f) which take approximately rise time 53msec, 76msec, 10msec, 82msec, 15msec and 10msec respectively and the settling time (with 5% error) are 96msec, 92msec, 126msec, 172msec, 128msec and 140msec respectively with overshoot 0.0%, 0.0%, 0.0%, 6.67%, 26.6% and 40% respectively.
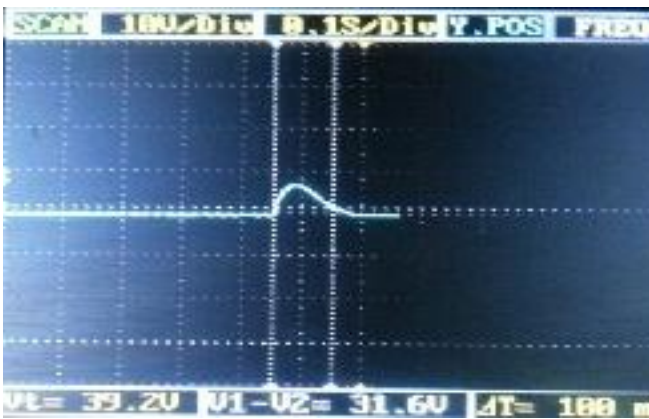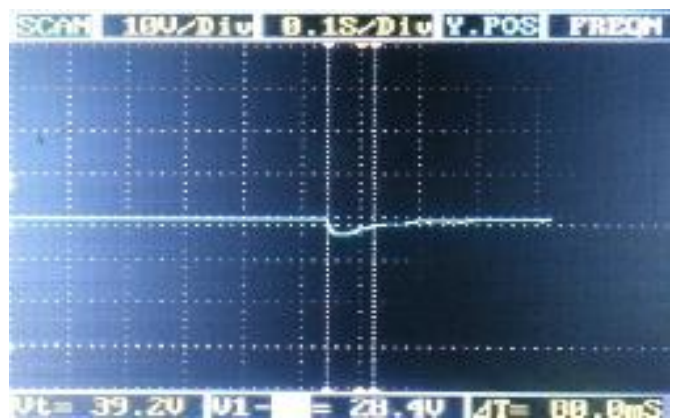
a: R=7.5-15Ω,Vin=12V&Vref=24V(5V/div&0.1s/div)

b: R=15-7.5Ω,Vin=12V&Vref=24V(5V/div&0.1s/div)

c: R=7.5-15Ω,Vin=12V&Vref=30V(10V/div&0.1s/div)

d: R=15-7.5Ω,Vin=12V&Vref=30V(10V/div&0.1s/div)
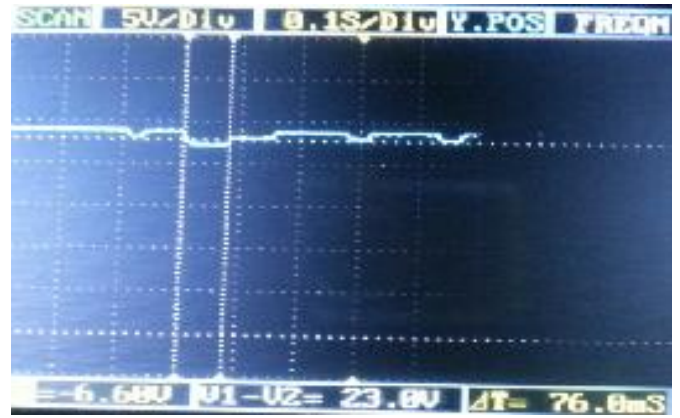

e: R=7.5-15Ω,Vin=24V&Vref=30V(5V/div&0.1s/div)
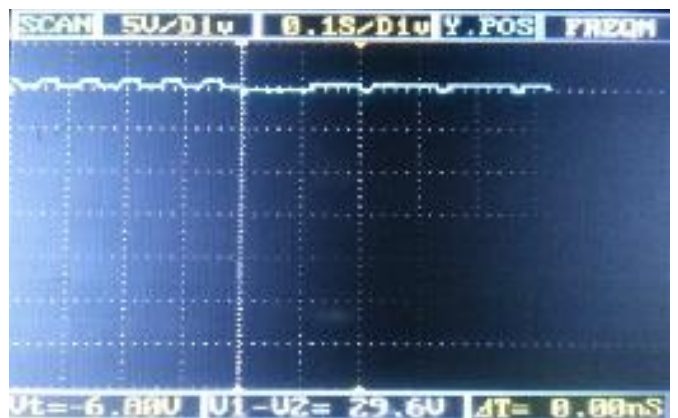
f: R=15-7.5Ω,Vin=24V&Vref=30V(5V/div&0.1s/div)

Fig 11: Load step change for different output and input voltages under Fuzzy Logic Controller technique.
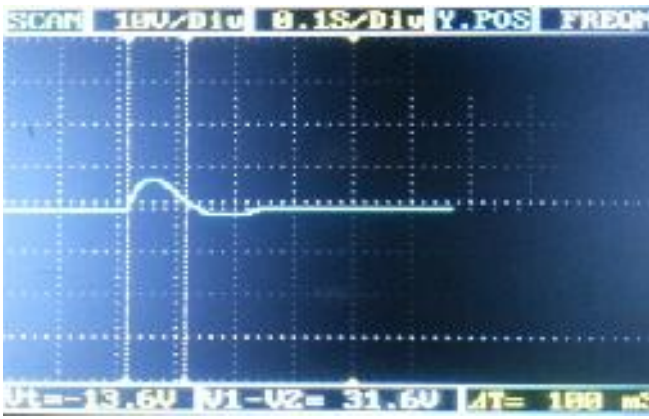
Fig.11 (a, b, c, d, e and f) show the load step change respons for different output and input voltages under Fuzzy Logic Controller technique. In Fig.11 (a, b, c, d, e and f) the time required to return the previous output voltages are approximately 60msec, 40msec, 100msec, 80msec, 20msec and 0.0msec respectively.
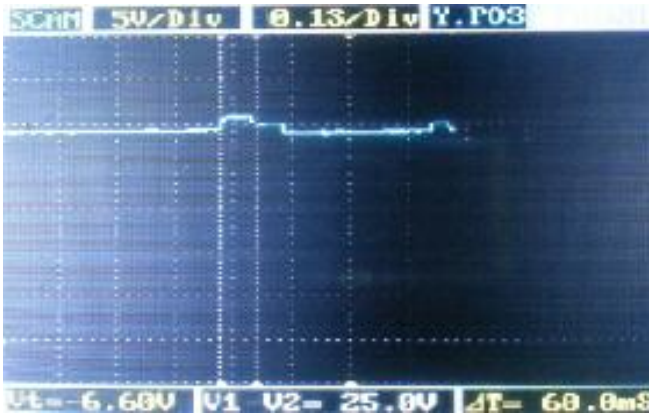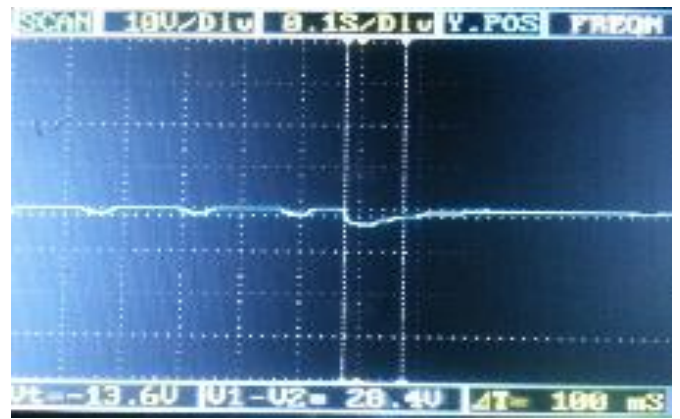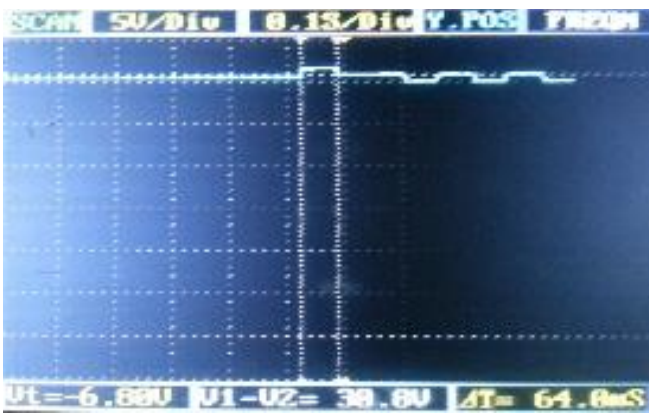
a: R=7.5-15Ω,Vin=12V&Vref=24V(5V/div&0.1s/div)

b: R=15-7.5Ω,Vin=12V&Vref=24V(5V/div&0.1s/div)

c: R=7.5-15Ω,Vin=12V&Vref=30V(10V/div&0.1s/div)

d: R=15-7.5Ω,Vin=12V&Vref=30V(10V/div&0.1s/div)

e: R=7.5-15Ω,Vin=24V&Vref=30V(5V/div&0.1s/div)
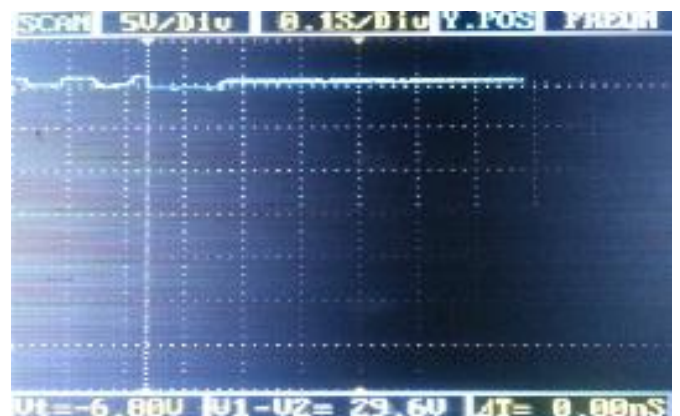
f: R=15-7.5Ω,Vin=24V&Vref=30V(5V/div&0.1s/div)

Fig 12: Load step change for different output and input voltages under PID Controller technique

Fig.12 (a, b, c, d, e and f) show the load step change respons for different output and input voltages under PID Controller technique. In Fig.12 (a, b, c, d, e and f) the time required to return the previous output voltages are approximately 60msec, 76msec, 100msec, 100msec, 64msec and 0.0msec respectively.

6. CONCLUSI0N

This work presents a dc power supply system with boost converter, in which a Programmable Logic Controller PLC has been used to retrieve the voltage of the boost converter circuit by increasing or decreasing the duty of the MOSFET switch to achieve the desired output voltage. Additionally, this

work adopts the frequently used PID and FLC. As it is clear from Fig.9(a, b, c, d, e and f) and Fig. 10.(a, b, c, d, e and f), the start-up response of boost converter for different loads using FLC with the shown input voltage (Vin) and output reference voltage (Vref), the response curves have rise times and settling times less than that for PID with the same Vin and Vref, but the FLC has an overshoot ratio higher than that for PID response only in Fig.9. (b, d, e and f) and Fig. 10.(b, d, e and f). Also the response curves of the load step change mode using FLC have settling time less than that for PID response curves.

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