Parametric Fault Detection of Analogue Circuits

Sherif Anas
Egyptian Armed Forces

Mohamed H. El-Mahlawy
Egyptian Armed Forces

Mahmoud E. A. Gadallah
Modern Academy, Maadi, Cairo, Egypt

Emad A. El-Samahy
Egyptian Armed Forces

ABSTRACT
This paper presents a new testing approach for analogue circuits based on the digital signature analysis. In this paper, the efficient parametric fault detection approach for analogue circuits using the simulation environment is presented. This approach has three main parts, an analogue test pattern generator (ATPG), an analogue test response compactor (ATRC), and an analogue circuit under test (ACUT) model, build in the PSpice circuit simulator. The proper ATPG is designed to sweep the applying sinusoidal frequencies to match the frequency domain of the ACUT. The output test response of the ACUT is acquired via the analogue-to-digital converter (ADC). The ATRC accumulates digital samples of the output response from the ADC to generate a digital signature that can characterize the situation of the ACUT. The signature comparison is achieved based on signature boundaries based on the worst-case analysis. In addition, the signature curve for each component variations of the ACUT is presented to be illustrated as image of some parameters affected in the transfer function of the ACUT. It combines effective parameters of the transfer function of the ACUT with respect to the component variations. These parameters are the band-with and the passband transmission. Using the signature curve, a parametric fault of each component of the ACUT can be detected under the sweep sinusoidal frequency of the ATPG. The presented testing approach is applied to the analogue benchmark circuit to validate the presented testing approach.

General Terms
Modeling of analogue circuit testing.

Keywords
Fault detection, Parametric faults, Signature analysis of analogue testing, Testing of analogue circuits.

1. INTRODUCTION
Automatic testing techniques play a great role in industrial applications. They are considered as standard way for detecting faults in analogue electronic systems. Researchers are concentrated their major attention to the automatic testing of the digital systems [1-7]. However, in most cases the digital system exists within an analogue enclosure system. This analogue part of the mixed-signal system requires to be tested for increasing the system performance. Testing applications of analogue circuits are still in research phase. In general, the most challenge of fault detection of the analogue circuits is to unify test procedures to properly generate test signals that are capable of stimulating faults, and to compact the test response for fault detection [8]. The analogue testing has to fit the specifications of the ACUT [9]. In addition, the modeling of hardware defects of the ACUT and the usage of these models for developing and improving test signals is considered another analogue testing challenge.

The manufacturing defects may have two types of permanent faults, namely catastrophic (hard) or parametric (soft) faults [10]. A catastrophic fault is one in which discrete component of a circuit is destroyed (e.g. short circuit, open circuit as well as topological change). With parametric fault, the component is still functioning but out of nominal tolerance band (out of specification). Figure 1 depicts the classification of analogue circuit faults. The range of the acceptance for the good ACUT, and the non-acceptance are illustrated for ± 5 %. Comprehensive researches have been conducted on analogue testing issues. Faults in an analogue circuit may occur due to a catastrophic fault model, considered easily to test. In the parametric fault model, it is hard to test, and its effect is represented by means of the change in circuit output signals.

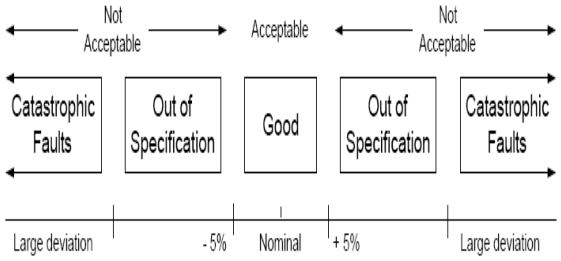

Fig 1: Classification of analogue circuit faults.

Several testing techniques for analogue circuits are attempted. Some testing approaches aim to test analogue circuits based on approximated impulse and step test signals [11-17]. The limitation of these approaches is the requirements generation of the ideal impulse. Therefore, an approximation of large-amplitude and narrow-duration is performed. As an impulse signal is shortened, its amplitude must be increased, and this may overload the ACUT. The shape and scale of the frequency spectrum of an impulse response or a step response is fixed. In other word, the power cannot be concentrated to any arbitrary frequency bands, which is not useful to target specific faults. In addition, impulse and step responses can characterize only linear system, which limits their applicability. The other testing approaches aim to test analogue circuits based on the input binary sequence [18-20]. They require extra hardware for stimulus generation and extra hardware at the output for analogue test response analysis (e.g. ADC or cross-correlators). Binary sequence (Square wave) has fixed frequency spectrum shape depending on the clock frequency. Its frequency spectrum follows the shape of the (sin(x)/x) function and includes only the odd harmonics. The binary signals (Impulse, step, square wave and binary sequence) cannot have more power at any arbitrary frequency bands. Thus, they cannot effectively excite the ACUT at pre-specified parts of the frequency spectrum.

Another testing approach aims to test analogue components in mixed-signal circuits, based on oscillation-based BIST (OBIST) methodology [21]. The limitations with that approach are that the catastrophic faults are considered only. The Multi-Detect test method for test generation is another test approach to identify a set of sinusoids. It forms the test

set that maximizes the difference between the responses of the good and faulty ACUT [22]. A faulty circuit is detected from a deviation of its oscillation parameters. The detection circuitry is provided by a single reference value as a reference input to the response comparator instead of multiple reference values for all faults in an ACUT. The limitations of that approach are the problem of finding the minimum detectability threshold between good and faulty circuits for detecting a fault. Estimating the detectability threshold for a given fault is affected by increased number of components, tolerances associated with each component, evaluation of the complex equations, and measurement accuracy of the response analysis circuit (i.e., comparator circuit). Therefore, this approach became too expensive in terms of computation time. Any attempt to reduce the computation time by using simple design models may result in inaccurate detectability threshold value. The testing approaches, based on wavelet filters to analyze and compress signatures [23], depend on acquiring the ACUT output response, and processing this response via an array of filters, each operates within a defined band, followed by a signature generator and comparison module for each band. The limitation of that approach is not using the multi-tone test input. Since a single frequency component is not effective in detecting faults.

From the most collected published testing approaches of analogue circuits, the practical implementation of the analogue testing focused on the detection of the catastrophic faults in the ACUT, but it has a shortage of the testing application of parametric faults in the ACUT. The main motivate is to build an efficient analogue testing scheme including the multi-test pattern generation capabilities (ATPG) to match the ACUT, the ATRC to characterize the ACUT based on inserted faults and component tolerances. The main objective of this paper is to design, analyze, evaluate, and verify the parametric fault detection approach for analogue circuits using a simulation environment. The proper ATPG is designed to sweep the applying sinusoidal frequencies to match the frequency domain of the ACUT and then is acquiring the output test response, via the ADC. The analogue test response compactor (ATRC) acquires and then compacts digital samples of the output response to generate a digital signature that characterize the situation of the ACUT. The signature comparison is achieved based on the pre-calculated signature boundaries, calculated based on the worst-case analysis of both the minimum and the maximum of the output analogue response of the ACUT using PSpice circuit simulator. In this paper, the presented testing approach enables to achieve the concept of the signature curve generation for each component of the ACUT. Based on this curve, the relation between the digital signatures and the component variations of the ACUT is presented. The signature curve combines the effects of both the band-with (BW) and the passband transmission (Amax) in the amplitude response of the ACUT with respect to the component variations of the ACUT.

This chapter starts with the introduction summary of the new analogue testing approaches. The second section is concerned with the design of the presented new analogue testing approach. Then, the next sections will focus on the PSpice circuit model simulation of the ACUT and the parametric fault analysis of the selected ACUT as case study. Finally, conclusions and contributions obtained in this paper.

2. DESIGN OF THE NEW ANALOGUE TESTING APPROACH

The objective of the presented analogue testing approach is to design the proper ATPG (stimulus) for stimulating the highest possible proportion of all faults, and to design the proper ATRC that can detect the stimulated faults. The main block diagram of the analogue testing architecture, presented in this paper, is shown in Figure 2. This testing architecture is suitable in the external testing approach. The ATRC consists of three sub-modules; the rectifier, the ADC, and the test response compactor (TRC). The rectifier is designed to rectify the negative analogue signal to positive one in the case of the bipolar signals. The ADC is used to convert the analogue signal of the output response of the ACUT into the digital samples. The TRC, composed of the double-precision accumulator, accumulates and compacts the generated samples to produce a digital signature.

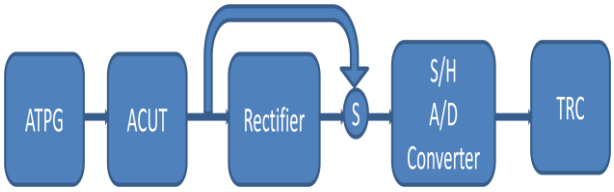

Fig 2: Main block diagram of the presented analogue testing approach.

Most of faults in analogue circuits can affect the frequency response of the ACUT. Therefore, in this architecture, the proper ATPG is designed to sweep the applying sinusoidal frequencies that provide a stimulation to detect faults in a wide range of analogue circuits. The frequency sweep in the sinusoidal waveform can exercise the frequency response of the ACUT. The existence of faults can affect the frequency response of the ACUT, and change the output waveform of the ACUT. Therefore, the change of the generated digital signature from the ATRC will be significant. The transfer function coefficient variations of the ACUT will prevent an exact output response sequence. Unique digital signature cannot be obtained for the fault-free ACUT. Therefore, in this paper, the ATRC function is an accumulator that sums the sample magnitude of the absolute analogue output response. This facilitates the determination of a range of good digital signatures to account for acceptable changes in the output response due to component variations of the transfer function coefficient of the ACUT. The analogue output response is generated from the circuit model of the ACUT to verify the effectiveness of this presented analogue testing approach.

During analogue fault simulation, many parametric faults have been considered for each component of the ACUT, including ±5%, ±10%, ±20%, ±50%, … variations of specified component values, short-circuit and open-circuit (i.e., very small value and very large value) in the component of the ACUT. The analogue fault simulation of the ACUT is performed using in the PSpice circuit simulator to illustrate the effectiveness of the new digital signature approach for analogue fault detection technique. Digital signatures based on the accumulation absolute sum of the sample magnitude of the ACUT outputs during test window can be plotted against the selected component variations of the ACUT, called signature curve with respect to that component. This curve illustrates the classification of the fault-free and the faulty ACUT with respect to that component based on parametric faults.

2.1 Analogue test pattern generator

The frequency change of the input signal, applied to the ACUT, controls the amplitude response of the output response. The rate of the frequency sweep is not a constant, but it may vary with each new generated cycle of the ATPG. In this section, the sweep sinusoidal frequency extraction procedure is used to affect the amplitude response of the ACUT and consequently affect the output response of the ACUT through its time domain I/O relation. Figure 3 illustrates the simulation model of the ATPG in this analogue testing architecture [24]. It is the modeling of voltage controlled oscillators (VCOs) using PSpice circuit simulator. It consists of two parts; the Sin Source Model, and the Integrator Model. A simple form of the VCO is obtained by starting with the time domain function for a sinusoidal source model (sin((2π × fc × time) + phi)). In this example, 2π, fc and phi are all constant global parameters. The single frequency source can be turned into a VCO by making phi a function of a controlling voltage instead of a constant. y(t) = sin (2π fct+φ(t)). The instantaneous frequency is given by the time derivative of total phase: 2πfinst = 2π fc + φ′(t). The relationship between the frequency deviation fd = finst – fc, and φ is given by: φ (t) = ∫ 2π fd(t) dt. For a linear VCO, we want fd to be proportional to the controlling voltage vctrl, therefore: φ (t) = 2π k1∫vctrl(t) dt, where k1 is in Hertz/volt. Using PSpice circuit simulator [24], the integrator can be modeled as a controlled current source plus a capacitor. The varying phase term is added into the controlled voltage (Sine) source.

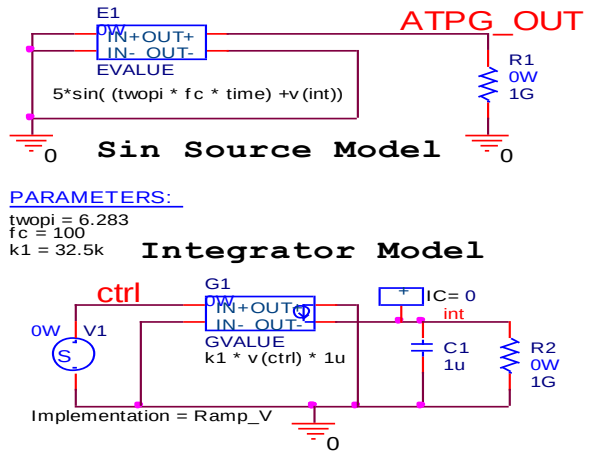

Fig 3: Model of the ATPG model in the PSpice simulation.

Figure 4 shows the timing diagram of the two main control input signals for the VCO model. Control signal CTRL controls the frequency sweep to produce the output signal ATPG_OUT. The generated signal is the mix of multi-frequency sinusoidal signals. Figure 5 illustrates the Fast Fourier Transform (FFT) of the output signals of the ATPG model from 100 Hz to 10 kHz. The amplitude is set to 5 Vpp, fc is set to 100 Hz and k1 is set to 32.5 kHz/volt, according to the model in Figure 3. In addition, Figure 6 shows the FFT of the output signal of the ATPG model. The amplitude is set to 5 Vpp, fc is set to 1.2 Hz and k1 is set to 3.8 kHz/volt. The extracted sinusoidal signals have the frequency sweep from 1.2 Hz to 1.5 kHz. All curves in Figure 5 and Figure 6 can be used to stimulate analogue filter circuits in the frequency range of the biomedical applications.

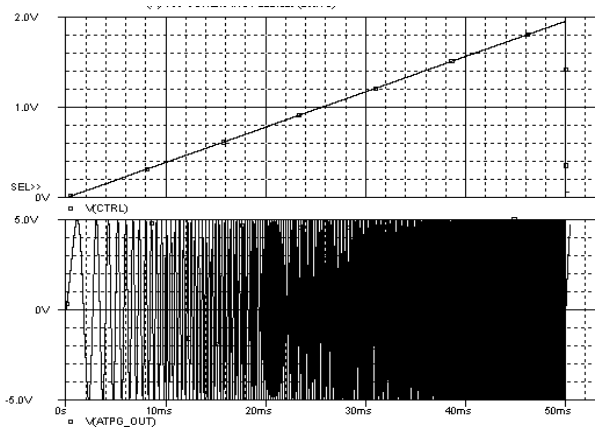

Fig 4: Timing diagram of the ATPG model using the PSpice simulation.

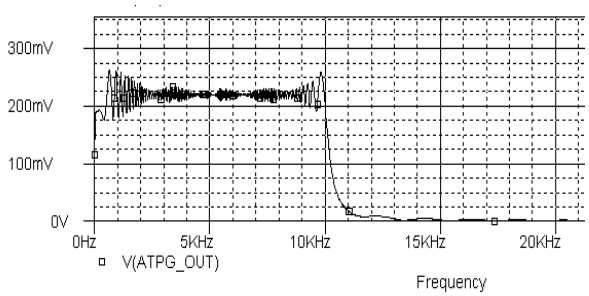

Fig 5: FFT of the output signals of the ATPG model.

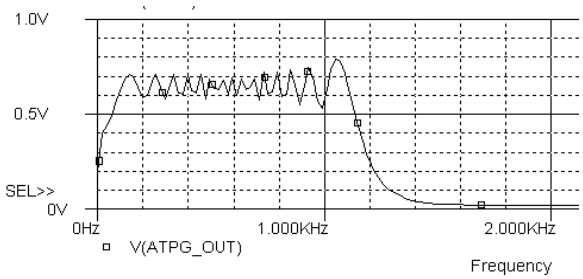

Fig 6: FFT of the output signal frequency from 1.2 Hz to 1.5 kHz.

2.2 Full rectifier circuit and Analogue-to-digital converter

According to Figure 2, the output signal of the ATPG model is applied to the ACUT whose output signal is applied to either the full rectifier circuit or the ADC. The output waveform of the rectifier stage produces unified signal waveform in the positive polarities. The schematic diagram of the full rectifier circuit is shown in Figure 7 [17]. The output signal of the traditional bridge full rectifier has different ground reference. But, the unified signal of the presented rectifier circuit has the same reference ground of the input signals. It is represented by two operational amplifiers (U5B, U5B) in the same integrated circuit (LM324), resistors R4, R5, and R6 and diodes D1, D2, D3, and D4. During the positive direction of the input Sine waveform, diodes D1 and D4 are off and D2 and D3 are on. During the negative direction of the input Sine waveform, diodes D2 and D3 are off and D1 and D4 are on. The unified signal, generated from the rectifier, is applied to an 8-bit ADC model in the PSpice circuit simulator.

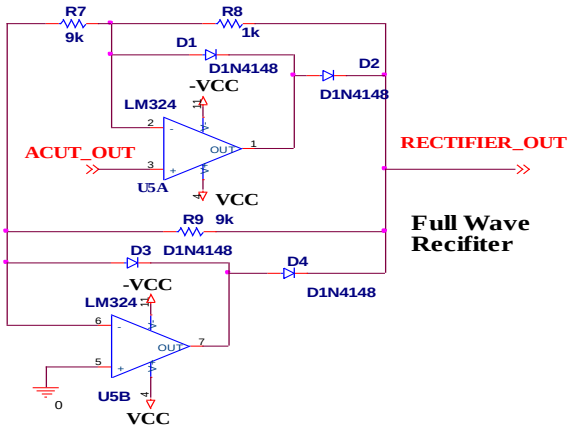

Fig 7: Schematic diagram of the full rectifier circuit.

The ADC is the main part of data acquisition systems. To process applied signals, the sample and hold (S/H) process and data conversion are required. Figure 9 shows the schematic diagram of 8-bit ADC model. The control signal S/H is generated to place the input analogue signal ADC_In in the sample mode and the hold mode, and the control signal RESET is generated to start of the data conversion cycle. The proper data conversion is to sample the analogue signal in the sample mode, and holds the signal constant during the hold mode. The timing is adjusted so that the encoder performs the conversion during the hold time. The control signal S/H clocks the ADC and the input analogue signal ADC_In is converted. Once a conversion cycle is started, it cannot be stopped or restarted until the data conversion cycle is complete and the data is available from the binary output, A[8:1]. Figure 8 illustrates the external connections for the ADC in unipolar input mode. The first output code transition from 0000 0000 to the full-scale transition 1111 1111. The binary data output of the ADC is applied to the test response compactor (TRC) Stage.

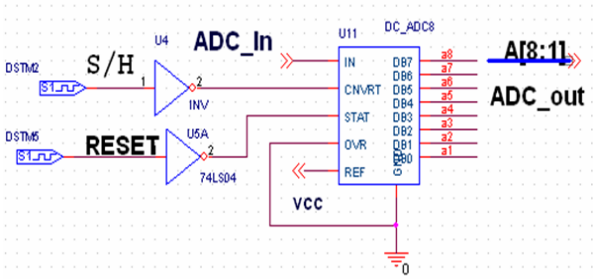

Fig 8: Schematic diagram of the 8-bit ADC model in PSpice simulator.

2.3 Test response compactor

In traditional testing approaches of digital circuits, the good circuit is tested by a digital signature, generated from the linear feedback shift register (LFSR) [3, 5, 7]. In addition, the single-shot circuit is tested by generating a digital signature based on the measurement of the time duration that expresses the proper functionality of the single-shot circuits [25]. In analogue circuits, the test response (TRC) function is design to generate a digital signature based on accumulation weighting sums of the sample magnitude of the analogue output response. These samples are generated from the ADC, and the required digital signature is generated from TRC by accumulating those samples. These samples are based on the analogue output response of the ACUT and the applied signal generated from ATPG. The schematic diagram of the TRC module, shown in Figure 9, is responsible for simulating the TRC scheme in the presented analogue testing. The generated signature from the TRC module can represent the analogue output response of the ACUT in the criteria of the ACUT judgment.

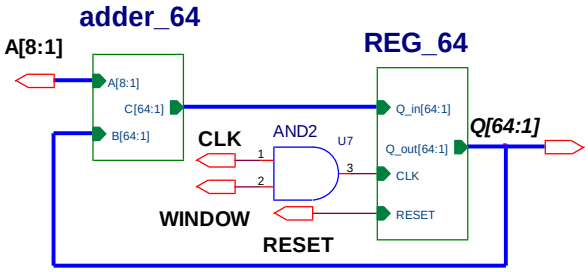

Fig 9: Schematic diagram of the TRC stage.

The TRC module has two main modules; 64-bit adder, and 64-bit register. The 64-bit adder is represented by module, ADDER_64, and the 64-bit register is represented by module REG_64. The adder accepts sample outputs of the ADC (A[8:1]) and outputs of the REG_64 (Q[64:1]), and produces the sum of them. After one clock shift (CLK, gated by control signal WINDOW, considered the test gate), the sum Q[64:1] is generated. The input clock of the 64-bit register, generated from CLK, is used to proper synchronization. The input data A[8:1] to the TRC is processed every clock cycle within the gate interval control signal WINDOW. Using suitable triggering edges of the CLK, the synchronization and processing operation are achieved. The test gate can be controlled and generated for proper operation of the signature generation. The input clock of the 64-bit register is the gated clock inside the test gate. The control signal RESET is the signal that clears the REG_64 in the beginning of each test gate WINDOW. The TRC generates a digital signature after the test gate WINDOW is closed shown in Figure 10, and the input clock of the 64-bit register stops running.

Figure 11 illustrates the full timing waveform cycle of the presented testing approach for both analogue signals and digital signals. The analogue signals are the ATPG output V(ATPG_OUT), the bipolar ACUT output V(BPF_OUT), and the rectified output from the rectifier circuit V(RECTIFIER_OUT). The digital signals are the RESET, S/H, CLK, and WINDOW. In addition, the digital buses are A[8:1], Q[32:1], and Q[64:33]. The accumulation process of the TRC module is triggered by the RESET signal to execute a number of iterations equals to the number of weighted samples. Figure 10 illustrates the timing of the digital signals that affect the TRC module in different time during the test cycle window. All control signals, presented in Figure 10 and Figure 11, are properly asserted in the start of the test gate, the middle of the test gate, and the end of the test gate to generate a digital signature.

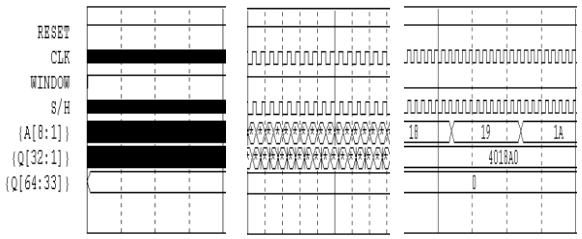

Fig 10: Timing diagram of the starting test gate, the middle test gate, and the closing test gate of the accumulation process.

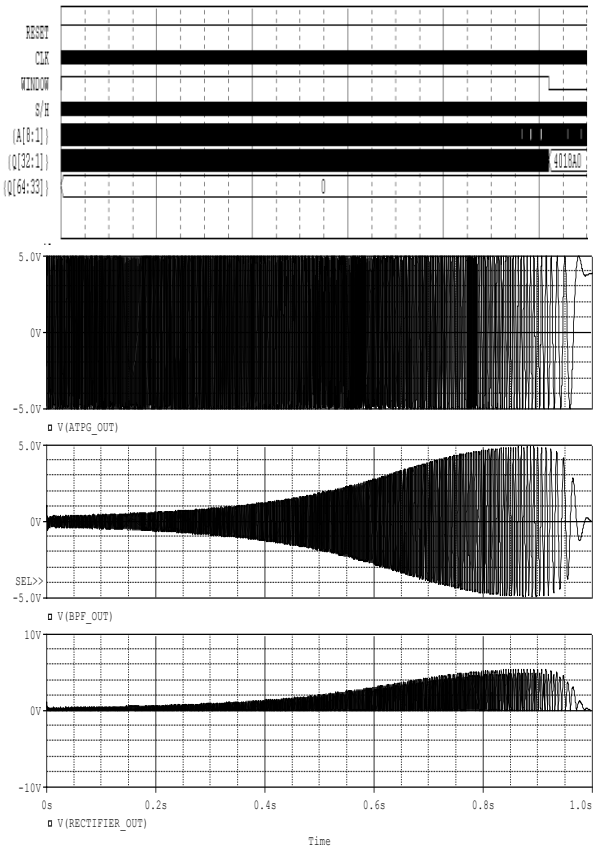

Fig 11: Full Timing diagram of the circuit model of the analogue testing.

3. PSPICE CIRCUIT MODEL SIMULATION OF THE ACUT

The modeling of ACUT transfer function is the main step to predict the output response of the ACUT. Analogue circuit differs by their characteristics and parameters that control its analogue response. These parameters have a great role in the process of predicting the fault-free output analogue response and accordingly improve the process of detecting different ACUT faults. The ACUT model selected from a group of standard analogue circuits called benchmark circuits [26]. Each benchmark circuit could be modeled through its transfer function in the frequency domain that requires a specified input sinusoidal signal swept in frequency.

The developed approach is verified and validated the decision for the ACUT in two major phases. The first phase is for a golden fault-free ACUT and the second phase is for predefined faults in the same ACUT. The presented testing approach determines an ACUT status in both cases based on the generated digital signature. The signature comparison is achieved based on the pre-calculated signature boundaries in the first phase. Signature boundaries are calculated from the analogue output response of the simulated ACUT model using the PSpice circuit simulator and based on the worst-case analysis of both the minimum and the maximum of the output analogue response of the ACUT. This boundary calculation considers the tolerances of ACUT components that affect the transfer function of the ACUT. If the calculated signature in the second phase lies within the pre-calculated signature boundaries, it judged as a fault-free ACUT, otherwise it judged as a faulty one. one of the benchmark circuits as an ACUT is selected. This circuit is the band pass filter (BPF) in the frequency range of the biomedical circuits.

The schematic diagram of the BPF is shown in Figure 12. By a simple analysis, it is clarified that its transfer function and its transfer function coefficients are as follow:

$$TF = \frac{ab}{s^5+s^4(a_2+b_1)+s^3(a_1+a_2b_1+b)+s^2(a+a_1b_1+b)+s(a_1+a_2b)+ab} \quad (4\text{-}1)$$

where,

$$a = \frac{1}{C_1C_2C_3R_1R_2R_3} \qquad b = \frac{1}{R_4R_5C_4C_5} \qquad b1 = \frac{1}{R_5C_4} + \frac{1}{R_4C_4}$$

$$a1 = \frac{1}{C_2C_3R_2R_3} + \frac{1}{C_1C_2R_2R_3} + \frac{1}{C_1C_2R_1R_3} + \frac{1}{C_1C_2R_1R_2}$$

$$a2 = \frac{1}{C_1R_1} + \frac{1}{C_1R_2} + \frac{1}{C_2R_3} + \frac{1}{C_2R_2}$$

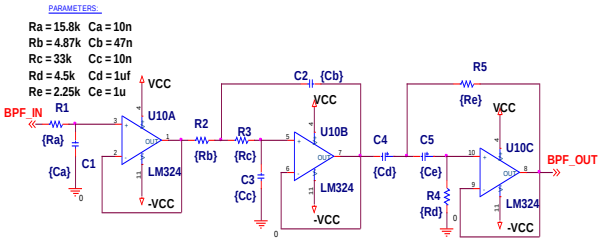

Fig 12: Schematic diagram of the BPF.

The worst-case analysis is used to find the worst-case probable output of an analogue circuit, given the circuit description, and the restricted parameter tolerances. It is the upper or lowest possible collating function relative to the nominal run. PSpice circuit simulator allows tolerances to be set on any number of the parameters that characterize a model. Models can be defined for nearly all primitive analogue circuit components (resistors, capacitors, semiconductor devices, etc). PSpice reads the standard model parameter tolerance, and uses the nominal, minimum, and maximum probable values. For instance, if the values of R1, R2, R3, R4, R5, C1, C2, C3, C4, and C5 in the case of BPF can vary by ±5%, ±10%, or ±20%, then the worst-case analysis will attempt to find the combination of possible resistor values and capacitor values which result in the worst simulated output. For the worst-case analysis, each component value is taken from its nominal as allowed by its tolerance, in the direction which should cause the collating function to be its worst (given by the upper or lowest specification).

A summary of that analysis is illustrated in Table 1 that shows the percent change corresponding to each component. For example, R1 equals 0.95 of nominal value for the lowest bound and equals 1.05 of nominal value for the upper bound. It indicates that resistor value decreases (D) by -5% for the lower bound, and increases (I) by +5% for the upper bound. In ±10% tolerance, R1 increases (D) by -10% for the lower bound, and decreases (I) by +10% for the upper bound. In addition, Table 2 illustrates the signature boundaries in hexadecimal format, and the nominal and worst-case component values based on the worst-case analysis. For example, SL equals 255758 for the lowest signature bound and SU equals 31BE12 for the upper signature bound according to the listed component values and ±10% component tolerance in Table 2. In ±5% component tolerance, SL equals 283038 and SU equals 2E4693. In this case study, the output signal frequency sweeps from 1.2 Hz to 1.5 kHz according to Figure 6.

Table 1. Component tolerances for the worst-case analysis of the BPF.

Comp	±5%		±10%		±20%	
	LOWEST	UPPER	LOWEST	UPPER	LOWEST	UPPER
R1	0.95 (D)	1.05 (I)	0.9 (D)	1.1 (I)	0.8 (D)	1.2 (I)
R2	1.05 (I)	0.95 (D)	1.1 (I)	0.9 (D)	1.2 (I)	0.8 (D)
R3	0.95 (D)	1.05 (I)	0.9 (D)	1.1 (I)	0.8 (D)	1.2 (I)
R4	1.05 (I)	0.95 (D)	1.1 (I)	0.9 (D)	1.2 (I)	0.8 (D)
R5	0.95 (D)	1.05 (I)	0.9 (D)	1.1 (I)	0.8 (D)	1.2 (I)
C1	0.95 (D)	1.05 (I)	0.9 (D)	1.1 (I)	0.8 (D)	1.2 (I)
C2	1.05 (I)	0.95 (D)	1.1 (I)	0.9 (D)	1.2 (I)	0.8 (D)
C3	0.95 (D)	1.05 (I)	0.9 (D)	1.1 (I)	0.8 (D)	1.2 (I)
C4	1.05 (I)	0.95 (D)	1.1 (I)	0.9 (D)	1.2 (I)	0.8 (D)
C5	1.05 (I)	0.95 (D)	1.1 (I)	0.9 (D)	1.2 (I)	0.8 (D)

Table 2. Signature boundaries for the worst-case analysis of the BPF.

Comp	Nominal	±5%		±10%		±20%	
		LOWEST	UPPER	LOWEST	UPPER	LOWEST	UPPER
R1 (Ω)	15.8k	16.56k	15.14k	17.38k	14.22k	18.96k	12.64k
R2 (Ω)	4.87k	4.6265k	5.1135k	4.383k	5.357k	3.896k	5.844k
R3 (Ω)	33k	34.65k	31.35k	36.3k	29.7k	39.6k	26.4k
R4 (Ω)	4.5k	4.275k	4.725k	4.05k	4.95k	3.6k	5.4k
R5 (Ω)	2.25k	2.3625k	2.1375k	2.475k	2.025k	2.7k	1.8k
C1 (F)	10n	10.5n	9.5n	11n	9n	12n	8n
C2 (F)	47n	44.65n	49.35n	42.3n	51.7n	37.6n	56.4n
C3 (F)	10n	10.5n	9.5n	11n	9n	12n	8n
C4 (F)	1uf	0.95u	1.05u	0.9u	1.1u	0.8u	1.2u
C5 (F)	1uf	0.95u	1.05u	0.9u	1.1u	0.8u	1.2u
	Digital Signatures						
	SN	SL	SU	SL	SU	SL	SU
	2B29CF	283038	2E4693	255758	31BE12	200BFD	3960E3

4. PARAMTERIC FAULT ANALYSIS OF THE BAND PASS FILTER USING SIGNATURE CURVE

In this section, the effect of the parametric fault of the component in the band pass filter, illustrated in Figure 12 is presented. The effects of all component variations in the ACUT with respect to the passband transmission (A_{max}) and the bandwidth (*BW*) are taken in the consideration. According to the nominal values of the resistors and the capacitors presented in Figure 12 and the AC Analysis of the PSpice circuit simulator, the value of the bandwidth (*BW*) equals 480 Hz, and the A_{max} equals 0.98305 V. This filter can be used in the extraction circuit of muscle potentials of EMG waveform to reject low signals besides the signals above 500 Hz.

Component variations in this paper will sweep from very small value (or short circuit (SC) in the case of impedances), ±10%, ±20%, ±50% …, until very large value (or open circuit (OC) in the case of impedances). Therefore, the effect of component variations on the BPF output response is achieved, and consequently the relation between the generated digital signatures with respect to component variations is required to be stated and analyzed. The derived curve is called the *signature curve*. The requirement of the signature curve combines the effect of the A_{max} and the *BW* in one curve that illustrates the ACUT status.

The analysis of the output response based on the amplitude response of the BPF is done using the PSpice circuit simulator (AC Analysis). The amplitude response of the BPF based on each resistor variation (*Ra*, *Rb*, *Rc*, *Rd*, *Re*) and each capacitor variation (*Ca*, *Cb*, *Cc*, *Cd*, *Ce*) is presented. The resistor variation is achieved from 1Ω (SC) to 10MΩ (OC), and the capacitor variation is achieve from 1 *pF* (very small value) to 1 *mF* (very large value). In Table 3 and Table 4, the *BW* values, the A_{max}, and the corresponding digital signatures with respect to each resistor variation and each capacitor variation is illustrated.

Table 3. Signatures, *BW*, and A_{max} for each resistor variations of the BPF.

Component values			*BW*	A_{max}	Sig. (Hex.)	Sig. (Dec.)
Ra (Ω)	1	short	544.750	0.996	313937	3225911
	10		544.750	0.996	31383E	3225662
	100		544.746	0.996	3137FE	3225598
	1000		544.398	0.996	312F1C	3223324
	7.9k	-50%	524.771	0.992	2F1F76	3088246
	10000		514.280	0.990	2E1F15	3022613
	12640	-20%	499.374	0.987	2CC916	2935062
	14220	-10%	489.847	0.985	2BF941	2881857
	15.01k	-5%	484.971	0.984	2B91C6	2855366
	15800	NOM	480.041	0.983	2B29CF	2828751
	16.59k	+5%	475.068	0.981	2AC3AD	2802605
	17380	+10%	470.129	0.980	2A5DE2	2776546
	18960	+20%	460.010	0.978	299524	2725156
	23.7k	+50%	429.996	0.971	275A39	2579001
	50000		292.888	0.926	1E5067	1986663
	1E+05		172.111	0.833	15BF58	1425240
	1E+06		71.617	0.214	6B4BB	439483
	1E+07	open	70.653	0.022	4A28A	303754
Rb (Ω)	1	short	397.099	0.948	2BCACE	2869966
	10		397.390	0.948	2BCFD1	2871249
	100		400.307	0.949	2BFEBB	2883259
	1000		430.060	0.954	2D5852	2971730
	2435	-50%	470.519	0.963	2D7B26	2980646
	3896	-20%	485.216	0.974	2C3A6E	2898542
	4383	-10%	483.797	0.978	2BB432	2864178
	4626.5	-5%	482.176	0.980	2B7070	2846832
	4870	NOM	480.041	0.983	2B29CF	2828751
	5113.5	+5%	477.455	0.985	2AE414	2810900
	5357	+10%	474.476	0.987	2A9D56	2792790
	5844	+20%	467.536	0.993	2A1116	2756886
	7305	+50%	441.650	1.013	28781F	2652191
	10000		391.138	1.059	25D1AE	2478510
	50000		154.850	1.179	156A95	1403541
	1E+05		100.820	1.050	F62C1	1008321
	1E+06		54.927	0.417	5CDDB	380379
	1E+07	open	56.709	0.214	49CC9	302281
Rc (Ω)	1	short	911.197	0.980	43583E	4413502
	10		912.116	0.980	435E92	4415124
	100		921.465	0.981	439FAF	4431791
	1000		1034.256	0.982	462CDD	4599005
	10000		998.997	0.996	450981	4524417
	16500	-50%	764.593	1.002	3AD089	3854473
	26400	-20%	565.812	0.992	301BCD	3152845
	29700	-10%	524.953	0.988	2D7967	2980199
	31.350	-5%	499.177	0.985	2C48B5	2902197
	33000	NOM	480.041	0.983	2B29CF	2828751
	34650	+5%	462.186	0.980	2A1CC3	2759875
	36300	+10%	445.493	0.978	291EE4	2694884
	39600	+20%	415.183	0.972	274C68	2575464
	50000	+50%	340.436	0.955	22A7E1	2271201
	66000	-50%	265.333	0.927	1DA0F1	1941745
	1E+05		182.619	0.863	172FF7	1519607
	1E+06		70.395	0.217	6A2AC	434860
	1E+07	open	69.553	0.022	4A0E8	4413502
Rd (Ω)	1	short	625.467	0.001	48D8C	298380
	10		625.294	0.011	49CDE	302302
	100		609.807	0.115	9E104	647428
	1000		475.219	0.702	21149D	2167965
	2250	-50%	476.635	0.891	27C3BB	2606011
	3600	-20%	481.081	0.957	2A97A2	2791330
	4050	-10%	480.997	0.970	2AC1E4	2802148
	4275	-5%	480.640	0.977	2AF85F	2816095
	4500	NOM	480.041	0.983	2B29CF	2828751
	4725	+5%	479.159	0.989	2B587F	2840703
	4950	+10%	477.943	0.995	2BC624	2868772
	5400	+20%	474.340	1.008	2C0C19	2886681
	9000	+50%	407.857	1.151	2D252B	2958635
	10000		383.089	1.194	2D5888	2971784
	50000		8.302	2.400	2E181D	3020829
	1E+05		3.615	3.344	2DBF30	2998064
	1E+06		0.345	9.826	2EE8FA	3074298
	1E+07	open	0.055	19.250	318DDA	3247578

Component values			*BW*	A_{max}	Sig. (Hex.)	Sig. (Dec.)
Re (Ω)	1	short	99.858	0.549	306FC9	3174345
	10		71.583	4.332	306FC9	3174345
	100		77.590	3.248	371D36	3611958
	1000		357.516	1.196	2C734D	2913101
	1125	-50%	385.893	1.148	2C37F0	2897904
	1800	-20%	463.351	1.013	2B7478	2847864
	2025	-10%	473.639	0.994	2B4BFD	2837501
	2137.5	-5%	477.208	0.988	2B3A52	2832978
	2250	NOM	480.041	0.983	2B29CF	2828751
	2362.5	+5%	482.320	0.978	2B1B02	2824962
	2475	+10%	484.184	0.975	2B0D0A	2821386
	2700	+20%	487.022	0.969	2AF409	2814985
	4500	+50%	494.223	0.949	2A7943	2783555
	10000		494.727	0.936	2A0F92	2756498
	50000		493.471	0.928	29ABAA	2730922
	1E+05		493.270	0.927	299D47	2727239
	1E+06		493.104	0.926	298D43	2723139
	1E+07	open	493.083	0.926	298AFE	2722558

***Discussion and comments*:** Figure 13 and Figure 14 illustrate the signatures with respect to *Ra*, *Rb*, *Rc*, *Rd*, and *Re* variations, called the *signature curve of Ra*, *Rb*, *Rc*, *Rd*, and *Re*. In addition, Figure 15 and Figure 16 illustrate the signatures with respect to *Ca*, *Cb*, *Cc*, *Cd*, and *Ce* variations, called the *signature curve of Ca*, *Cb*, *Cc*, *Cd*, and *Ce*. During *Ra*, *Rb*, and *Rc* variations, the variation of A_{max} is nearly unity gain. The signature curves of *Ra*, *Rb*, and *Rc*, illustrated in Figure 13, clearly have the same corresponding variations of *BW*, illustrated in Table 3**.** In these cases, the signature curves are affected with the *BW*, while it is not affected with the A_{max}.

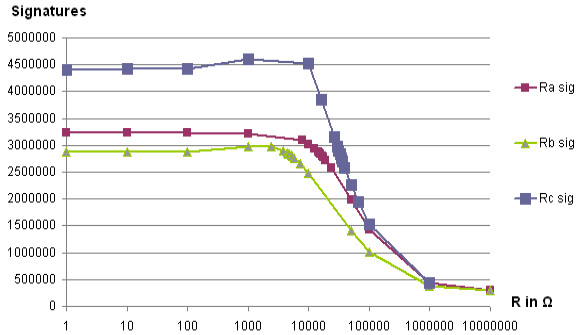

Fig 13: Signature curves of resistors *Ra*, *Rb*, and *Rc* in BPF.

During *Rd* variation, the signature curve is affected with both the variation of the *BW* and the variation of the A_{max}. During *Rd* variation from 1Ω to 100Ω, the variation of A_{max} is low with very low gain below 0.115 V/V, and in the same time the variation of *BW* is nearly constant with maximum *BW*. Therefore, the signatures illustrated in Figure 14 have small values due to low gain of the BPF that makes low values of output samples. During *Rd* variation from 100Ω to 10kΩ, the variation of A_{max} is increasing, and in the same time the variation of *BW* is slowly decreasing. Therefore, the signature variation, illustrated in Figure 14, is increasing. During *Rd* variation from 1kΩ to 1MΩ, the variation of A_{max} is increasing, and in the same time the variation of *BW* is largely decreasing. Therefore, the signature variation, illustrated in Figure 14, is nearly constant according to the signature curve. During *Rd* variation from 1MΩ to 10MΩ, the variation of A_{max} is largely increasing, and in the same time the variation of *BW* is also largely decreasing. The signature variation, illustrated in Figure 14, is slowly increasing in the signature curve.

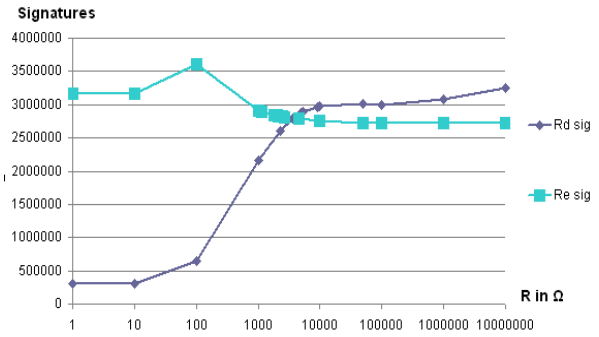

Fig 14: Signature curves of resistors *Rd*, and *Re* in BPF.

During *Re* variation, the signature curve is affected with both the variation of the *BW* and the variation of the A_{max}. During *Re* variation from 1Ω to 10Ω, the variation of A_{max} is largely increasing, and in the same time the variation of *BW* is slowly decreasing with the minimum *BW*. Therefore, the signature variation, illustrated in Figure 14, is nearly constant. During *Re* variation from 10Ω to 100Ω, the variation of A_{max} is decreasing, and in the same time the variation of *BW* is slowly increasing. Therefore, the signature variation, illustrated in Figure 14, is slowly increasing. During *Re* variation from 100Ω to -20% of the nominal value (*Re* = 2.25kΩ), the variation of A_{max} is decreasing, and in the same time the variation of *BW* is largely increasing. Therefore, the signature variation, illustrated in Figure 14, is slowly decreasing. During *Re* variation from -20% of the nominal value (*Re* = 2.25kΩ) to 10MΩ, the variation of A_{max} is nearly constant with unity gain, and in the same time the variation of *BW* is nearly constant with the maximum value of *BW*. Therefore, the signature variation, illustrated in Figure 14, is nearly constant.

Table 4. Signatures, *BW*, and A_{max} for each capacitor variations of the BPF.

Component values			*BW*	A_{max}	Sig. (Hex.)	Sig. (Dec.)
Ca (pF)	1	open	544.750	0.996	313941	3225921
	10		544.749	0.996	31394E	3225934
	100		544.741	0.996	31387E	3225726
	1000		543.875	0.996	312050	3219536
	5000	-50%	524.770	0.992	2F1F52	3088210
	8000	-20%	499.374	0.987	2CC900	2935040
	9000	-10%	489.847	0.985	2BF923	2881827
	9500	-5%	484.971	0.984	2B91BC	2855356
	10000	NOM	480.041	0.983	2B29CF	2828751
	10500	+5%	475.068	0.981	2AC3A9	2802601
	11000	+10%	470.065	0.980	2A5DF3	2776563
	12000	+20%	460.010	0.978	299553	2725203
	15000	+50%	429.996	0.971	275A61	2579041
	1E+05		123.866	0.732	10F11A	1110298
	1E+06		72.5738	0.265	5D16A	381290
	5E+07		70.8697	0.139	491CD	299469
	1E+08		70.6536	0.001	491CD	299469
	1E+09	short	70.653	0.0001	491CD	299469
Cb (pF)	1	open	358.661	0.940	293424	2700324
	10		358.688	0.940	2934BC	2700476
	100		358.961	0.940	2939C9	2701769
	1000		361.708	0.941	2968ED	2713837
	10000		391.138	0.947	2AF234	2814516
	23500	-50%	437.646	0.958	2BE320	2876192
	37600	-20%	472.299	0.972	2BA39B	2859931
	42300	-10%	477.734	0.977	2B6B09	2845449
	45825	-5%	479.742	0.981	2B3B3F	2833215
	47000	NOM	480.041	0.983	2B29CF	2828751
	48175	+5%	480.162	0.984	2B1965	2824549
	51700	+10%	479.509	0.989	2AE31E	2810654
	56400	+20%	476.409	0.998	2A983E	2791486
	94000	+50%	405.909	1.127	283585	2635141
	1E+05		393.520	1.152	27DA7E	2611838

Component values			*BW*	A_{max}	Sig. (Hex.)	Sig. (Dec.)
	1E+06		38.047	3.298	16EB52	1502034
	5E+07		0.914	2.424	53357	340823
	1E+08		0.539	1.461	4D00D	315405
	1E+09	short	0.202	0.123	491D0	299472
Cc (pF)	1	open	400.216	1.277	45657D	4547965
	10		702.234	1.429	4585E6	4556262
	100		396.392	1.286	46D83D	4642877
	1000		1950.75	1.198	580198	5767576
	5000	-50%	811.094	1.037	3E48B9	4081849
	8000	-20%	580.018	0.996	30DFF3	3203059
	9000	-10%	26.039	0.989	2DCCA2	3001506
	9500	-5%	502.142	0.986	2C6EDF	2911967
	10000	NOM	480.041	0.983	2B29CF	2828751
	10500	+5%	459.562	0.979	29FB70	2751344
	11000	+10%	440.553	0.976	28E084	2678917
	12000	+20%	406.419	0.970	26DD62	2547042
	15000	+50%	327.958	0.950	220FB9	2232249
	1E+05		81.52	0.486	A9FF1	696305
	1E+06		69.787	0.059	4EF8E	323470
	5E+07		69.712	0.001	491D0	299472
	1E+08		69.716	0.0006	491D0	299472
	1E+09	short	69.715	5.914E-5	491D0	299472
Cd (pF)	1	open	623.610	1E-5	491D0	299472
	10		623.610	0.0001	491D0	299472
	100		623.606	0.001	491D0	299472
	1000		623.445	0.01	490F5	299253
	100000		469.990	0.956	1F7930	2062640
	500000	-50%	476.293	0.978	29C313	2736915
	800000	-20%	478.205	0.981	2AD6D0	2807504
	900000	-10%	479.133	0.982	2B05C7	2819527
	950000	-5%	480.041	0.983	2B1910	2824464
	1E+06	NOM	80.928	0.983	2B29CF	2828751
	1050000	+5%	481.794	0.984	2B38F0	2832624
	11E+05	+10%	483.457	0.984	2B4737	2836279
	12E+05	+20%	487.855	0.983	2B5CF0	2841840
	15E+05	+50%	70.954	0.664	2B890D	2853133
	5E+07		469.990	0.956	2B5A3B	2841147
	1E+08		480.041	0.983	2B4F38	2838328
	1E+09	short	504.723	0.966	2B4748	2836296
Ce (pF)	1	open	623.626	1.85E-05	491D0	299472
	10		623.605	0.0001	491D0	299472
	100		623.603	0.001	491D0	299472
	1000		623.458	0.01	490F5	299253
	1E+05		470.943	0.665	1F7930	2062640
	5E+05	-50%	469.978	0.956	29C313	2736915
	8E+05	-20%	476.289	0.979	2AD6D0	2807504
	9E+05	-10%	478.203	0.981	2B05C7	2819527
	95E+04	-5%	479.132	0.982	2B1910	2824464
	1E+06	NOM	480.041	0.983	2B29CF	2828751
	1050000	+5%	480.929	0.984	2B38F0	2832624
	11E+05	+10%	481.796	0.984	2B4737	2836279
	12E+05	+20%	483.461	0.984	2B5CF0	2841840
	15E+05	+50%	487.861	0.984	2B890D	2853133
	5E+07		480.041	0.983	2B5A3B	2841147
	1E+08		504.715	0.966	2B4F38	2838328
	1E+09	short	504.601	0.965	2B4748	2836296

Discussion and comments: During *Ca* variation, the variation of A_{max} is nearly unity gain from 1 *pF* to 1 μF, and is decreasing from 1 μF to 1 *mF*. The signature variation of *Ca* clearly has the same corresponding variation of *BW***.** In this case, the signature curve, illustrated in Figure 15, is affected with the *BW*.

During *Cb* variation, the variation of A_{max} is nearly unity gain from 1 *pF* to 0.1 μF, is increasing from 0.1 μF to 1 μF, and is decreasing from 1 μF to 1 *mF*. The signature variation of *Cb* clearly has the same corresponding variation of *BW***.** In this case, the signature curve, illustrated in Figure 15, is affected with the *BW*. Large values of A_{max} during *Cb* variation from 0.1 μF to 1 *mF* cannot affect the signature values due to very low *BW* values.

During *Cc* variation, the variation of A_{max} is nearly unity gain from 1 *pF* to 15 *nF*, and is decreasing from 15 *nF* to 1 μF. In addition, the variation of A_{max} is very low gain from 1 μF to 1 *mF***.** In this case and during *Cc* variation, the signature curve is affected with both the variation of the *BW* and the variation of the A_{max}. During *Cc* variation from 1 *pF* and 1 *nF*, the variation of A_{max} is nearly unity gain, and in the same time small irregular variation of *BW* during *Cc* variation from 1 *pF* and 100 *pF*, and increasing variation of *BW* during *Cc* variation from 100 *pF* and 1 *nF*. Therefore, the signature variation is constant from 1 *pF* and 100 *pF*, and is increasing from 100 *pF* and 1 *nF*, illustrated in Figure 15. During *Cc* variation from 1 *nF* to 1 μF, the variation of A_{max} is slowly decreasing, and in the same time the variation of *BW* is largely decreasing. Therefore, the signature variation, illustrated in Figure 15, has the same corresponding variation of *BW*. During *Cc* variation from 1 μF and 1 *mF*, the variation of A_{max} is low with very low gain, and in the same time the variation of *BW* is constant with low values of *BW*. Therefore, the signature variation, illustrated in Figure 15, is nearly constant with the low signature values in the signature curve.

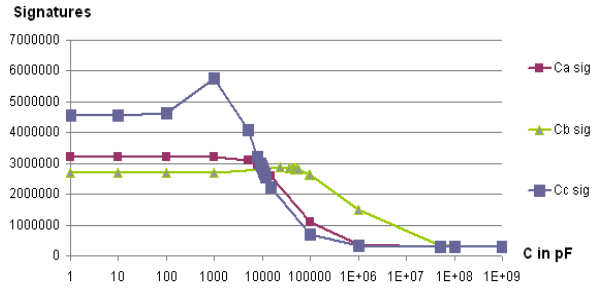

Fig 15: Signature curves of capacitors *Ca*, *Cb*, and *Cc* in BPF.

During *Cd* variation and *Ce* variation, the variation of *BW* is nearly fluctuating above and below the nominal *BW*. The signature variations of *Cd* and *Ce* clearly have the same corresponding variation of A_{max}**.** In this case, both coincident signature curves, illustrated in Figure 16, are affected with the A_{max}.

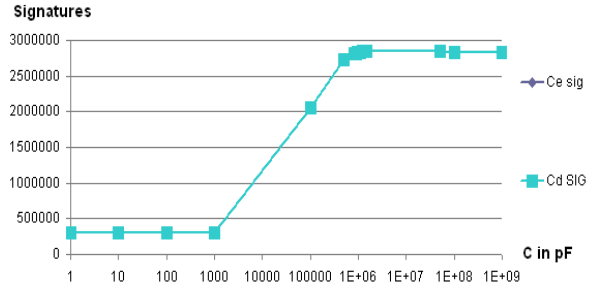

Fig 16: Signature curves of capacitors *Cd*, and *Ce* in BPF.

In general, the signature curve is affected with the *BW*, while it is not affected by the A_{max} due to its constant variation. When the *BW* has large values, the number of generated samples and their accumulation are large values. Therefore, the signature curve will be affected by the *BW*. In the other cases, the signature curve is affected with the A_{max}, while it is not affected by the *BW* due to its constant variation. When the A_{max} has large values, the number of generated samples and their accumulation are large values. Therefore, the signature curve will be affected by the A_{max}. In the other cases, the signature curve is affected with the *BW*, and the A_{max}. In this case, the large values of *BW* and small values of the A_{max} due to the attenuation of the transfer function of the ACUT. Therefore, the digital accumulated signatures in the signature curve have small values due to the small values of the output

samples. In addition, small values of the *BW* and the constant variation of the A_{max} produce small values of the digital accumulated signatures in the signature curve due to small values of the output samples.

5. CONCLUSION

This paper presented the new testing approach of analogue circuits for detecting parametric faults based on the simulation environment. The proper ATPG that matches the frequency domain of the ACUT and the ATRC that generates a digital signature are achieved. The ATPG generates the required stimulation for the ACUT in the frequency sweep manner. Control signals are used to synchronize the ATPG and ATRC for digital signature generation based on accumulation weighting sums of the sample magnitude of the analogue output response. Component tolerances of the ACUT affect the transfer function of the ACUT. Therefore, the signature comparison is achieved based on signature boundaries, calculated from the worst-case analysis in PSpice circuit simulator for the ACUT judgment. In this paper, the presented testing approach enables the concept of the signature curve of each component of the ACUT. Based on this curve, the relation between digital signatures and component variations of the ACUT combines the effects of the bandwidth (BW) and the passband transmission (Amax) on the output response of the ACUT during component variations. In some cases, the signature curve is affected with the bandwidth only during the constant variation of Amax. In some other cases, the signature curve is affected with the Amax only during the constant variation of bandwidth. In other cases, the signature curve is affected with both the bandwidth and the Amax.

The presented testing approach is applied to a benchmark analogue circuit. The signature curves for that ACUT were determined. The proper decision is taken when the input signal has the frequency sweep manner contrary to the previously published work that states that the suitable input signal type for the ACUT was the pulse waveform. In the future work, the development of a low-cost ATE for testing of analogue circuits is highly required.

6. REFERENCES

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