Design of High Speed Full Adder using Improved Differential Split Logic Technique for 130nm Technology and its Implementation in making ALU

Gurleen Kaur
Mtech Microelectronics
UIET, Panjab University
Chandigarh, UT India

Arvind Kumar
Assistant Professor, ECE
UIET, Panjab University
Chandigarh, UT India

Jatinder Singh
Assistant Professor, ECE
UIET,Panjab University
Chandigarh,UT India

ABSTRACT
Adders are the main components in digital designs which are used not only for addition but can be used for multiplication and division too. Adders find use in very large scale integrated circuits from processors (like in arithmetic logic circuits) to application specific integrated circuits. At the same time, high speed computation has become the important part of any digital applications today though low power is a key factor too. In this paper, a high speed full adder using improved differential split logic (DSL) technique is used. We further implement it in 1bit arithmetic logic circuit (ALU). Measurements show that proposed full adder is better than DSL full adder in terms of speed, and further implementation of it in ALU shows that it is better than CMOS ALU in terms of speed, power and power delay product (PDP).

General Terms
Full adder, Differential split level logic (DSL), Differential cascade voltage logic (DCVS), Arithmetic logic circuit (ALU), Power delay product (PDP), Full adder (FA), Multiplexer (Mux).

Keywords
Differential Split logic, Full adder, Arithmetic logic circuits

1. INTRODUCTION
Full adders are the heart of all arithmetic calculations [13]. It is a combinational logic unit that performs all the calculations like addition, subtraction, increment and decrement. There are certain factors that can simply slow down the development of small complex IC chips. These factors are design cost, design productivity and IC fabrication technology. The increasing demand for high speed very large scale integration can be obtained at design levels such as architectural, circuit and layout level .For the circuit design, at this level a proper choice of logic design style for high speed combinational logic circuits should be done. It is because all the important parameters affecting speed are switching capacitance, transition activity and short circuit currents are actually influenced by the chosen logic style. Earlier the parameters like power dissipation, small area and cost factor were given more weight age , but now days speed considerations are also the important factors for the scientific community related to VLSI designs.

In CMOS technology, even if we design high speed full adder, power dissipation is also taken care of. Power dissipation is one of the critical factors which is of two types and is classified into dynamic power and static power. Dynamic power dissipation comes into picture when the circuit is operational and static power dissipation is considered when the circuit is inactive.

Dynamic power is further classified into switching power ($P_{switch)}$ and short circuit power (P_{sc}).Static power is because of leakage power dissipation [7].

There are three major sources of power dissipation which are given in the following equation.

$$P_{total} = \alpha.C_l.V_{dd}^{\ 2}.f_{clk} + I_{sc}.V_{dd} + I_{leakage}.V_{dd}$$

The first term shows the switching component of power where α is the switching factor, C_l is the loading capacitance, f_{clk} is the clock frequency. The second term represents the dissipation due to short circuit currents. The last term is the dissipation due to leakage currents ($I_{leakage}$)[1].

The switching power dissipation in CMOS digital integrated circuits is an important function of the power supply voltage V_{dd} Reduction of power supply voltage is an important way to limit the power dissipation. But then limiting the power dissipation, results in increased circuit delay. The given equation tells about the dependence of delay on power supply voltage:

$$T_d \propto C_l V_{dd} k(V_{dd} - V_{th})^{\alpha}$$

Where k = transistor aspect ratio (W/L),V_{th}= transistor threshold voltage, α = velocity saturation index which varies between 1 and 2.

On decreasing the power supply voltage, power dissipation though is reduced, but instead the delay increases as the threshold voltage reaches near the supply voltage. This problem is overcome by using the low power differential split logic technique.

Section II gives a brief introduction of conventional full adder and the various logic styles that can be used to make full adders. Section III describes about the propagation delay analysis in DCVS and DSL circuits.

Section IV describes about the proposed DSL full adder and its implementation using the Tanner v 13.0 tool.

Section V further discusses about the implementation of these adders in designing arithmetic logic circuit.

Section VI tells about the conclusion.

2. LOGIC DESIGN STYLES

2.1 Conventional CMOS

The schematic diagram of a conventional CMOS adder is shown in the given figure:

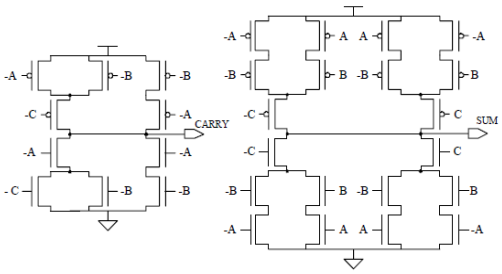

Fig 1: CMOS full adder [2]

Signals noted with '-'are basically complementary signals. The width of the transistors is increased to obtain a reasonable conducting current to drive the capacitive loads which further results in increased capacitance and high propagation delay.

2.2 Complementary pass transistor logic

The schematic diagram of CPL adder is shown in the diagram.

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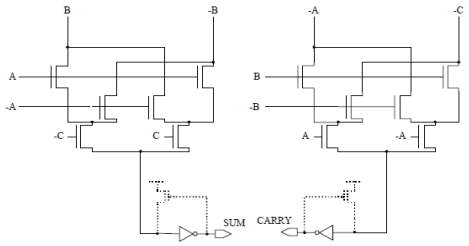

Fig 2: CPL full adder [2]

In CPL, the logic functions are implemented by the use of only an NMOS. This basically results in low input capacitance and high speed operation.CPL circuits consume less power than conventional static logic circuits because the logic output voltage swing of the pass transistor is less than the supply voltage level.

2.3 Differential cascode voltage switch logic (DCVSL)

DCVS have reduced transistor counts over NAND/NOR implementations. DCVS has got better performance of about 4times as compared to the CMOS/NMOS NAND/NOR circuits and maintaining the low power circuitry. The schematic diagram of the full adder is shown

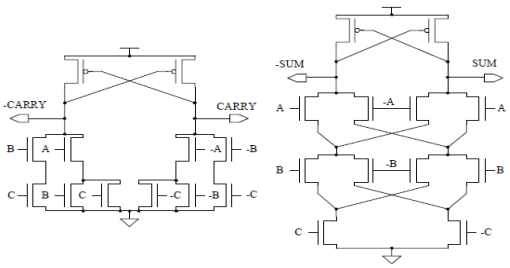

Fig 3: DCVS full adder [2]

Two complementary NMOS transistors set of switching trees are designed to connect to a couple of cross coupled PMOS transistors. One of the outputs is pulled down by NMOS network depending on the differential inputs. The input capacitance is two or three times smaller than that of conventional CMOS adder because the inputs drive only the NMOS transistors.

2.4 Differential split level logic (DSL)

Two NMOS transistors with their gates connected to the reference voltage are added to reduce the logic swing at the output nodes.

$$V_{ref} = (V_{dd} / 2) + V_{th}$$

Where V_{th} = NMOS threshold voltage.

So the output nodes are clamped at the half power supply voltage, hence the operation of the circuit becomes faster than the DCVSL operation. But these circuits dissipate high static power dissipation due to the incomplete turn off of the cross coupled circuits. Addition of two more NMOS transistors results in the increase of area. The circuit diagram of DSL full adder is shown.

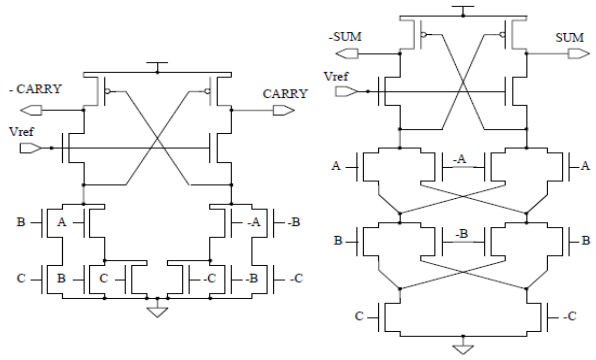

Fig 4: DSL full adder [2]

3. DELAY IN DSL

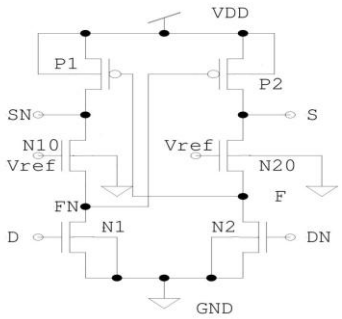

Fig 5: Basic DSL circuit

The propagation delay of a logic gate is defined as the difference between an input and output change [5]. The delay t_d is very well shown as the time difference between V_I and $V_{Q,}$ so that it goes through $0.5V_{dd}$. The input/output waveforms of half DSL logic circuit is shown here in figure 6 [3].

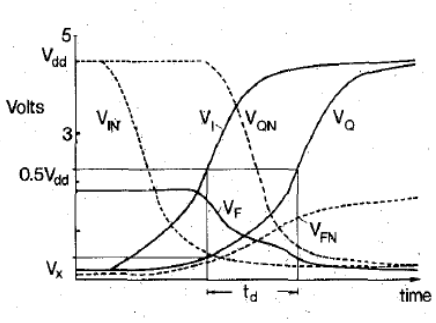

Fig 6: Input /output waveforms of half DSL circuit

The given figure of half DSL logic circuit is considered for the delay analysis.

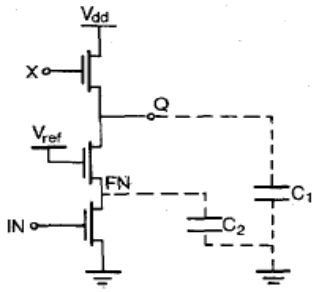

Fig 7: Half DSL circuit

Voltage change at Q is $(0.5V_{dd}-V_x)$. Hence, if C_1 is the capacitance at Q and $I_{C1,}$ the current which charges it during the propagation delay then t_d can be expressed as:

$$T_d = C_l(0.5V_{dd} - V_x) / I_{c1}$$

Moreover t_d can be expressed in term of the current of I_{pmos} which flows through P_2 during the propagation delay, which not only charges the capacitance at C_1 but also charges the capacitance at node F_n. Referring to the capacitance C_2, voltage change across it during the propagation delay t_d is $V_{fn.}$ Considering the I_{pmos}, t_d is expressed as follows :

$$T_d = (C_l(0.5V_{dd} - V_x) + C_2(V_{fn})) / I_{pmos}$$

Where $V_{fn} = K(V_{ref} - V_{tn2})$

$$K = A + B(C_2 / C_1)$$

$$I_{pmos} = (W_n / L_n)A(\beta / 2)(V_{dd} - B(V_{ref} - V_{tn}) - V_{tp})^2$$

4. IMPLEMENTATION OF PROPOSED FULL ADDER

In this modified DSL full adder is proposed. Two resistors are added in series to the reference NMOS N10 and N20 transistors in the DSL circuit in figure 5which will switch on the PMOS transistors more quickly .This helps in decreasing the delay in the full adder. The worst case delay is considered for the measurements. The transistor W/L ratio is 1.66.Tanner v13.0 too is used with the 130nm technology file. The schematic diagram of the proposed full adder is shown.

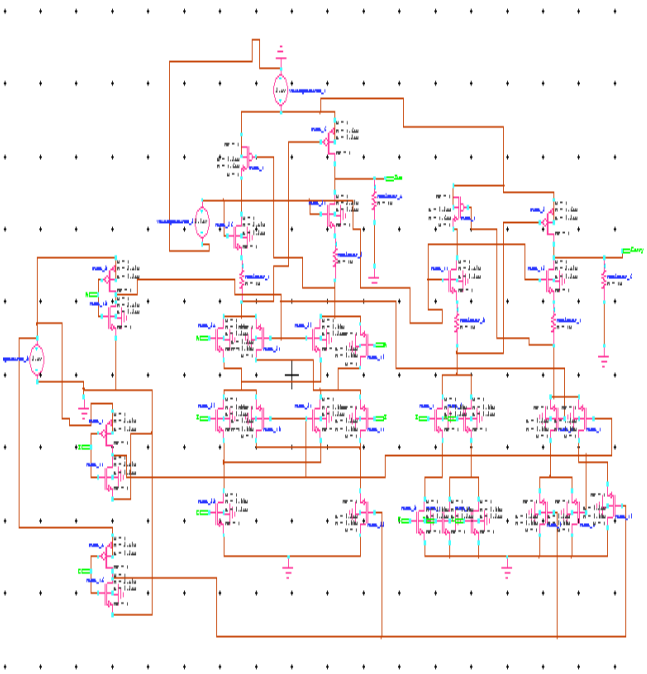

Fig 8: Proposed DSL full adder

The above proposed full adder is further modified by putting capacitor in parallel with the resistors that are added in series to the reference transistors in figure 9.

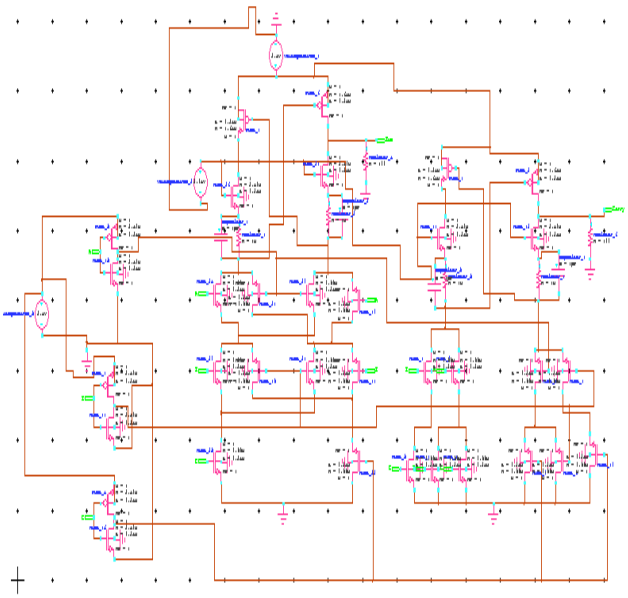

Fig 9: Proposed DSL full adder with capacitance

4.1 Simulation Results

The table showing simulation results with proposed full adder starting from resistor R=0 and with increasing resistances is shown. The power voltage source is 2.5V and the reference voltage is 2.05V.

Table 1.Delay (10^{-10}ns) calculations wrt increasing resistance (ohms)

Resistance	Delay(C=0 pF)	Delay(C=0.0001pF)	Delay(C=0.001pF)
0	1.4846	1.4846	1.4846
100	1.4577	1.4577	1.4577
200	1.4341	1.4341	1.4343
300	1.4220	1.4220	1.4224
400	1.4104	1.4104	1.4109
500	1.3977	1.3978	1.3986
1000	1.3449	1.3452	1.3481
1100	1.3306	1.3309	1.3343
1200	1.3224	1.3231	1.3285
1300	1.3170	1.3177	1.3181
1400	1.3149	1.3108	1.3179
1500	1.3156	1.3164	1.3202
1600	1.3182	1.3191	1.3241
1700	1.3099	1.3111	1.3218
1800	1.3034	1.3046	1.3160
1900	1.2993	1.3007	1.3127

Table 2.Power consumption (µw) calculations wrt increasing resistance (ohms)

Resistance	Power(C=0 pF)	Power(C=0.0001pF)	Power(C=0.001pF)
0	7.977327	7.977327	7.977327
100	8.59742	8.597420	8.597418
200	9.220806	9.220805	9.220798
300	9.845852	9.84585	9.845835
400	10.471105	10.471102	10.471104
500	11.095287	11.095282	11.095239
1000	14.16555	14.165531	14.165364
1100	14.764302	14.76428	14.764161
1200	15.356704	15.356677	15.356677
1300	15.942382	15.942351	15.356442
1400	16.521041	16.521006	16.520694
1500	17.092466	17.092426	17.092072
1600	17.656211	17.656167	17.655773
1700	18.212428	18.212379	18.211942
1800	18.760887	18.760833	18.760351
1900	19.575752	19.575789	19.576158

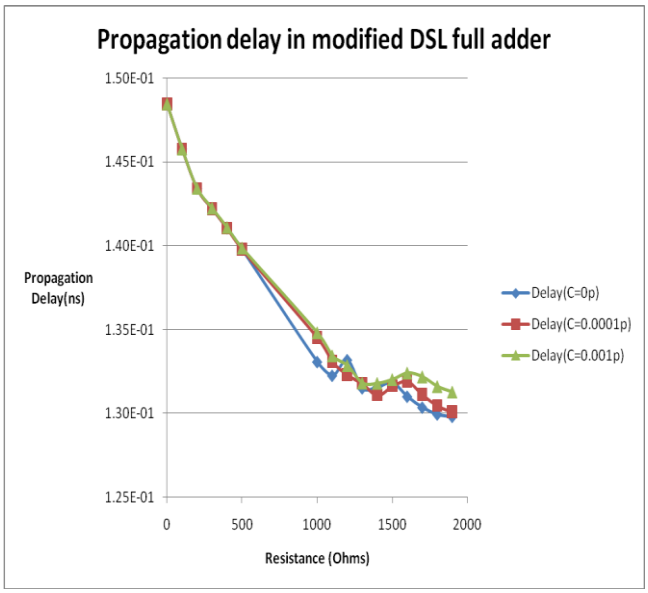

Fig 10: Graph for propagation delay with increasing resistance

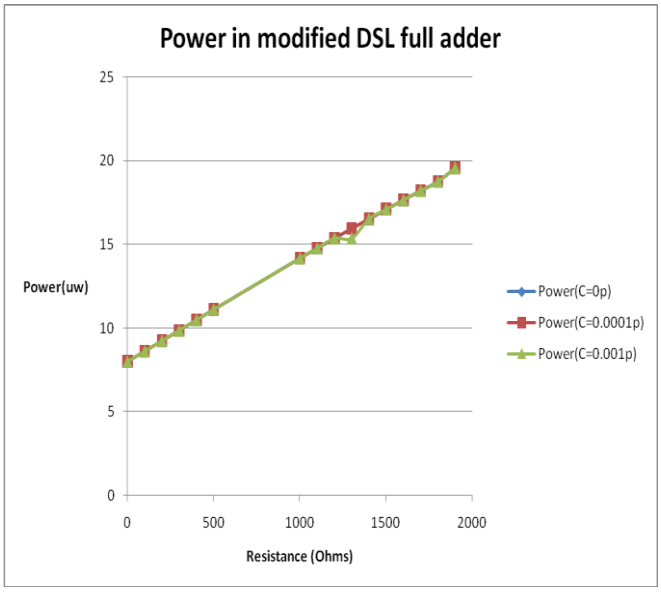

Fig 11: Graph for power consumption with increasing resistance

Table 3.PDP (µw ns) calculations wrt increasing resistance (ohms)

Resistance	PDP(C=0pF)	PDP(C=0.0001 pF)	PDP(C=0.001 pF)
0	1.184313966	1.184313966	1.184313966
100	1.253245913	1.253245913	1.253245622
200	1.322355788	1.322355645	1.322539057
300	1.400080151 4	1.40007987	1.40047157
400	1.476844649	1.476844226	1.477368063
500	1.550788264	1.550898518	1.551780127
1000	1.90512482	1.90554723	1.909632721
1100	1.964538024	1.964978025	1.969982002
1200	2.030770537	2.031841008	2.040134539
1300	2.099611709	2.100723591	2.02413262
1400	2.172351681	2.165573466	2.177262262
1500	2.248684827	2.250046959	2.256495345
1600	2.327441734	2.329024989	2.337800903
1700	2.385645944	2.387825011	2.407254494
1800	2.445294012	2.447538273	2.468862192
1900	2.543477457	2.546222875	2.569762261

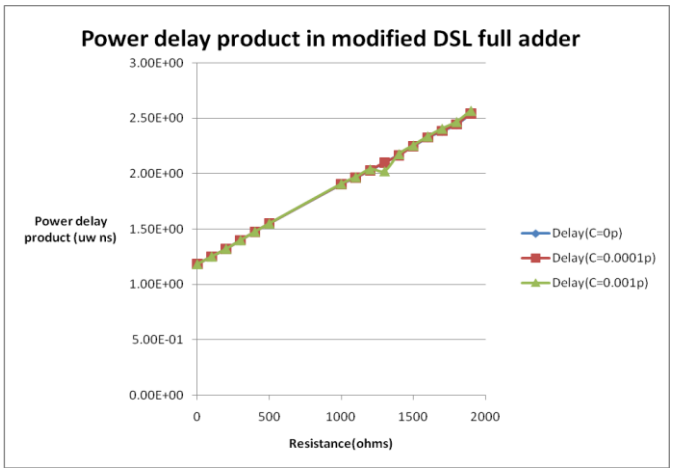

Fig 12: Graph for PDP with increasing resistance

4.2 Comparison results of proposed FA

The performance parameters of proposed full adder are compared to the ones given in the paper [10].

Table4. Comparison of performance parameters of FA

Logic circuits	Delay(ns)	Power(µw)	PDP(µw ns)
Proposed FA	0.12	19.57	2.569762261
DSL FA	0.148	7.977327	1.184313966
CMOS FA	0.12	73.8	8.856
CPL FA	0.11	39.1	4.301
DCVSL FA	0.13	110.7	14.391
P-CPL FA	0.18	21.3	3.834
P-DCVSL FA	0.2	103	20.06

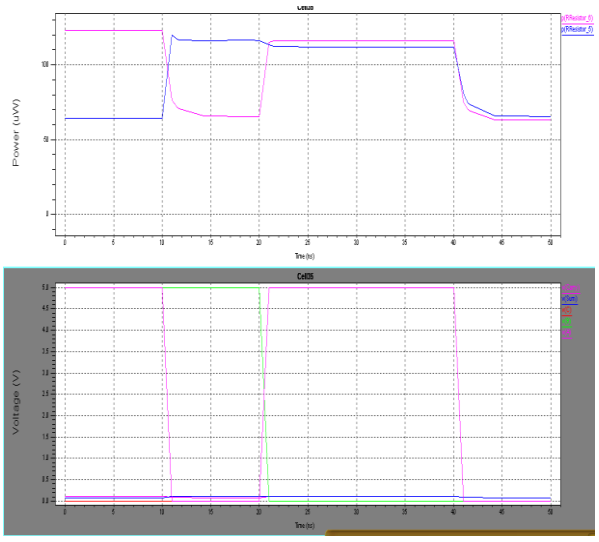

Fig 13: Simulation waveforms of FA (modified) in W-edit

5. DESIGN OF ALU USING PROPOSED FULL ADDER

Arithmetic logic unit is designed using the proposed full adder for arithmetic unit. This adder is used for addition, subtraction, increment and decrement by controlling the data inputs to implement these operations [9].Moreover for logic unit AND, OR, XOR and inverter is designed using modified DSL logic which is used in full adders too [11]. For designing ALU, two 4:1 mux and one 2:1 mux are designed using DSL logic [12]. So eight operations are performed by using this ALU shown in table 5.

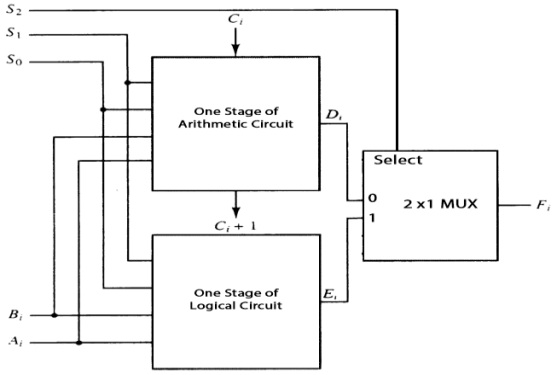

Fig 14: Structure of ALU

Table5. Truth table for ALU

S	S1	S2	Function
0	0	0	Decrement
0	0	1	Increment
0	1	0	Addition
0	1	1	Subtraction
1	0	0	AND
1	0	1	OR
1	1	0	XOR
1	1	1	Invert

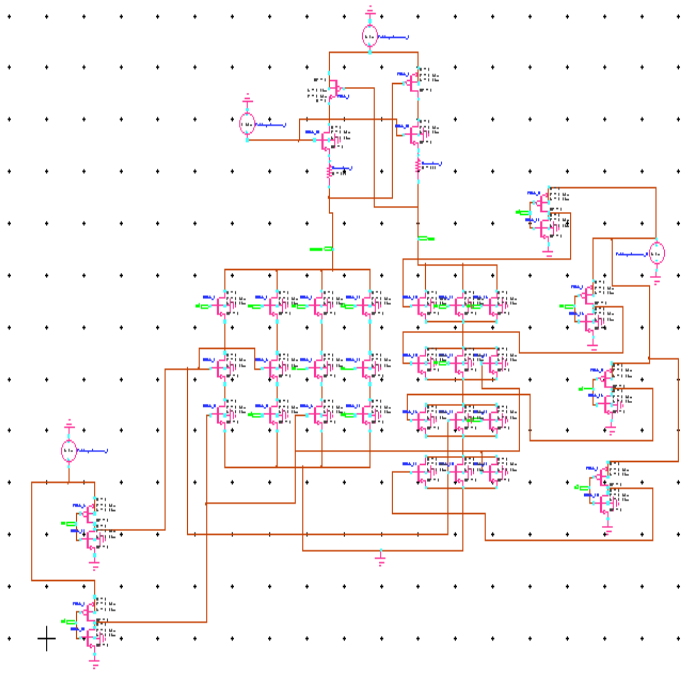

Fig 15: 4:1 Mux circuit schematic

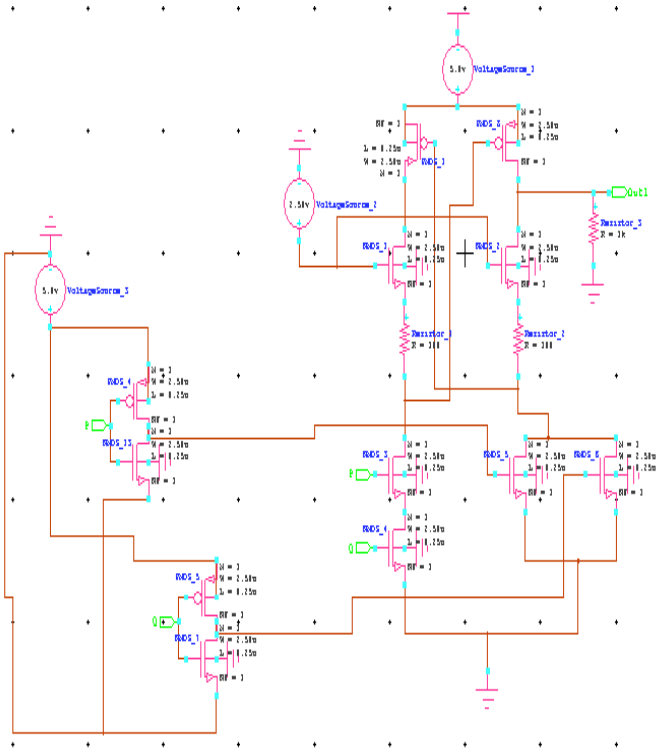

Fig 16: AND circuit schematic

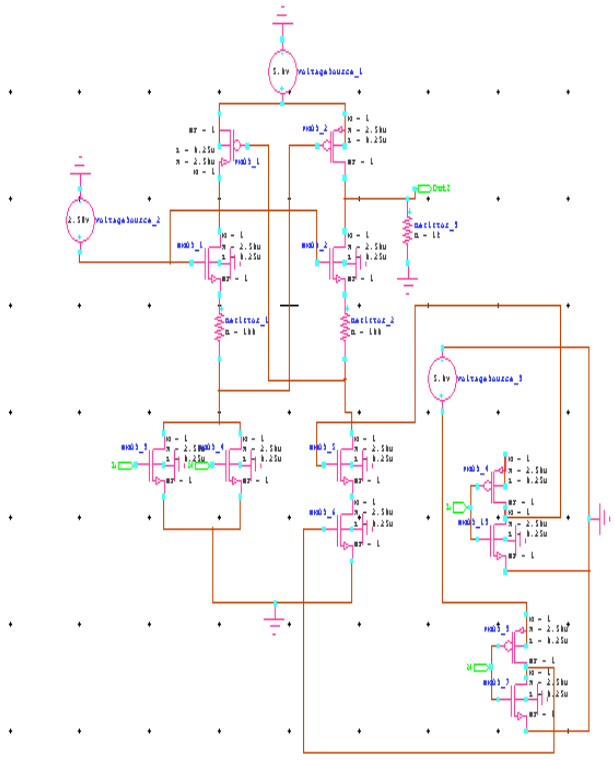

Fig 17: OR circuit schematic

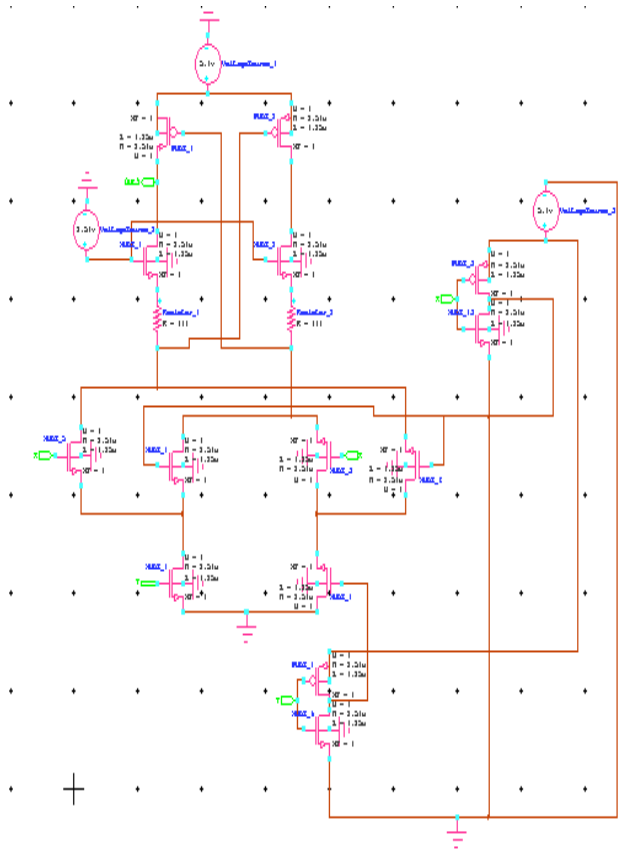

Fig 18: XOR circuit schematic

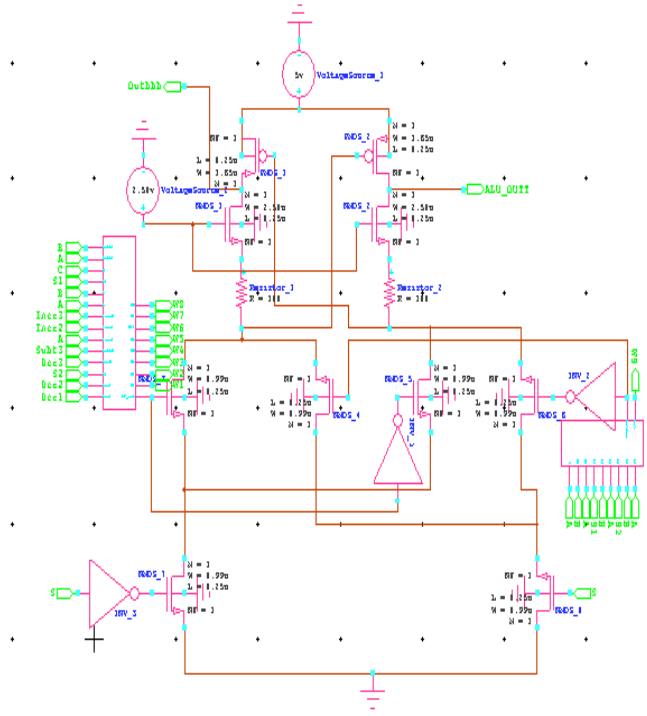

Fig 19: ALU circuit schematic

The output is taken across 2:1 mux [8]. The propagation delay, power dissipation and power delay product are calculated with power supply voltage as 5.0v and reference voltage as 2.58V provided to reference NMOS transistors.

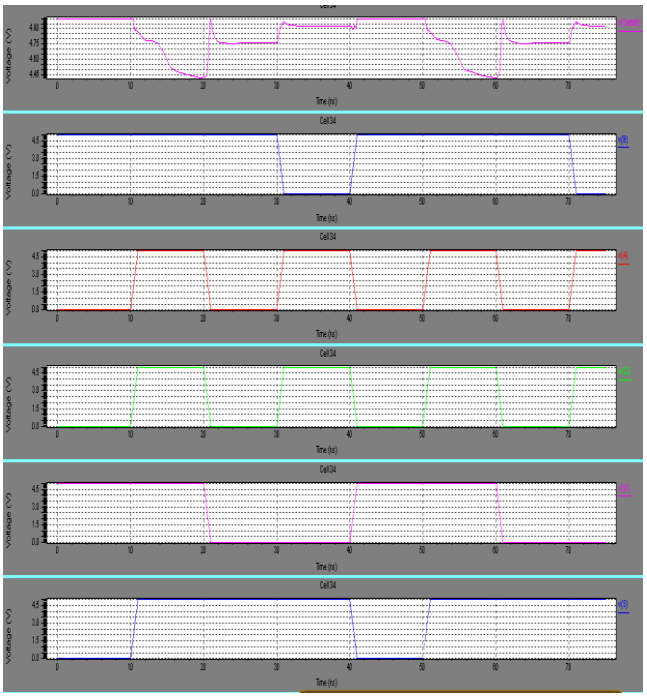

Fig 20: Simulation waveforms of ALU in W-edit

The given table shows the delay, power dissipation and power delay product calculated by using tanner eda v13.0 tool and technology file 130nm.

Table 6. Performance parameters of ALU

Function	Delay(ns)	Power(watt)	PDP(watt ns)
AND	2.02	6.732498e-007	13.626575 e-007
OR	1.385	3.561170e-009	4.93222045 e-009
XOR	1.91	9.706720e-011	18.5398352 e-011
INV	1.2175	9.217640e-007	11.2224767 e-007
Addition	1.955	2.218303e-009	3.58828129 e-009
Subtraction	1.955	1.835438e-009	3.58828129 e-009
Increment	1.955	1.537571e-009	3.005951305 e-009
Decrement	1.955	1.378934e-009	2.69581597 e-009

6. CONCLUSION

The proposed full adder has better performance in terms of delay. It is observed with the simulation results that with adding resistor, propagation delay decreases in a fast way. But it is observed that on addition of capacitor in parallel to the resistor added in the circuit, the delay decreases gradually and the power dissipates more but less gradually in comparison to the modified full adder with added resistance only. Since priority is high speed, proposed full adder with only added resistor is used in designing ALU .After the analysis , the other components of ALU are designed with same modified DSL logic technique This proposed ALU can be used for high speed and low power applications.

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