

# Analysis and Verification of Multi-Core Enabled ESL Model using SystemC and VLang

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## ABSTRACT

Today most of the system on chip (Soc) integrate multiple processing cores, digital signal processors, as well as dedicated hardware accelerators, etc [1]. This results into large and complex systems which pose challenges to conventional design and verification flow. This raises the need for higher level of abstraction (i.e. Electronics system level abstraction). This paper discusses how we can make changes in an existing conventional method of simulation to achieve really fast high yielding method of verification. The model is implemented using SystemC and Vlang. The results demonstrate the impact of enabling multiple simulators for verification of hardware models.

## Keywords

SystemC, Vlang, Multicore, Multithread, ESL

## 1. INTRODUCTION

Today, designers develop systems that consist of application specific hardware and software and needs to be developed synchronously on a persevering schedule. These systems need to go through a profound verification processes in order to avert a calamitous collapse of the system in a real world [2].

As we all know that necessity is the mother of invention. In order to meet the demand of such complex systems in the market, that too in a short span of time, designers need some powerful tools on which they can count easily for high productivity.

Your guess is right. SystemC is one of the languages that have emerged in respond to inescapable need for a language that can support an increasing in complexity and productivity of such electronic systems [3].

Open SystemC initiative was formed in 1990, to make new design language open to the community and not be proprietary [9]. SystemC is a language which offers productivity gains by allowing engineers to synchronously develop a high level abstraction for both hardware and software as these would exist on the final systems. High level abstraction is a methodology that benefits engineers to access better understanding of intricate processes and communication among other modules at early stage. This enables better, earlier verification and overall productivity gains through reuse of early system models [4].

## 2. INTRODUCTION TO SYSTEM

SystemC is a C++ class library and Open SystemC initiative (OSCI) supports TLM 2.0 transaction level modeling.

Here we have considered a simple algorithm of converting a PNG format file into buffer data using libpng library. Libpng is a library file that makes apparent the various methods of

modifying the PNG file into other formats. Libpng is a thread safe, on the condition that all the threads should be using different instances of the structures and their own image. Structure png\_struct and png\_info are the important structures. Structure png\_struct is an internal structure, which is not used by a user. Whereas png\_info structure specifies the information about the PNG file. The fields of png\_info were set to be directly accessible to the user. But this is a cause of problem for the applications using dynamically loaded libraries. Therefore to avoid this problem set and get functions were developed. The png.h is a indispensable header file used inside the code when programming with libpng.

One of the features, that libpng library offer, is to handle any special transfigurations of the image data. Both SystemC and libpng are C++ libraries which are available for free. Here we are modeling a multithreaded model for converting the RGB pixels of any image into grayscale.

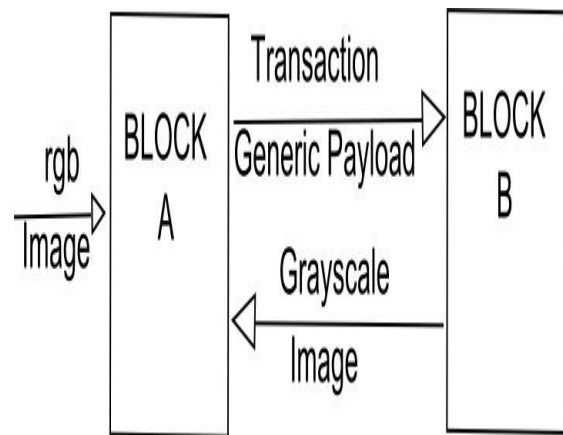


Figure 1: Shows the block diagram of the system.

Block A is modeled to take an image with rgb pixels as inputs. It extracts the information of each pixel and stores into a buffer. Here we add an additional payload known as generic payload to form a complete transaction as per the rules of TLM 2.0. Block A acts as initiator, as it initiates the transaction. Whereas block B acts as target as it responds to the transaction. Block B is responsible to read the data that is stored into the buffer by the block A and further making the changes in each pixel. Block B is modeled to run a following algorithm.

Image in png format, containing rgb pixels is fed into block A. Block A stores the information of the image in a buffer. It adds a generic payload with the existing stream of data stored in buffer. Thus initiate the transaction containing details of the image and acts as initiator. Block B acts as target as it

responds to the transaction initiated by the initiator. Once the transaction reaches the block B through function calls, the algorithm is followed, shown in Figure 2.

Block B recollects the information through the transaction. Divide the complete image in eight parts. Since our normal system consists of four cores, we can examine the performance of model by actually enabling four simulators simultaneously. This concept is not easy to understand as none of the hardware language allows the feature of enabling multiple simulators for verification purpose. But this is very essential feature that must be provided to the verification engineers. This feature is important as it gives the real savor of multi-core. Recently while comparing different languages with SystemC, there was a language which proved to be very pleasing, when it comes to verification. Vlang is the language which offers a great variety of features for verification engineers.

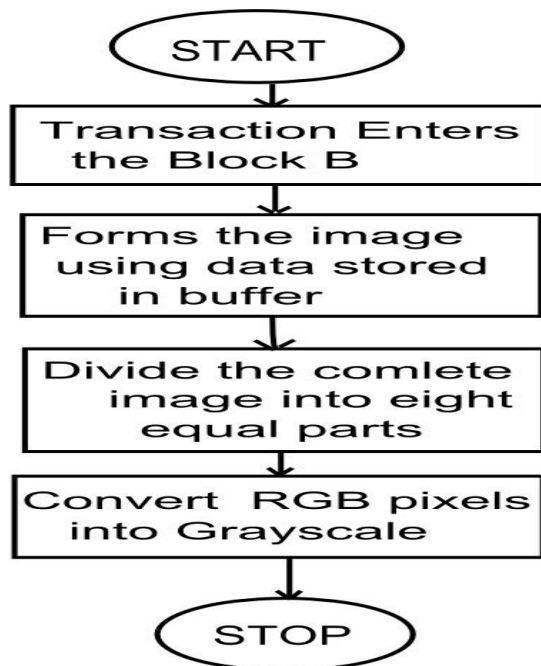


Figure 2: Shows the algorithm followed by block B

Vlang is the language which is recently developed by CoVerify Systems Technology. Unlike the old existing verification languages, Vlang is an open source verification language with some special features which will provide a new horizon for verification and testbench development. Vlang is a language which proves to be a great help for verification engineers as it consist of a very simple syntax and inherits some special features suchlike concept of object oriented programming, and multicore programming from D language. This makes it easy for a new developer to use this language. Even some new verification features and UVM has been implemented by the Vlang community. In this paper alsowe would be talking about the interface between the SystemC (TLM) and Vlang.

### 3. INTRODUCTION TO TRANSACTION LEVEL MODELING

Transaction level modeling in SystemC focus more on communication between processes rather than algorithm [5]. The communication between processes is done by function calls. It is assume that, some of the processes produce the data and some of the processes consume that data. While some processes are responsible for initiating the communication and other responds.

In TLM 2.0, the transaction is generally passed between initiator and target. A transaction is nothing but sets of C++ objects which are passed between initiator and target through function calls [6]. Both initiator and target use socket to send and receive the transaction respectively [7].

### 4. INTRODUCTION TO ALGORITHM

There are many algorithm for converting RGB image into grayscale are available. RGB image is the image containing the components of pure red, green, blue colour whereas grayscale image is the image containing only white and black component. Both RGB and gray values are incoded in a set of three equal numbers ranging from 0 to 255. For instance, white is represented as (255,255,255) and black is represented as (0,0,0). In order to determine grayscale value equivalent to its RGB value, one needs to calculate the average value of x by the given formula  $x = 0.299r + 0.587g + 0.114b$ . For instance, grayscale value equivalent to pure red (255,0,0) is gray (76,76,76).

In this paper work block A is designed using SystemC as shown in the Figure 1. As mentioned above block.

A is responsible for creating a transaction which will be fed into a block B. block B is designed using Vlang. This interface between SystemC and Vlang is at transaction level rather than signal level.

### 5. RESULTS

SystemC uses quick threads also known as Q threads as shown Figure 5. This means that if any multi-threaded application is written using SystemC, the compiler borrows one thread from the kernel of the operating system. Further, imposes all other threads of the application on a single thread borrowed from the kernel. This multiple threads present inside SystemC application are executed on the context based switching [8]. In context based switching, chunks of each thread are executed, one at a time. In order to perform a context switching, the scheduler has to save the state and instructor pointer for the current running task, has to work out the switching between the tasks and again it has to reload the CPU state. This also involves the loading and reloading of memory for data and instructions.

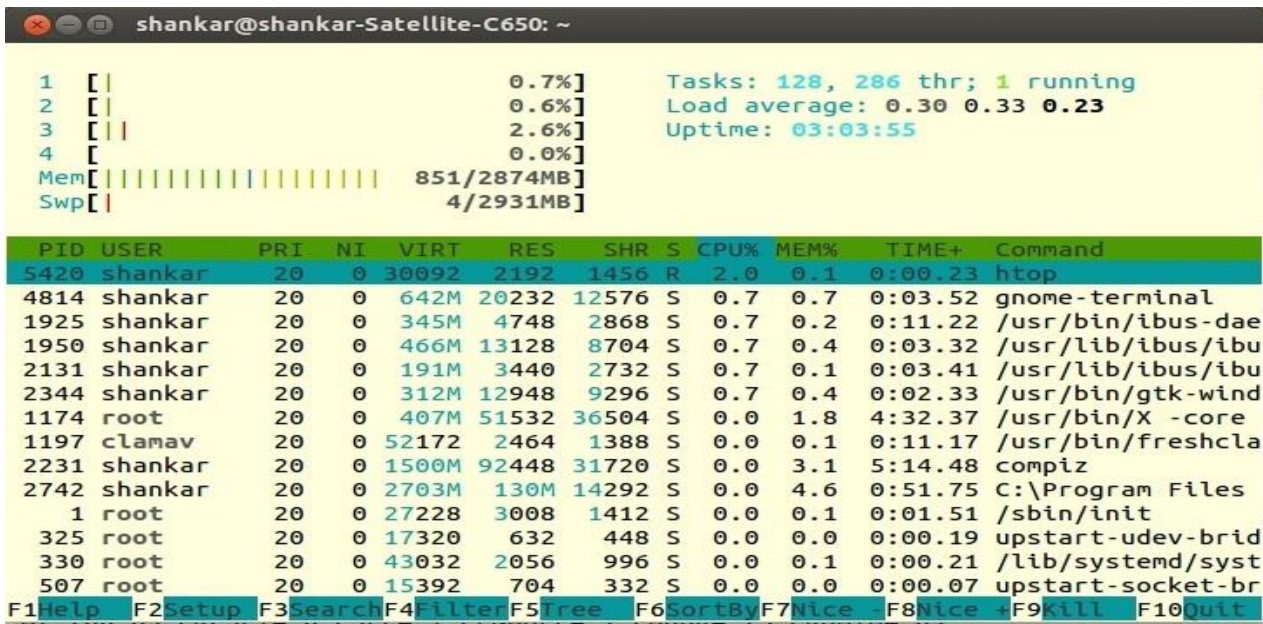


Figure 5: Shows the effect of running SystemC Application on kernel

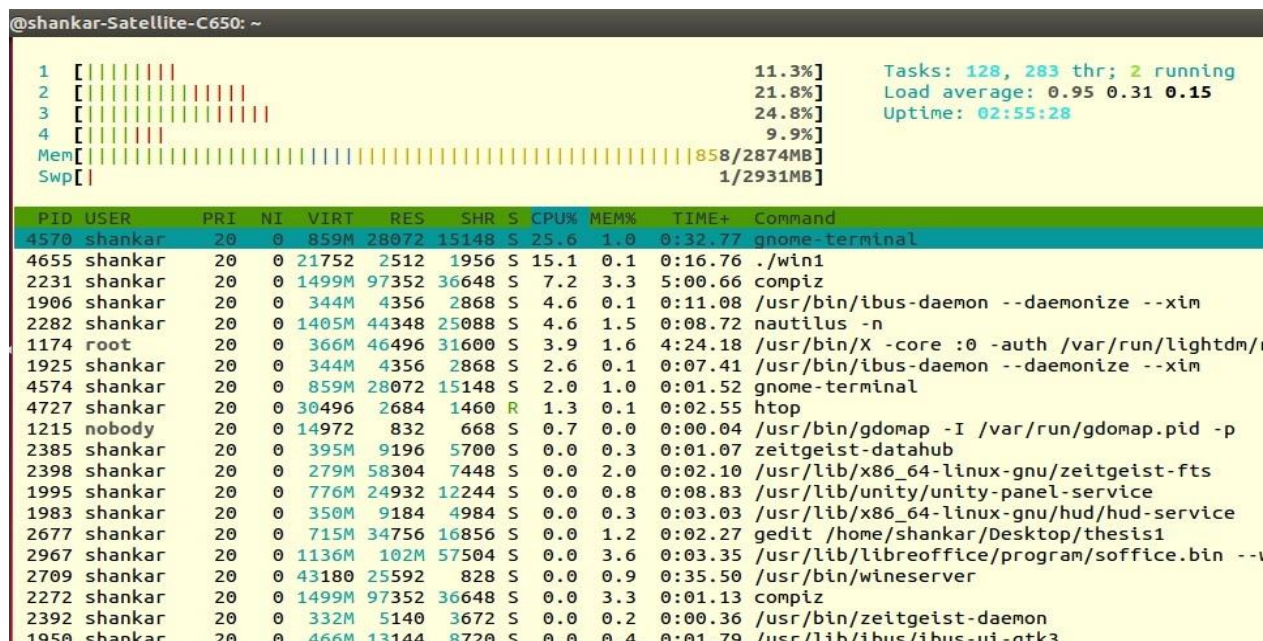


Figure 6: Shows the effect of running multi-threaded Vlang Application on kernel

Vlang uses preemptive threads also known as P threads as shown in Figure 6. This means that when a multi-threaded application is written using Vlang, the compiler can borrow more than one thread from the kernel of the operating system. The maximum number of threads which can be borrowed is limited by the number of cores CPU. Once the threads are acquired from the kernel, the application can run its multiple threads using context switching. Since block B is designed using Vlang, this scenario is common with block B. Whereas Figure 5 describes the scenario of block A.

## 6. CONCLUSION

In today's VLSI industry, the higher level of abstraction has become the necessity. Also, the Amdahl's law needs to be followed. Amdahl law states that in order to attain the

maximum speed for the given application, one need to exploit the maximum number of cores of CPU.

This work revolves around the above mentioned facts. Block A is designed to form a transaction containing generic payload using SystemC. Block B is designed to perform the parallel simulation on the different parts of the image and converts its RGB components into gray value.

In case of small multi-threaded application, the SystemC application seems to compile and run faster than Vlang. But in case of more complex multi-threaded application Vlang seems to be faster as compared to SystemC. This is due to the fact that the time required to acquire the multiple threads from the kernel is more as compared to the time required to acquire the single thread from the kernel.

However this paper does not aim to compare the above mentioned languages with reference to specific figures. This is due to the following reasons.

First, to compare two languages, we need to work on some standard real world applications which are written unbiased to both the languages (such as Ethernet, PCI, etc).

Second, mentioning the figures will violate the License conditions. No doubt Vlang claims to have better features as compared to SystemC but as far as single-core is concerned, the choice may vary from user to user and application to application. If the user wants to make his design or Verification IP (VIP) with multi-core enabled feature, Vlang is more prominent.

## **7. REFERENCE**

- [1] C. Schumacher, J.H. Weinstock, R. Leupers, G. Ascheid, "Legacy SystemC Model Integration into Parallel SystemC Simulators." In the proceedings of *Parallel and Distributed Processign Symposium Workshops & PhD Forum international Conference*, Cambridge, pp. 2188 – 2193, 20 – 24 May 2013.
- [2] T. Chan, "A robust multithreaded HDL/ESL simulator for deep submicron integrated circuit designs," In the proceedings of *Circuits and Systems Asia Pacific Conference*, Kaohsiung, pp. 416 – 419, 2 – 5 Dec. 2012.
- [3] A. Pulka, L. Golly, "Multitask Real-time Systems modeling in SystemC," In the proceedings of *Signals and Electroni Systems International Conference*, Wroclaw, pp. 1 – 6, 18 – 21 Sept. 2012
- [4] A. Prakash, H.D. Patel, R. Sinha, "Parallel simulation of mixed – abstraction SystemC models on GPUs and multicore CPUs," In the proceedings of *Design Automation Conference*, Sydney, pp. 455 – 460, 30 Jan. – 2 Feb. 2012.
- [5] R.S. Lobato, R. Spolon, M.A. Cavenaghi, R.C. Detomini, "Using GPU to exploit parallelism on cryptography," In the proceedings of *Information Systems and Technologies Conference*, Chaves, pp. 1 – 6, 15 – 18 June 2011.
- [6] T. Chan, "Race logic synthesis for a multithreaded HDL/ESL simulator for Soc designs," In the proceedings of *Circuits and Systems Asia Pacific Conference*, Kuala Lumpur, pp. 1179 – 1182, 6 – 9 Dec. 2010.
- [7] Sen, A., "Mutation Operators for concurrent SystemC Designs," In the proceedings of *Microprocessor Test and Verification Conference*, Austin, pp. 27 – 31, 7 – 9 Dec. 2009.
- [8] S. Sudharsanan, N. Manjikian, "Modeling and simulation of multicore multithreaded processor architectures in SystemC," In the proceedings of *Electrical and Computer Engineering conference*, Niagara Falls, Ontario, pp. 001155 – 001160, 4 – 7 May 2008.
- [9] IEEE Standards for standards System CLanguage Reference Manual, pp.421.