High-Resolution CMOS Counter Type ADC Layout Design by using Transmission Gate Logic

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Abstract:

In this paper, we propose counter type ADC for high-speed applications. Counter type ADCs are one of the most popular ADC topology used to implement moderate resolution converter due to their reasonably fast conversion time and simplicity.. Designed ADC has 8 input channels each of which has 0 – 2.6 V signal range. The resolution of ADC the converter is 8 bits. The amount of passing through a system from input to output ADCs can be increased by using its technique This is implemention on the circuit level with pass transistor circuit. The primary focus of this work design and implementation of a pass transistor based Analog-to-Digital converter. The proposed counter type ADC is composed of a 8-bit DAC design by using transmission gate logic, a comparator logic , 8 bit digital counter and "AND" gates to pass the clock signal by considering the chip area, operation speed, and circuit complexity.

Introduction:

The measurement taken by analog instruments are continuous and slow. Analog-to-digital converters (ADCs) are use as a intermediate path between analog signal such asd voltage, current, power, frequency etc and the digital signals. Continuous time analog signal to be converted to a discrete time signal with the relationship of continuous time and descrete as t=nT, where T is the sampling time depends on sampling frequency. The digital system may consist of resistor, capacitors, transistors, linear ICs, If an analog readout is desire then it can be done by digital to analog converter (DAC). DAC and ADC form two very important aspects of digital data processing.[3]-[4] Most physical variables are analog in natureand can take on any value within a continuous range of values. Digital system performs all their operation using digital circuitry. Thus the analog signals are converted into digital form by using analog to digital converters. Thus the analog outputs generated by transducers are fed to ADC for converting it to its equivalent digital form.The digital ouputs consist of number of bits that represents the value of analog input. Digital to analog converter is a straight forward process and is considerably eisear than ADC. The DAC is usually an integral part of any Analog to Digital Converter. [6]

Designed ADC has 8 input channels each of which has 0 – 2.6 V signal range. The resolution of the converter is 8 bits. Of course, integral and dynamic nonlinearities of the converter are less than an LSB throughout the whole input signal range. One LSB is around 0.01V. The conversion time is specified as less than 10 μs with 1GHz system clock frequency.

ADC Static Performance Metrics

Resolution of DAC is define as the smallest change that can occur in the analog output as a result of change in the digital input. Resolution is also refer to as step size, since it is the amount that output voltage will change as the digital input value is change from one step to the next. Percentage resolution is given by[1]

$$\% \text{ Resulution} = \frac{\text{Step Size}}{\text{Full Scale}} * 100$$

Percentage resolution is also define as the reciprocal of total number of states. This means that increase in number of bits w2ill increases the total number of steps creating smaller step size and finer resolution.

The quantization step is the same as the voltage range of Least Significant Bit (LSB). Then the function DNL and INL can be defined as

$$DNL(i) = \frac{V_{in}(D_i) - V_{in}(D_{i-1}) - \Delta}{\Delta}$$

$$INL(i) = \sum_{k=1}^{i} DNL(k)$$

Where Vin (D_i) and Vin (D_{i-1}) represent the input voltage corresponding the output code D_i and D_{i-1}.[1]

Differential Non-Linearity (DNL)

When the step size of an ADC's output is not equal to the ideal step size, the ADC is said to have Differential nonlinearity. The DNL is a measured of the separation between one code to nearest code If the DNL is greater than 1 LSB, a non-monotonic transfer function will cause missing codes.

Integral Non-Linearity (INL)

Integral nonlinearity is the difference between maximum the quality of being determine digital code resolution characteristicmeasured vertically. The INL can be express as a positive INL and negative INL. The maximum difference between the actual and ideal transfer characteristic is the INL.

Monotonocity:

Monotonocity in a DAC that define as a digital code to the converter increases over its full scale range, the analog output never exhibit a decrease between one conversion digital voltage and the another digital voltage. In other words level or sideways position between the two end of the transfer characteristic is never negative in a monotonic- converter.

Offset Errors: It is a costant differenc between the actual finite resolution characteristic and the ideal finite resolution characteristic.[1]-[4]

Blocks of ADC:

The our The proposed counter type ADC in the is composed of a 8-bit voltage scaling DAC, a comparator logic , 8 bit digital counter and and logic to pass the clock signal by considering the chip area, operation speed, and circuit complexity. Voltage scaling DAC convert the reference voltage Vref to a set of 2^n voltages that are decoded to a single analog output by the input digital word.The block diagram of this DAC and its layout design is shown in fig and fig

respectively[5]. The voltage scaling is done by using series connected resisitors with Vref. And ground.in our design we can use pass transistor transmission gate to design this voltage scaling

DAC.

Transmission Gate (TG):

A transmission gate is an analog switch controlled by logic signals. It consists of a n and a p type MOS transistor. When the EN = 1 the gate conducts and shorts the input signal and the output signal, otherwise it cuts off and the output floats.[2]

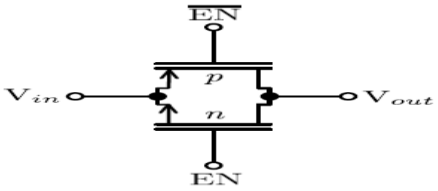

Fig 1. Transmission Gate

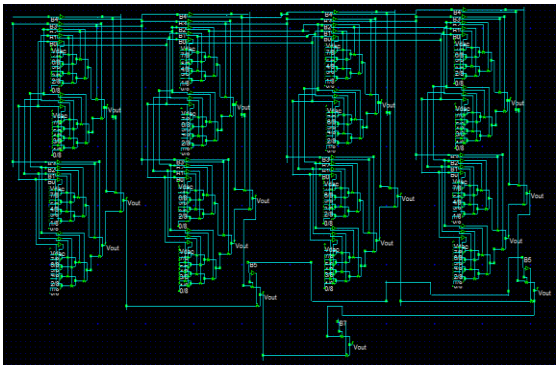

Fig 2 : Block schematic of TG base voltage scaling 8 bit DAC

A differential circuit design is a must to suppress the noise injected by the switching regulators to the substrate and to the supply lines. These noise signals are common mode signals; they can be suppressed further by the common mode rejection of the differential circuits.Fig show differential amplifier. It convert the input voltage to a current to solve high voltage related issues and then convert back to voltage. This amplifier architecture does not employ internal feedback to correct the phase margin because it is self-compensating, i.e., the larger the capacitive load on the amplifier, the greater the phase margin. Its transfer function can be expressed as

$VOUT = R1 + R2 /R1 VB − R2/ R1 V_{IN}$

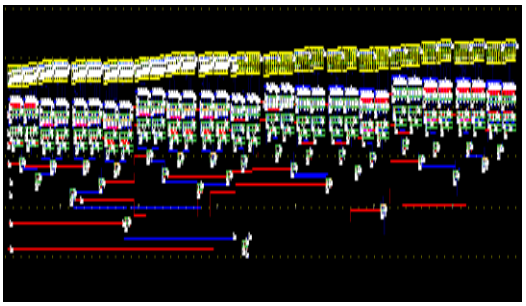

Fig 3.Layout design of 8 bit DAC

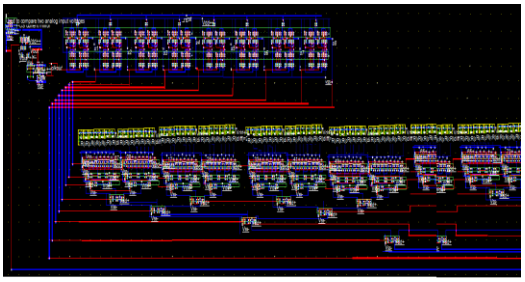

Fig 4. Layout design of 8 bit ADC

In this ADC the reference ramp type voltage is applied to the comparator and when it become equal to the input analog voltage , the conversion would be complete. conversion During this process, the n bit counter hold the digital value equivalent to the analog input voltage shown on fig4.

The ADC operation proceeds as follows:

1. A start pulse is applied to reset the asynchronous counter to zero. The high at start also inhibit the clock pulse from passing through the AND gate into the counter. The output of DAC will be zero.
2. Thus comparator start to compare the DAC output with the input analog voltage. Since Va> Vout , the Asynchronous comparator output will be high.
3. When start pulse become low, the AND gate is enable and clock pulse get through to the counter.[3] Thus asynchronous counter increment at every clock pulse, and DAC output increases one step at time.[5]
4. This continues until vout reaches a step that exceed Vanalog input. At this time Asynchronous comparator output will become low and inhibit the flow of clock pulses into the asynchronous counter and counter will stop counting shown on fig.5.
5. The conversion process is now complete 1nS/s.and the content of the counter are the digital equivalent of analog input voltage Vanalog. The Asynchronus counter will hold this digital value until the next start pulse initiate a new conversion.[5]

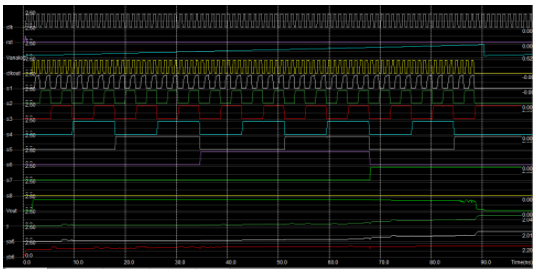

Fig 5.Timing simulation of 8 bit ADC

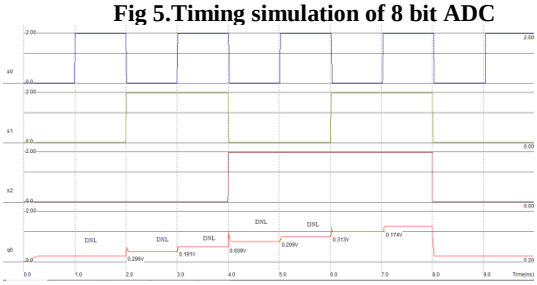

Fig 6. DNL calculation from DAC

DNL is the measure in 3 bit counter type DAC of the deviation of one digital output voltage to nearest digital output voltage measure at each vertical step fig6.

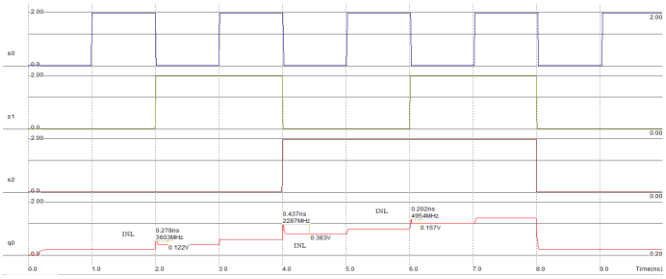

Fig 7. INL calculation from DAC

INLs the maximum difference between actual code to the and the ideal finite code resolution characteristic measure vertically. The INL is measure in 3 bit counter type DAC as -0.122, -0.383, -0.157shown on fig7.

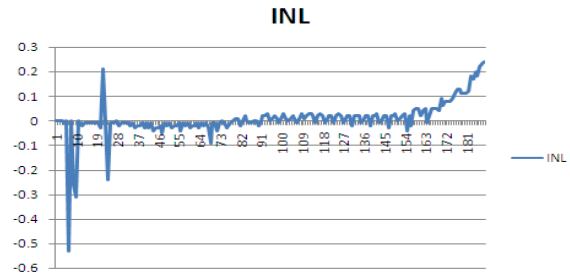

Fig 8.INL calculation fro 8 bit DAC

In 8 bit counter type DAC circuit to be measure of INL error is 0.23LSB, -0.55 LSB shown on fig.8.

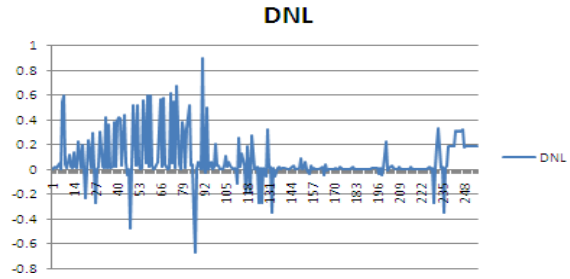

Fig 9. DNL calculation fro 8 bit DAC

In 8 bit counter type DAC circuit to be measure of DNL error is 0.85LSB, -0.65 LSB shown on fig9.

RESULT:-

Authors	Hanqing Xing, Degang Chen.	Alok Barua, Md. Tausiff	Young-Deuk-Jeon, Jae –Won Nam	Our Work
CMOS Technology	0.5µm	180 nm	45 nm	50nm
Supply	1.7V	2.5V	1.2V	1.2V
INL	±0.15 LSB	±1 LSB	0.54,-0.67 LSB	0.85,-0.62 LSB
DNL	±0.25,	±1LSB	0.23,-0.36 LSB	0.85,-0.62 LSB
Power Consumption	------	3.26 mW	17.65mW	2.96mW

Table1:-Comparision Analysis of Our Work

In a counter type ADC design cmos layout using pass transistor reduce the power of 2.96 mW and Nonlinearity error such as INL is 0.85,0.62LSB and DNL is 0.85,-0.62 shown on Table1.

Conclusion:

In this paper, an 8-bit Sub-Ranging Analog to Digital converter (ADC) is proposed for for high-speed applications. The throughput of ADCs can be increased by using parallelism. This is demonstrated on the circuit level with pass transistor circuit. The primary focus of this work design and implementation of a pass transistor based Analog-to-Digital converter.

References:

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