# A Methodology for Very Low Power and Small Size Capsule Manufacturing for Wireless Capsule Endoscopy

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## ABSTRACT

We are presenting a method of reducing the size of traditional capsule used in wireless capsule endoscopy (WCE) for . The conventional wireless endoscopic capsule was manufactured on 18μm technology and its size is 26mmx11mm. Here we are using Ultrascale FinFET 16nm technology to reduce the size of capsule . By using this technique the Size of traditional capsule can be reduced by 11-12 % .Using this method leakage current content reduces and power consumption also reduces up to 50% than the traditional one. The device can be operated on a very low operating voltage and thus the life of battery increases. But after the advancement of FPGA technology, here we are emphasizing on ultra-scale technology with 16nm FINFET technology for fabrication of CMOS transistors using 16 nm technology 3D ICs. This method increases system performance and speed upto 2 folds and speed increases upto 30% .

## General Terms

Wireless Capsule Endoscopy, FinFET, Ultrascale ,dual-gate MOSFET

## Keywords

FinFET ,16nm Technology, Ultrascale, MOSFET, FPGA, leakage current, Capsule Endoscopy.

## 1. INTRODUCTION

Wireless capsule endoscopy (WCE) is a state of art technique designed to allow gastroenterologist (physicians) to visualize the most inaccessible parts of the gastrointestinal (GI) tract. Endoscopy provides unprecedented diagnostic capabilities for certain ailments that no other method can match today, such as detecting polyps[5] in the colon and ulcers or fungi in the GI tract. The gastroenterologist uses captured images for diagnosis of various diseases like Diarrhoea,[1][2] Anaemia and internal bleeding, functioning of Bowel, Malabsorption, pain in Abdominal sections, Tumors and some cancers, Celiac sprue diseases. As well as the images captures and decompressed help the gastroenterologist to monitor the progress of treatment plans for the patient conditions. These methods provide much more accurate visualization gastrointestinal diseases than could be achieved in earlier endoscope systems, enabling physicians to more accurately diagnose patient ailments[3]. Such demands force suppliers to deploy new techniques for high quality image capturing, image compression, image decompression , to reduce the size of capsule and the life of capsule ie the battery life so that sensor can capture more images of tract and this will help the physician in diagnosis of disease .

Traditional capsule[6] endoscopy uses a vitamin pill size just 26mm x11mm ( **Figure 1 (a)**).The front end of the capsule has an optical dome where white light emitting diodes (LEDs) illuminate the luminal surface of the gut, and a micro camera, image compression block which compresses captured images
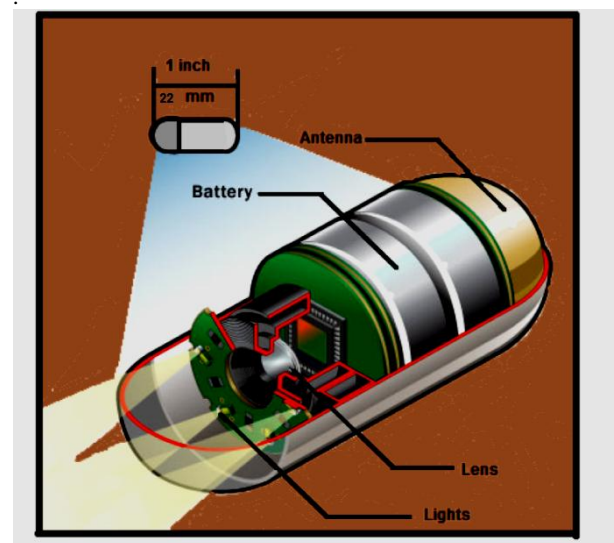
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**Fig- 1(a) Traditional Endoscopic Capsule**

Patient has to swallow it and then it travels through the gastrointestinal (GI) tract, buffering these images in memory and JPEG –LS and LZO technique is used for image compression, after compression .These compressed images finally transmitted via wireless transmission to a receiver worn by a patient. This data are transferred to a computer for interpretation by the specialists.

The capsule is then passed in the patient's stool without the need for retrieval (**Figure -1(b)**).

Another part of the capsule contains a small battery that can last up to 8-10 hours.

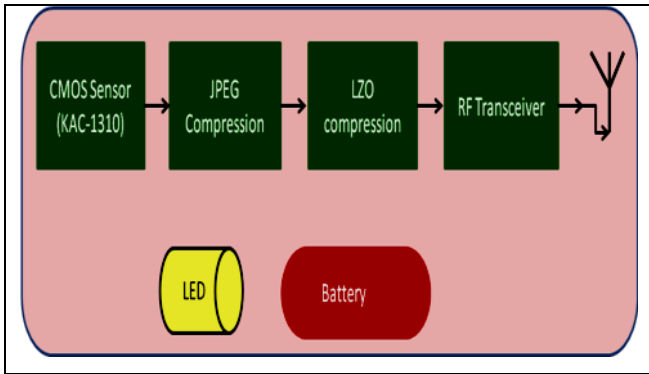Technology advancements have enabled the use of endoscopes in many different applications

**Fig-1(b) Block Diagram of Endoscopy Capsule**

Health care providers have aggressively adopted endoscopic techniques and continue to challenge suppliers to push the boundaries of technology for many reasons[11]. Diagnosis with endoscopes is radiation-free and can be done with minimal pain to the patient. With these inherent benefits, physicians have aggressively adopted endoscopic techniques and are continually demanding innovation to improve imaging capabilities even further. Such demands force suppliers to deploy new techniques for high quality image capturing, image compression, to reduce the size of capsule and the life of capsule and the battery life so that sensor can capture more images of tract and this will help to the physician[6].

These methods provide much more accurate visualization gastrointestinal diseases than could be achieved in earlier endoscope systems, enabling physicians to more accurately diagnose patient ailments. Endoscopy greatly improves the quality of patient care by enabling minimally invasive surgical techniques[7]. While traditional surgeries required large incisions to enable surgeons to view the subject tissue and to use large, hand-held instruments, endoscopes and laparoscopes (a type of endoscope with a rigid tube)[8] enable minimally invasive surgical techniques with only one or two incisions less than a centimeter in length. This greatly reduces risk of infection and provides faster patient recovery time. Within this small system[9], the electronics must also be low heat generating, since there is minimal clearance for heat dissipation techniques, and the tolerance for heat at the exterior of handheld products is low.

The conventional endoscopic capsule was manufactured on 18μm technology and thus the size is 26mmx11mm. After using 16nm FinFET the capsule size reduces 11.25% approximately[12].

Because memory is used to store images and its consumed more power thus in this paper our focus is on reducing the power consumption and size of capsule and so that the battery can last up to 10-12 hours and more images can be captured for examination.

Here we propose a methodology by exploring the unique features of FPGA Ultrascale planar technology which has enabled the extreme miniaturization of ICs and 16nm FinFET technology for 3D ICs[13]. With the planar process, semiconductors are built in layers on top of, and etched into, ultrapure silicon wafers. In 16nm FinFET technology the gate is surrounded by three sides while in a planar transistor it is surrounded by on surface only[14]. Thus three sides surrounding increases the speed of the device, reduces leakage current and power consumption reduces.

The rest of the paper is arranged as follows: -The 2nd section is design criteria,3rd is material and methodology, the 4th section describes the analysis,5th results and tables and final is conclusion in the 6th section.

## 2. DESIGN CRITERIA
We are focusing on the following design criterion:
  (i)   To improve battery life ,the capsule should be operated at low power consumption[4] .
  (ii)  The size of a conventional capsule is limited to 26mm ×11mm. Thus, the critical issue is area captured by capsule that limits the usage of memory size. More memory consumes more silicon area and power. Here, we focus on methods that reduces memory size.
  (iii) The image sensor should be of high resolution and consumes less power. The compressor should scan images in raster scan fashion.
  (iv)  For an accurate diagnosis, the decompressed and reconstructed image quality is very important. So, we focus on lossless and fast image compression and decompression algorithms.
  (v)   To reduce the memory requirements, captured images are compressed using JPEG technique and then LZO . This approach reduces the memory requirement.

We are proposing a method to reduce the leakage current in MOSFETs so that power consumption reduces, performance improves and to increase the battery backup .

## 3. MATERIAL AND MATHODOLOGY
### 3.1 Planar Transistor
In traditional planar transistor source and drain is embedded in substrate. The 'gate' electrode ( **Figure(2(a)**) is placed above the conducting channel ,is separated from conducting channel by insulating layer. The gate creates an electric field that controls the flow of charge carriers between source and drain through that conducting channel[15]. If the dimensions of IC processes shrinks, unwanted leakage currents grows, particularly between source and drain. In the planar FET, the single gate provides inadequate electrostatic control over the channel region, hence leading to large leakage currents between the source and the drain when the gate is "off."

To overcome this leakage problem, if we dope the channel increasingly heavily , which reduces carrier mobility and device performance.
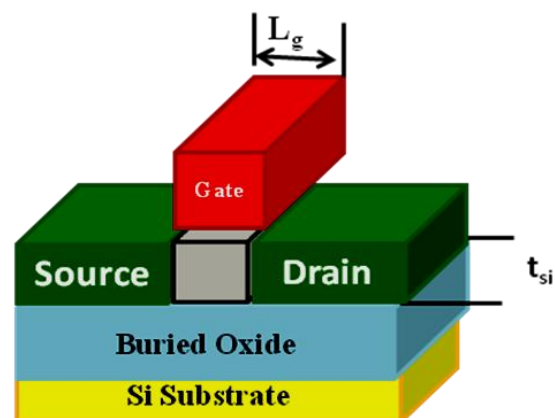


**Fig-2(a) Planar Transistor**

The standard threshold voltage of a MOSFET with long channel length/width and uniform substrate doping concentration is given by:

$$Vt = VFB + 2\emptyset B + 2\varepsilon q NA \frac{(\sqrt{2\emptyset B + Vsb})}{Cox} + Vg - trapped$$

where $V_{FB}$ is the flat band voltage, $V_{Tideal}$ is the ideal threshold voltage of the long channel device at zero volt substrate bias.
Threshold depends on:
– Physics constants
– Doping concentration
– Source to bulk voltage
– Thickness of gate insulator
– Radiation damage

## 3.2 Dual Gate Transistor

If a gate is build above and below, the channel of a planar transistor, and the thickness of channel is reduced so that the gate had better control over it, leakage current is dramatically reduces.

Example: In one experiment, the thickness of channel is halved from 20nm to 10 nm in a double-gate planar transistor, leakage current reduces up to 8000-fold. **(Figure -2(b))**
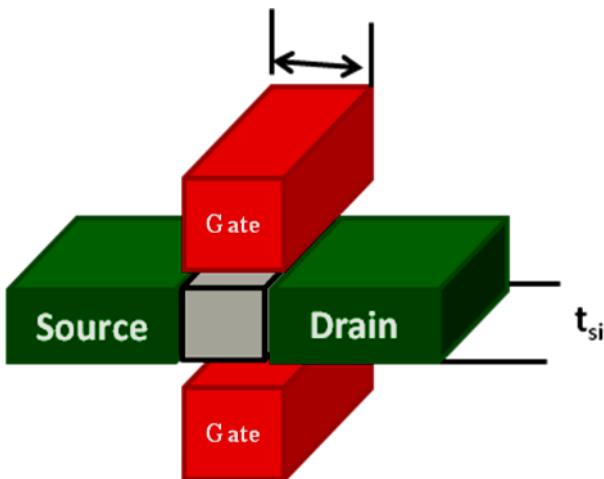


**Fig-2(b) Dual Gate Planar Transistor**

## 3.3 FinFET Transistor

A FinFET is comprised of fins that form the source and drain portion of the transistor and provide the path (channel) for current to flow when switched on. The gate, which controls the switching operation, wraps around the fins to form a 3-D structure.

To make FinFET turn the double-gate device through 90 degrees (**Figure 2-(c)**), the gate electrode is deposited over the surface of silicon, the channel is built in a fin and gate covers the surface of the silicon .This method creates a single gate formation that means it is possible to control the channel from both sides and the top also (**Figure 2(d)**).
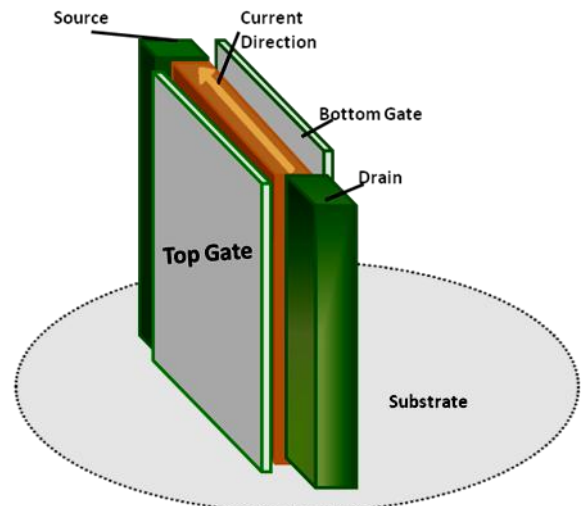


**Fig- 2(c) FinFET**

The lesser the thickness of the fin, the lower the leakage current, and if fin height is increases , improves its drive strength.

The distance between fins (their pitch) determines the area each device will take in a layout, although there's a trade-off between making the fins closer together. Closer the Fins , increases density but limits the tilt angle available to implant the source and drain, and performance.

The channel of a FinFET transistor is formed in a thin vertical fin that is wrapped and controlled by the gate from three sides. The most important parameters of a FinFET are its height (HFIN), its width or body thickness (Tfin), and its gate length (L) as shown in Figure 2(d). The effective electrical width of a FinFET is the planar width/body thickness plus twice the fin height .
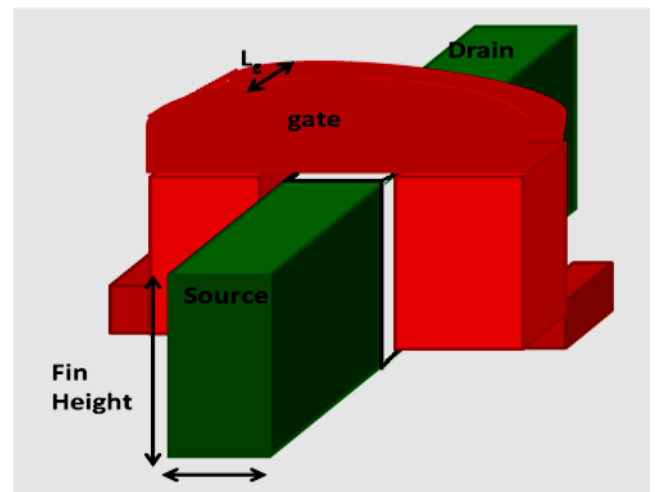


**Fig-2(d) FinFET**

Thus using 16nm FinFET technology, the thickness of Fins is 16nm and it reduces the leakage problem.

## 3.4 Multi-Gate FinFET

FinFET devices are also referred to as "multi-gate" transistors. In this device structure, the fin body often needs to be fully depleted even in the sub-threshold region. This results in much better electrostatic control of the channel.This

improves   electrical characteristics, such as faster turning on and off.

In practice, the thin Fin body is required in order for the wrapped gate to attain good control of the channel.Tri-gate or 3D transistor **(Figure- 2(e)) f**abrication is used for the nonplanar transistor architecture used in  processors.

These transistors employ a single gate stacked on top of two vertical gates .It gives  three times the surface area for electrons to    travel.    These    tri-gate    transistors reduce leakage and  consume  far  less  power than  current transistors. This architecture allows up to 37% higher speed, as well as  a power consumption at under 50% of the previous conventional type of transistors.
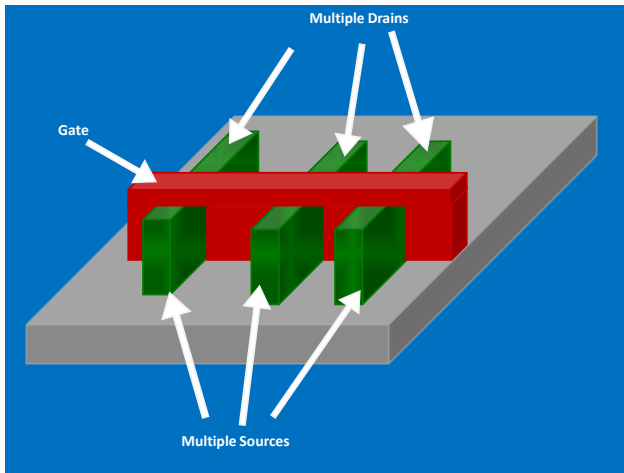


**Fig-2(e) TriGate or 3D Transistors**

**B**uffer   memory   of   FinFET   technology   have   higher performance   as   well   as   lower   leakage   than   planar conventional buffer memory, and can operate at lower operating voltages. The devices offer good static noise margins   at   these   low   voltages,   because   dopant-based variability is low, and good noise to signal ratios can be achieved. Due to lower operating voltage and less leakage current Read and Write margins are smaller, and their distribution narrower. Buffer memory to store images can be made on 16nm FinFET technology which reduces the leakage current and improves performance, speed and operated on low operating voltage .

## 4.  ANALYSIS
16 nm FinFET    process technology    provides several advantages over the preceding planar processes – some of these benefits are listed below.

1.  Lower leakage and dynamic power: Very good electrostatic control of the channel is a key benefit of FinFETs. The channel can be blocked more easily. The sub-threshold behaviour of FinFETs  is nearly impossible to achieve with planar technology (Figure 4). Lower dynamic power is achieved with options to reduce the threshold voltage of the transistor, enabling lower power supplies and overall dynamic power consumption, lower leakage current .

2.  Higher integration: The vertical channel orientation of FinFETs deliver more performance per linear

width   than   planar   FETs   even   after   the   isolation dead-area between the fins is taken into account.
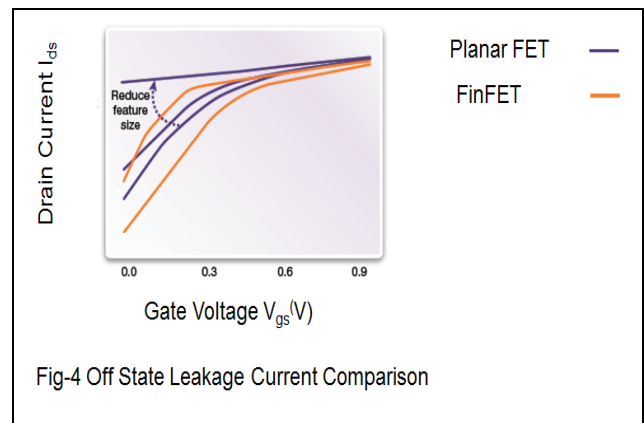


Fig-4 Off State Leakage Current Comparison

## 5.  RESULTS
i)   At 1V, the finFET speed is 18% more than the equivalent conventional planar device

ii)   At 0.7V, the FinFET is  37% faster than equivalent planar transistor. This is because the finFET's sub-threshold swing is lower than in a planar device, so the device can be operated at lower threshold voltages for the same leakage.

iii)   The  difference  between  the  gate  and  threshold voltage at very low operating voltages is much greater,      exaggerating      the      performance advantage of very low-voltage finFETs.

iv)   FinFETs are  up to 37% faster than the traditional planar transistors.

v)   It is  using less than half the dynamic power or cut static leakage current by as much as 90%.

vi)   Dynamic power consumption can be reduces up to 50% at 0.7V.

vii)   Making buffer memory on this technology also helps to reduce power consumption, leakage current and improves speed and size of buffer

viii)  Using 16nm FinFET technology in manufacturing endoscopic capsules also reduces its size up to 11-12% than a traditional 0.18 μm technology based capsule.

## 6.  CONCLUSION
Here we presented 16nm FinFET technology to improve the conventional endoscopic capsule performance. The proposed methodology   for   manufacturing   endoscopic   capsules increases the life of battery, reduces power consumption up to 50%, reduces size up to 11-12% and leakage upto 37%   .

## 7.  ACKNOWLEDGEMENT

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