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A Versatile Digitally Programmable Voltage Mode Multifunctional Biquadratic Filter

Bilal Arif
Department of Electronics Engineering
Aligarh Muslim University
Aligarh, India

Mohd. Usama Ismail
Department of Electronics Engineering
Aligarh Muslim University
Aligarh, India

Ale Imran
Department of Electronics Engineering
Aligarh Muslim University
Aligarh, India

ABSTRACT

In this paper, a digitally controlled single input multi-output voltage mode multifunctional biquadratic filter is presented. The circuit makes use of only a single DVCC, two grounded capacitors, one grounded and two floating resistors. The digital control is incorporated using a current-summing network (CSN). Tuning of cut-off frequency is carried out with the help of a 3–bit digital control word. PSPICE simulations using TSMC 0.25 micron CMOS technology have been performed to validate the theoretically predicted results.

General Terms

Analog Signal Processing, Active Filters

Keywords

Current-mode; Voltage-mode; Differential Voltage Current Conveyor (DVCC); multifunctional filter; digitally controlled circuits; cut off frequency; single input multi output (S.I.M.O).

1. INTRODUCTION

Lately the world has observed the emergence of the current mode circuits as new and more efficient analog building blocks owing to the various advantages they have over the conventional voltage mode circuits, like wider bandwidth, greater linearity, higher slew-rate, better dynamic range, simple circuitry and low power consumption [1]. Resulting in inception of new current-mode active building blocks such as operational transconductance amplifiers, current-feedback op-amps (CFOA), second generation current conveyors (CCII), four terminal floating nullors (FTFN), differential voltage current conveyor (DVCC), differential difference current conveyor (DDCC), third-generation current-conveyor (CCIII), dual X current conveyors (DXCCII), current controlled current conveyors (CCCII) [2].

Instrumentation, analog signal processing, automatic control and communication are the application areas for current-mode circuits. Realization of the current mode filters and oscillators is the most significant of these applications [3].

CCII (second generation current conveyor) has become very popular and is very useful [4]. But it has its own limitations such as it cannot provide differential or floating inputs and also has only single high input impedance terminal.

Considering drawbacks of CCII block new analog building blocks were introduced which include differential difference current conveyor (DDCC) [5] another building block introduced was differential voltage current conveyor (DVCC) which is slight modified version of DDCC block having its Y_3 terminal grounded [6]. DVCC is a very useful analog building block whose applications have been thoroughly worked upon and could be studied in the existing literature. [7-10]

In this paper , the filter circuit proposed in [11] by Hua-Pin Chen, Wei Chen and Guo-Wei Huang employs a single DVCC, two grounded capacitors and three resistors is used to design and implement a digitally controlled S.I.M.O. voltage-mode multifunctional biquadratic filter.

Simultaneous realization of lowpass, bandpass and highpass responses increases the utilization of the filter circuit reduces its overall cost Use of grounded capacitors increases the circuit's suitability for integration as grounded capacitors can compensate for the stray capacitances at the nodes. PSPICE simulations of the CMOS based controlled multifunctional filter are performed to demonstrate results.

2. DVCC

As shown in Fig. 1, the DVCC is a five-terminal active analog building block with terminal characteristics described by the following matrix equation [12].

$$\begin{pmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z+} \\ I_{Z-} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_{Z+} \\ V_{Z-} \end{pmatrix} \qquad (1)$$

An ideal DVCC has very low (almost zero) input resistance at terminal X, and quite large (infinite) resistance at the two Y terminals as well as the Z terminal. The output current follows the flow direction of the input current with both currents flowing either into or out of the device. The CMOS implementation of DVCC is as shown in Fig. 2. The MOS transistors used are matched and 0.25 micron technology has been used.

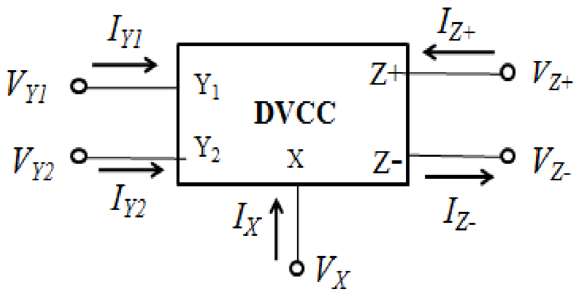

Fig 1: Symbol representing the dual output DVCC

3. IMPLEMENTATION OF THE DVCC FILTER

The implemented voltage-mode multifunctional filter [11] is illustrated in Fig. 3. The analysis of the circuit provides us with the following equations (2), (3) and (4), these equations are lowpass, bandpass and highpass filter transfer functions respectively.

$$\frac{V_{01}}{V_{IN}} = \frac{\frac{1}{R_1R_2C_1C_2}}{s^2+s\left(\frac{1}{R_1C_2}+\frac{1}{R_2C_2}\right)+\frac{1}{R_1R_2C_1C_2}} \qquad (2)$$

$$\frac{V_{02}}{V_{IN}} = \frac{(-s)\frac{1}{R_1C_2}}{s^2+s\left(\frac{1}{R_1C_2}+\frac{1}{R_2C_2}\right)+\frac{1}{R_1R_2C_1C_2}} \qquad (3)$$

$$\frac{V_{03}}{V_{IN}} = \frac{rs^2}{s^2+s\left(\frac{1}{R_1C_2}+\frac{1}{R_2C_2}\right)+\frac{1}{R_1R_2C_1C_2}} \qquad (4)$$

$$\text{where } r = \frac{R_3}{R_1} \qquad (5)$$

The resonant angular frequency ωo, and the quality factor, Q, are given by:

$$\omega o = \frac{1}{\sqrt{R_1R_2C_1C_2}} \qquad (6)$$

$$Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1+R_2C_1} \qquad (7)$$

Equation 6 clearly indicates that the change in cut-off frequency can be done only if passive component are change. Hence the limitation of this circuit is that for a given set of passive elements the circuit can work for only a particular cut-off frequency. In the next section a block DC-DVCC is discussed which eliminates this limitation and the frequency of this circuit could be digitally controlled.

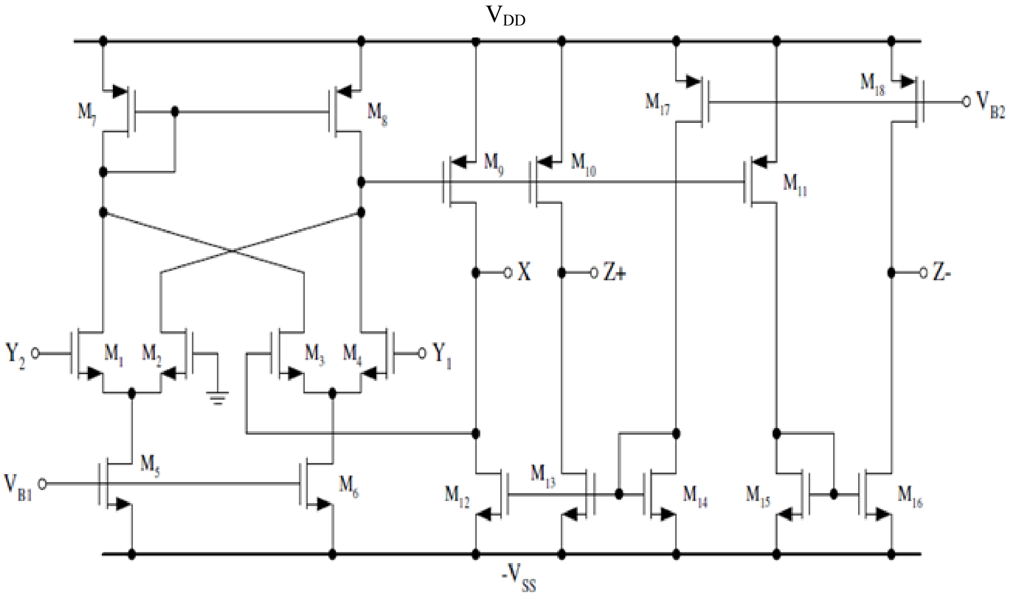

Fig 2: CMOS realization of the dual output DVCC [12]

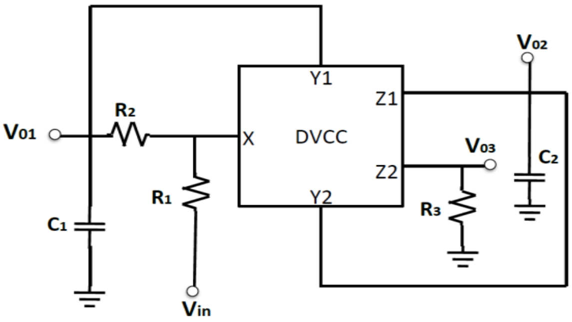

Fig 3: Circuit diagram of the multifunction biquadratic filter [11]

We can see that lowpass, bandpass and highpass functions can be simultaneously realized without changing the circuit configuration. Also, for R_1=R_3, by adding lowpass and highpass outputs, the transfer function can be re-organized to give a band reject filter transfer function as follows:

$$\frac{V_{BR}}{V_{IN}} = \frac{V_{03}+V_{01}}{V_{IN}} = \frac{rs^2+\frac{1}{R_1R_2C_1C_2}}{s^2+s\left(\frac{1}{R_1C_2}+\frac{1}{R_2C_2}\right)+\frac{1}{R_1R_2C_1C_2}} \qquad (8)$$

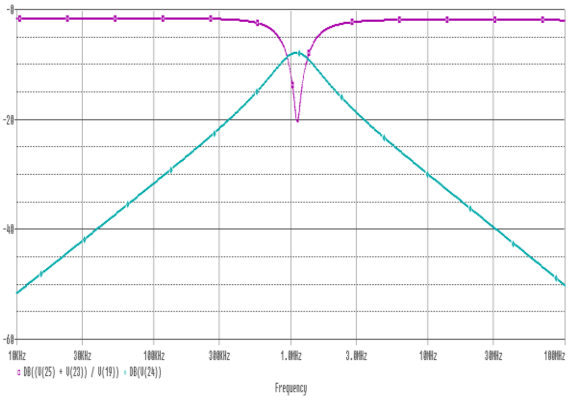

Fig. 4(a). Simulated Bandpass and Bandreject responses

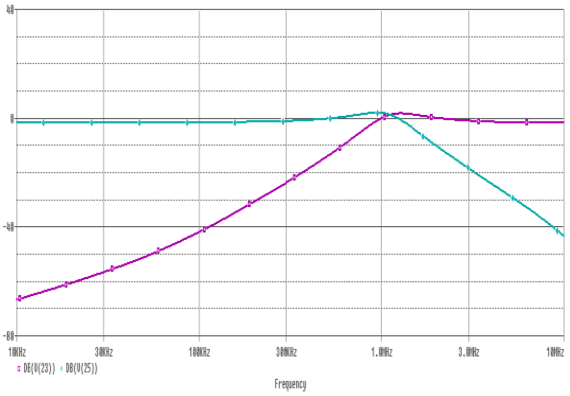

Fig.4(b): Simulated Lowpass and Highpass responses

Table 1. Aspect ratios of the cmos transistors of the DVCC [12]

Transistors	W (µm)	L (µm)
M_1-M_4	1	0.8
M_5-M_6	24.2	0.8
M_7-M_8	6.8	0.8
M_9-M_{11} , M_{17}	18.6	0.6
M_{12}-M_{14}	25	0.8
M_{15}	19.6	0.8
M_{16}	18	0.8
M_{18}	20	0.6

In simulations, using PSPICE DVCC was realized by the CMOS implementation illustrated in Fig. 2 using TSMC 0.25-µm process parameters. The aspect ratios of the CMOS transistors used for implementing DVCC are presented in Table 1. The supply voltages were given value V_{DD} =–V_{SS} = 2 V and the biasing voltages were assigned as V_{B1} =–1.32 V and V_{B2} = +0.7 V. The circuit was designed for fo = ωo/2π = 1 MHz and Q = 1.58 by choosing R_1 = R_2 =R_3=10 kΩ and C_1 =5 pF, C_2 = 50 pF. The responses of the multifunctional filter for the above configuration are shown in Fig. 4(a) and (b). The results agree with the theoretical analysis.

4. DC- DVCC

To introduce the controllability in the multifunctional filter we have used a digitally controlled DVCC (DC-DVCC) shown in Fig. 5. The modified terminal characteristics for the same are as follows:

$$\begin{pmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z+} \\ I_{Z-} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & k & 0 & 0 \\ 0 & 0 & -k & 0 & 0 \end{pmatrix} \begin{pmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_{Z+} \\ V_{Z-} \end{pmatrix} \qquad (9)$$

Where: $k = \frac{I_Z}{I_X}$

For obtaining the digital control in the DVCC current summing networks (CSNs) are employed at the Z (Z+ and Z-) terminals for controlling the current transfer gain parameter k. A variation from 1 to (2^n – 1) is observed in the gain parameter k, where n signifies the number of transistor arrays. The modified circuit of DVCC with the transistors arrays is as shown in Fig.5. The CSN consists n transistor pairs, the aspect ratios of whose PMOS and NMOS transistors respectively are given by:

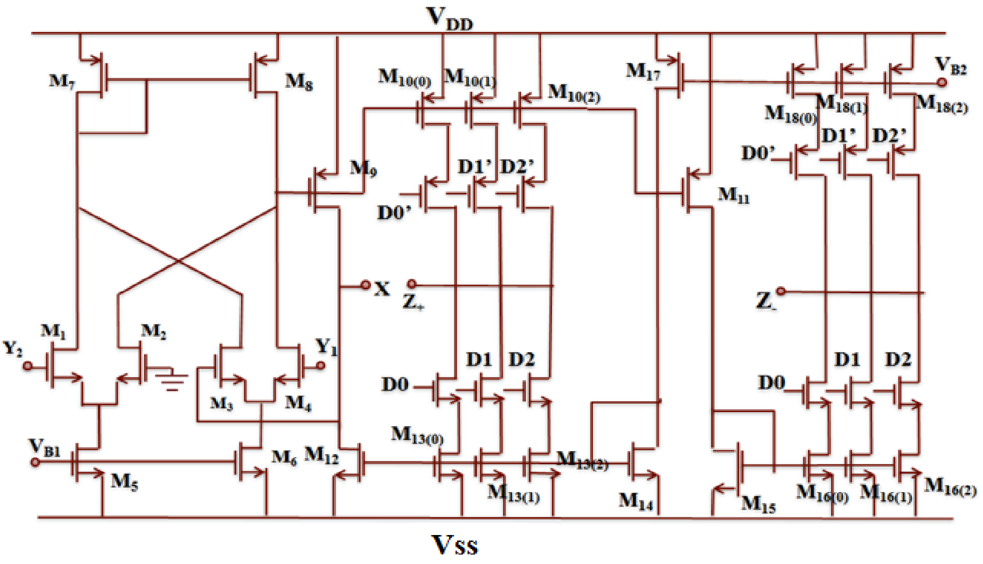

Fig.5: CMOS realization of the digitally programmable DVCC with gain *k*

$$\left(\frac{W}{L}\right)_i = 2^i \left(\frac{W}{L}\right)_9 \qquad (10)$$

$$\left(\frac{W}{L}\right)_i = 2^i \left(\frac{W}{L}\right)_{12} \qquad (11)$$

The current at the Z terminal is assumed to be flowing out of the DC-DVCC and can be expressed by:

$$I_Z = \sum_{i=0}^{n-1} d_i 2^i (I_9 - I_{12}) \qquad (12)$$

Therefore, the proposed DC-DVCC provides a current transfer gain, k equal to:

$$k = \frac{I_Z}{I_X} = \frac{\sum_{i=0}^{n-1} d_i 2^i (I_9 - I_{12})}{(I_9 - I_{12})} = \sum_{i=0}^{n-1} d_i 2^i \qquad (13)$$

Where d_i are the bits applied to the i-th branch in the CSN. Now the current flow in a particular branch is enabled or disabled depending upon whether d_i is a logic 1 or logic 0 [13].

5. DIGITALLY CONTROLLED S.I.M.O. FILTER

In this section the proposed digitally controlled voltage-mode multifunctional biquadratic filter is presented as shown in Fig. 6. The introduction of the DC-DVCC comprising of CSN modifies the expression of pole-frequency ω_0 of the multifunctional filter. The expressions for the digitally controlled filter responses can now be expressed as:

$$\frac{V_{01}}{V_{IN}} = \frac{\frac{k}{R_1 R_2 C_1 C_2}}{s^2 + ks\left(\frac{1}{R_1 C_2} + \frac{1}{R_2 C_2}\right) + \frac{k}{R_1 R_2 C_1 C_2}} \qquad (14)$$

$$\frac{V_{02}}{V_{IN}} = \frac{(-sk)\frac{1}{R_1 C_2}}{s^2 + ks\left(\frac{1}{R_1 C_2} + \frac{1}{R_2 C_2}\right) + \frac{k}{R_1 R_2 C_1 C_2}} \qquad (15)$$

$$\frac{V_{03}}{V_{IN}} = \frac{rks^2}{s^2 + ks\left(\frac{1}{R_1 C_2} + \frac{1}{R_2 C_2}\right) + \frac{k}{R_1 R_2 C_1 C_2}} \qquad (16)$$

$$\text{where } k = \frac{I_Z}{I_X} \text{ and } r = \frac{R_3}{R_1}$$

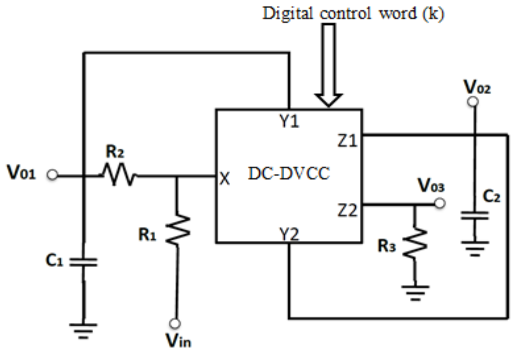

Fig.7: Proposed Digitally controlled voltage-mode multi-function biquadratic filter

Cutoff frequency (ω_o) and quality factor (Q) of the controlled filter can be expressed as:

$$\omega o = \frac{\sqrt{k}}{\sqrt{R_1 R_2 C_1 C_2}} \qquad (17)$$

$$Q = \frac{1}{\sqrt{k}} \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 C_1 + R_2 C_1} \qquad (18)$$

6. SIMULATION RESULTS

The proposed digitally controlled multifunctional biquadratic filter circuit in Fig. 6 has been simulated and all the results are verified with PSPICE. Fig.7, 8 and 9 are the simulated responses obtained for the low-pass, high pass, and band-pass filters respectively keeping the digital control word [d_2 d_1 d_0] = [0 1 0] and [1 0 1].The 3-bit digital control word is varied from [0 0 1] to [111] to obtain the variation in the cut off frequency of the multifunction filter. Figures 10 (a), (b) and (c) are the plots showing the variation in the cut off frequency with the control word.

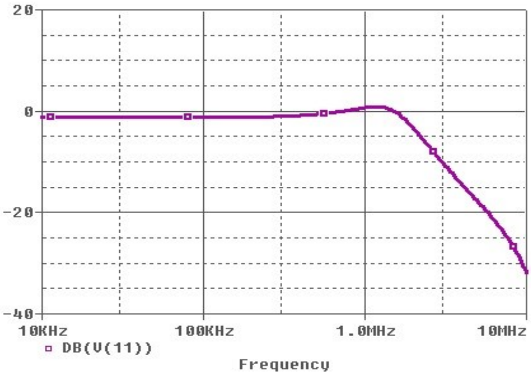

Fig. 7(a): Simulated magnitude response (in dB) for low pass filter with control word [d_2 d_1 d_0 = 0 1 0] selected

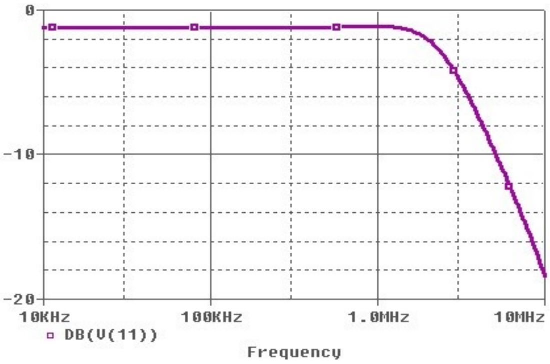

Fig. 7(b): Simulated magnitude response (in dB) for low-pass filter with k [d_2 d_1 d_0 = 1 0 1]

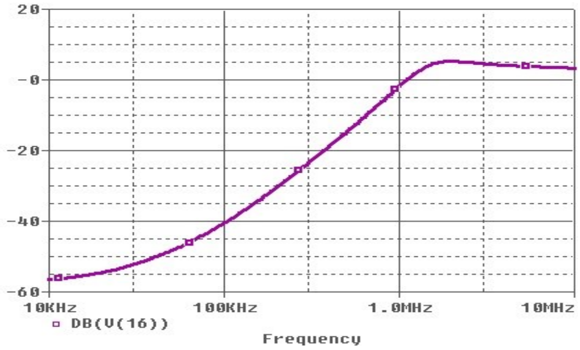

Fig. 8(a): Simulated magnitude response (in dB) for high pass filter with control word [d_2 d_1 d_0 = 0 1 0] selected

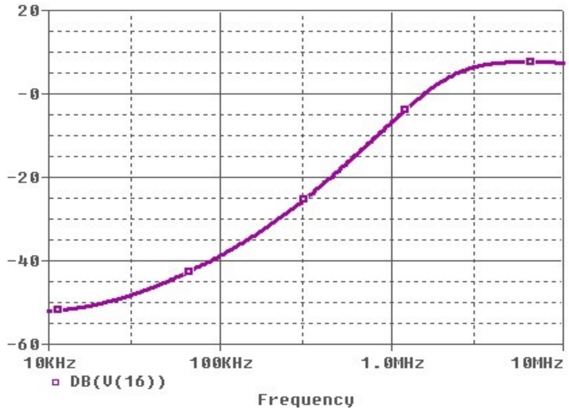

Fig. 8(b): Simulated magnitude response (in dB) for high pass filter with control word [d_2 d_1 d_0 = 1 0 1] selected

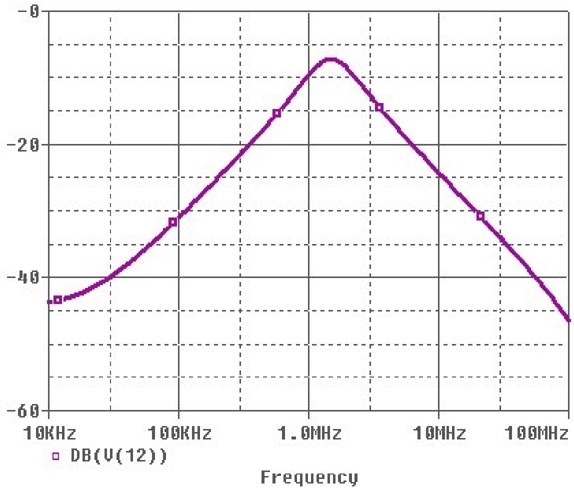

Fig. 9(a): Simulated magnitude response (in dB) for band pass filter with control word [d_2 d_1 d_0 = 0 1 0] selected

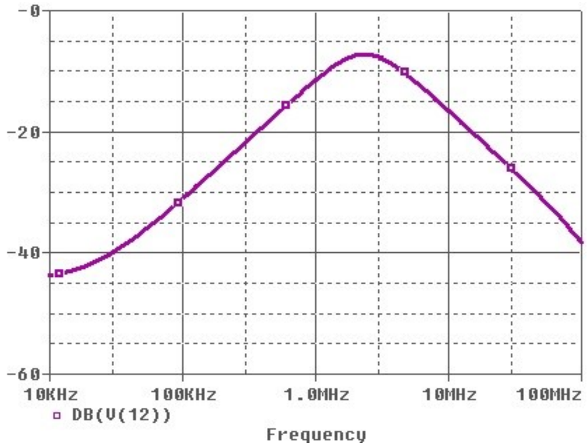

Fig. 9(b): Simulated magnitude response (in dB) for band pass filter with control word [d_2 d_1 d_0 = 0 1 0] selected

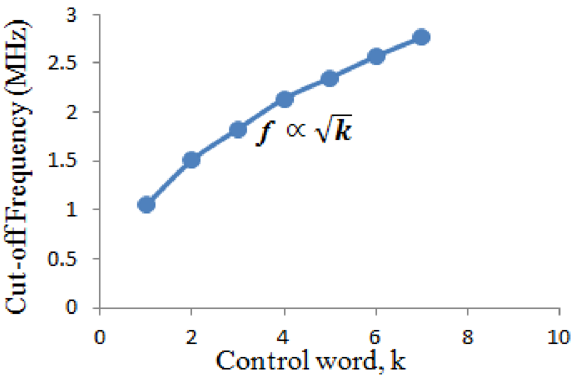

Fig. 10(a): Variation of cut-off Frequency of LPF with digital control word

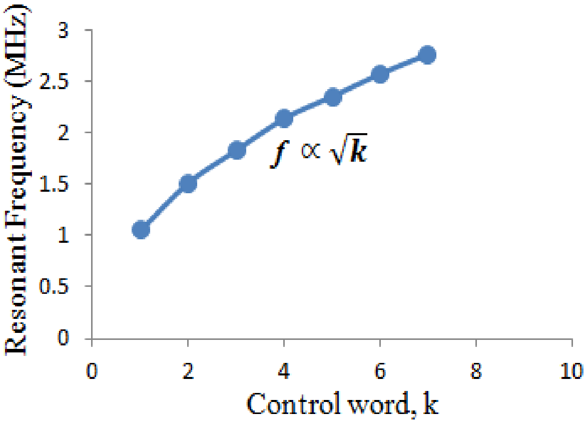

Fig. 10(b). Variation of cut-off Frequency of BPF with digital control word

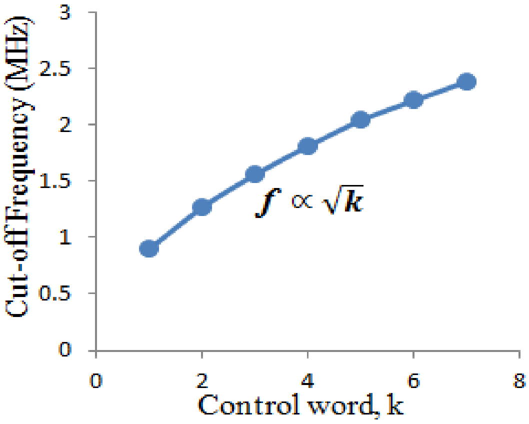

Fig. 10(c): Variation of cut-off Frequency of HPF with digital control word

Table 2. Variation in cut-off frequencies with the control word

Control word, k	Cut-off frequency of LPF (MHz)	Resonant frequency of BPF (MHz)	Cut-off frequency of HPF (MHz)
1	0.901	0.901	0.901
2	1.269	1.269	1.269
3	1.561	1.561	1.561
4	1.812	1.812	1.812
5	2.041	2.041	2.041
6	2.216	2.216	2.216
7	2.385	2.385	2.385

7. CONCLUSIONS

In this paper, a digitally controlled voltage-mode multifunctional biquadratic filter based on single DVCC was presented. Digital control was achieved by the variation of 3-bit digital control word using a Current summing network (transistor arrays). Digitally controlled low-pass, high-pass and band-pass filter responses were obtained. PSPICE simulations were carried out to verify the working of the digitally controlled multifunctional biquadratic filter. It is observed that the cut-off frequency varies from 1.267 MHz to 3.072 MHz for low-pass filter, 901 kHz to 2.385 MHz for high-pass filter, 1.051 MHz to 2.765 MHz for band-pass filter by varying the digital control word from [0 0 1] to [1 1 1] (recorded in Table 2), without changing the value of any of the passive components i.e. resistors and capacitors being used in the design. The significant feature of this circuit is that it uses a single DVCC block and minimum number of passive components. The digital controls for the cut-off frequency of the respective filters are in full conformity with the mathematical calculations.

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