Triple DVCC based Digitally Programmable Biquadratic Filter

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ABSTRACT
In this paper, a digitally programmable single input multi-output voltage mode multifunctional biquadratic filter has been presented. The circuit employs three differential voltage current conveyors (DVCC), two grounded capacitors, two grounded and two floating resistors. The digital re-configurability is obtained using a current-summing network (CSN). Cut-off frequency is controlled and varied with the help of a 3–bit digital control word. PSPICE simulations using TSMC 0.25µCMOS technology have been performed to validate the theoretically predicted results.

Keywords
Voltage-mode; Differential Voltage Current Conveyor (DVCC); multifunctional filter; digitally programmable circuits; cut off frequency

1. INTRODUCTION
In this modern world and with the ever increasing technology and demands for betterment the current mode circuits came into attention. Although many types of signal processing applications have moved towards the digital domain but analog circuits still hold their importance and pave the path between real world and digital systems. They also play a fundamental role in many complex and high performance systems. [1-3]

Current conveyors (CCs) came as a new and significant class of circuits in analog electronics field. The analog filters are used in a large variety of applications. These include signal separation and noise rejection in many industrial circuits, shaping of audio signal and enhancing the sound, providing a feedback for phase and amplitude control in case of servo loops, separating channels and enhancing the signal in communication are some of its significant examples. The increasing demand of these applications and with the advantages of current mode circuits led to a continuous development in this area.

From Current Conveyor Second Generation (CCII) to Differential Difference Current Conveyor (DDCC) and finally to Differential Voltage Current Conveyor (DVCC) proves it. [4-10] In this paper, the circuit proposed in [11] by Jiun-Wei Horng, Chun-Li Hou, Chun-Ming Chang, Hung-Pin Chou and Chun-Ta Lin has been used to design and implement a digitally programmable voltage-mode multifunctional biquadratic filter. Various filters like Low-pass, band-pass and high-pass can be realized together which further makes the circuit more versatile. Using the grounded capacitor enhances the circuit suitability for integration as grounded capacitor in the circuit can compensate for the stray capacitances at their nodes.

PSPICE simulations of the CMOS based programmable multifunctional filter are performed to demonstrate results.

2. DVCC
As shown in Fig. 1, the DVCC is an active building block having five terminals. Matrix below shows the characteristics of these terminals: [12]

$$\begin{pmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z+} \\ I_{Z-} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_{Z+} \\ V_{Z-} \end{pmatrix} \quad (1)$$

$$V_X = V_{Y1} - V_{Y2} \quad (1.1)$$

$$I_{Z+} = I_X = - I_{Z-} \quad (1.2)$$

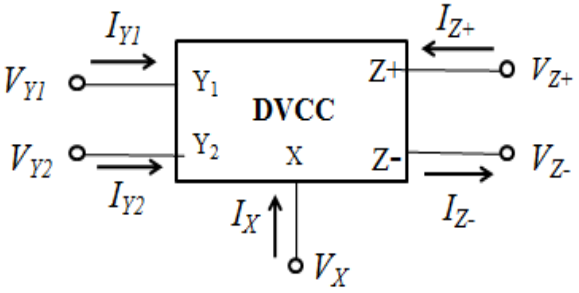

Fig.1. Symbolic representation of the dual output DVCC [12]

Ideally a DVCC exhibits very low or negligible input resistance at X terminal and both the Y terminals as well as the Z terminal have infinite resistance. The output current's flow follows the direction of the input current. Either both the terminal currents flow into the block or out of the block. The CMOS implementation of DVCC is as shown in Fig. 2.

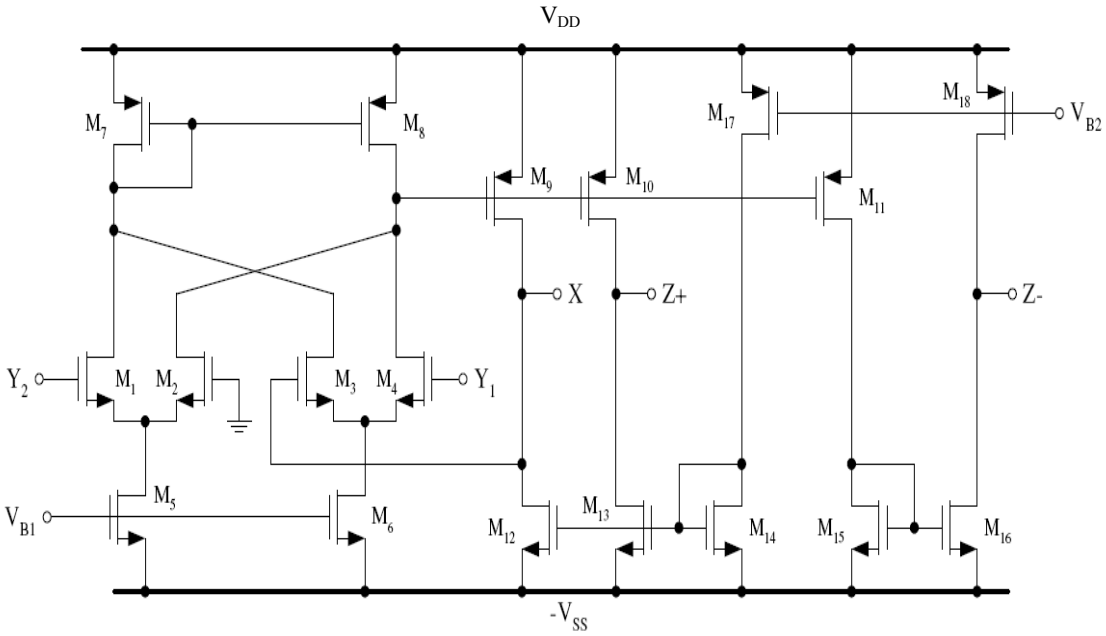

Fig.2. CMOS realization of the dual-output DVCC [12]

3. IMPLEMENTATION OF THE FILTER

The implemented voltage-mode multifunctional filter [11] is illustrated in Fig. 3. The analysis of the circuit yields the following equations (2), (3) and (4)

$$\frac{V_{01}}{V_{IN}} = \frac{\frac{G_1 G_2}{C_1 C_2}}{s^2 + s\frac{G_1 G_2}{G_3 C_2} + \frac{G_1 G_2}{C_1 C_2}} \quad (2) \qquad \text{(Lowpass)}$$

$$\frac{V_{02}}{V_{IN}} = \frac{-s\frac{G_1}{C_2}}{s^2 + s\frac{G_1 G_2}{G_3 C_2} + \frac{G_1 G_2}{C_1 C_2}} \quad (3) \qquad \text{(Bandpass)}$$

$$\frac{V_{03}}{V_{IN}} = \frac{-s^2}{s^2 + s\frac{G_1 G_2}{G_3 C_2} + \frac{G_1 G_2}{C_1 C_2}} \quad (4) \qquad \text{(Highpass)}$$

$$\frac{V_{04}}{V_{IN}} = \frac{s^2 + \frac{G_1 G_2}{C_1 C_2}}{s^2 + s\frac{G_1 G_2}{G_3 C_2} + \frac{G_1 G_2}{C_1 C_2}} \quad (5) \qquad \text{(Bandreject)}$$

The resonant angular frequency $\omega_\circ$, and the quality factor, Q, are given by:

$$\omega_\circ = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \quad (6)$$

$$Q = G_3 \sqrt{\frac{C_2}{C_1 G_1 G_2}} \quad (7)$$

In simulations, using PSPICE the DVCC was realized by the CMOS implementation shown in Fig. 2 using TSMC 0.25-µm process parameters. The aspect ratios of the CMOS transistors of the DVCC are presented in Table 1.

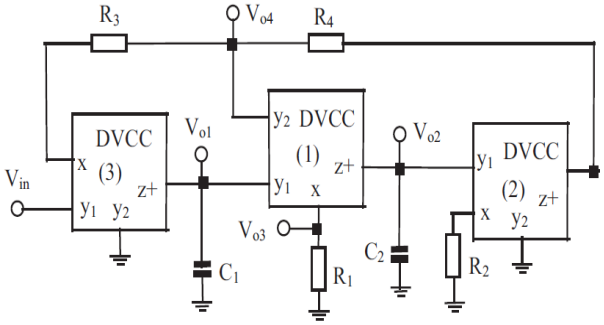

Fig. 3. Circuit diagram of the filter [11]

V_{DD} =−V_{SS} = 2 V which are the supply voltages and V_{B1} =−1.32 V and V_{B2} = +0.7 V which are two biasing voltages. The circuit was designed for fo = ωo/2π = 99.5 kHz and Q = 1 by choosing R_1 = R_2 =R_3= R_4=16 kΩ and C_1 = C_2 = 100 pf. Responses obtained are shown in Fig. 4(a), (b) are in conformity with the theoretical analysis.

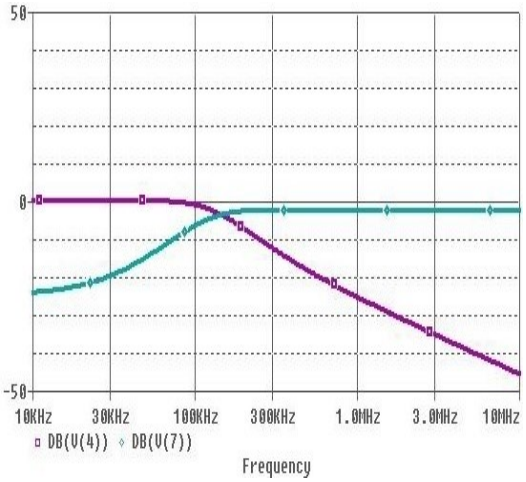

Fig. 4(a). Simulated Lowpass and Highpass responses

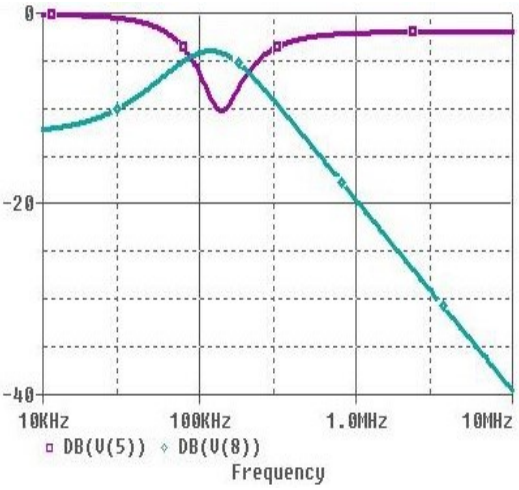

Fig. 4(b). Simulated Bandpass and Bandreject responses

Table 1. Aspect ratios of the CMOS transistors of the DVCC [1]

Transistors	W (µm)	L(µm)
M_1-M_4	1	0.8
M_5-M_6	24.2	0.8
M_7-M_8	6.8	0.8
M_9-M_{11} , M_{17}	18.6	0.6
M_{12}-M_{14}	25	0.8
M_{15}	19.6	0.8
M_{16}	18	0.8
M_{18}	20	0.6

4. DIGITALLY PROGRAMMABLE DVCC

To introduce the programmability in the multifunctional filter we have used a digitally controlled DVCC (DC-DVCC) shown in Fig.5. The modified terminal characteristics for the same are as follows:

$$\begin{pmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z+} \\ I_{Z-} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & k & 0 & 0 \\ 0 & 0 & -k & 0 & 0 \end{pmatrix} \begin{pmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_{Z+} \\ V_{Z-} \end{pmatrix} \quad (8)$$

Where: $k = \frac{I_Z}{I_X}$

For obtaining the digital control in the DVCC current summing networks (CSNs) are employed at the Z (Z+ and Z-) terminals for controlling the current transfer gain parameter k and it can be varied from 1 to $(2^n - 1)$. Here n is the number of transistor arrays. The modified circuit of DVCC with the transistors arrays is as shown in Fig. 5. The CSN consists of n transistor pairs, the aspect ratios of whose PMOS and NMOS transistors respectively are given by:

$$\left(\frac{W}{L}\right)_i = 2^i \left(\frac{W}{L}\right)_9 \quad (9)$$

$$\left(\frac{W}{L}\right)_i = 2^i \left(\frac{W}{L}\right)_{12} \quad (10)$$

Further, the Z terminal current is assumed to be flowing out of the block and can be expressed as:

$$I_Z = \sum_{i=0}^{n-1} d_i 2^i (I_9 - I_{12}) \quad (11)$$

Therefore, the proposed DC-DVCC provides a current transfer gain, k equal to:

$$k = \frac{I_Z}{I_X} = \frac{\sum_{i=0}^{n-1} d_i 2^i (I_9 - I_{12})}{(I_9 - I_{12})} = \sum_{i=0}^{n-1} d_i 2^i \quad (12)$$

Where di are the bits applied to the i-th branch in the CSN. Now the current flow in a particular branch is enabled or disabled depending upon whether di is a logic 1 or logic 0. [13]

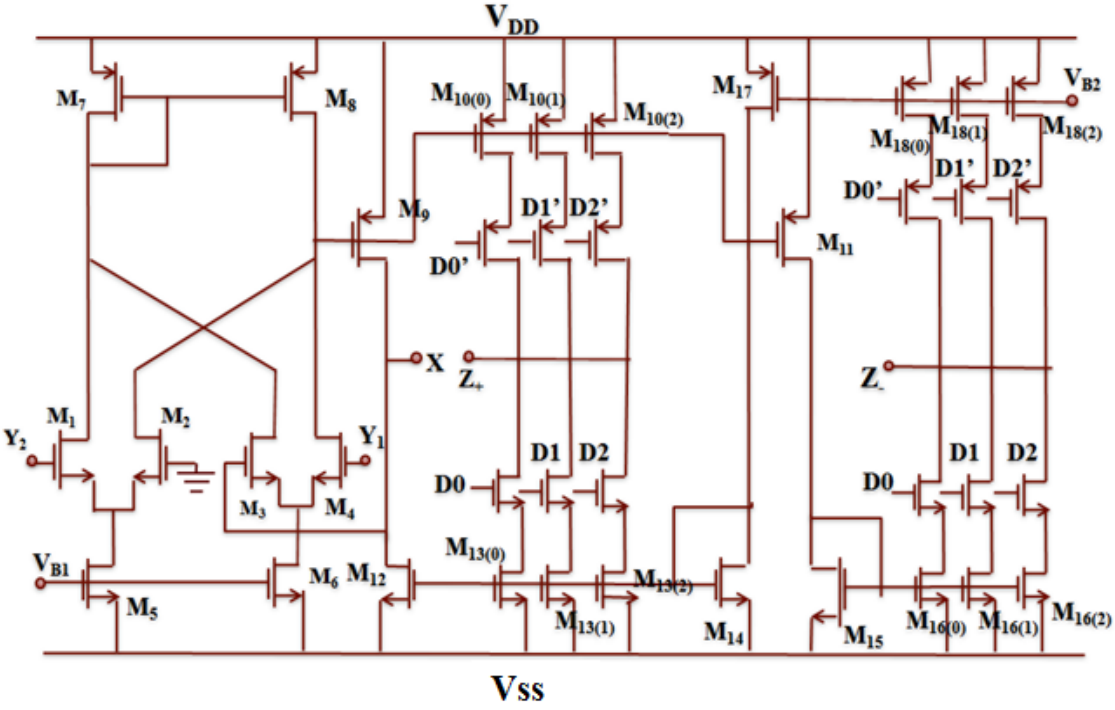

Fig. 5. CMOS realization of the digitally programmable DVCC with gain k

5. DIGITALLY PROGRAMMABLE MULTIFUNCTIONAL FILTER

In this section the proposed digitally programmable voltage-mode multifunctional biquadratic filter has been presented as shown in Fig. 6

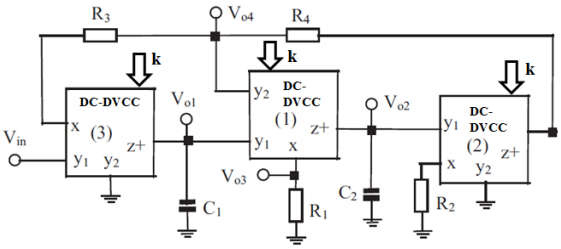

Fig.6. Proposed Digitally controlled voltage-mode multi-function biquadratic filter

The introduction of the DC-DVCC comprising of CSN modifies the expression of pole-frequency ω_0 of the multifunctional filter. The expressions for the digitally programmable filter responses can now be expressed as:

$$\frac{V_{01}}{V_{IN}} = \frac{k^3\frac{G_1\,G_2}{C_1\,C_2}}{s^2+sk^2\frac{G_1\,G_2}{G_3C_2}+k^3\frac{G_1\,G_2}{C_1\,C_2}} \quad (13)$$

$$\frac{V_{03}}{V_{IN}} = \frac{-s^2}{s^2+sk^2\frac{G_1\,G_2}{G_3C_2}+k^3\frac{G_1\,G_2}{C_1\,C_2}} \quad (14)$$

$$\frac{V_{02}}{V_{IN}} = \frac{-sk\frac{G_1}{C_2}}{s^2+sk^2\frac{G_1\,G_2}{G_3C_2}+k^3\frac{G_1\,G_2}{C_1\,C_2}} \quad (15)$$

Resonant angular frequency ωo, and the quality factor Q are given as:

$$\omega_{\circ} = k^{3}/_{2}\sqrt{\frac{G_1\,G_2}{C_1\,C_2}} \quad (16)$$

$$Q = G_3\sqrt{\frac{C_2}{k\,C_1G_1\,G_2}} \quad (17)$$

6. SIMULATION RESULTS

The proposed digitally controlled multifunctional biquadratic filter circuit in Figure 6 has been simulated and all the results are verified using PSPICE. Fig. 7(a) and 7(b) shows the simulated responses obtained for the low-pass, high pass, and band-pass filters keeping the digital control word $[d_2\ d_1\ d_0] = [0\ 1\ 0]$ and $[1\ 0\ 1]$.The 3-bit digital control word is varied from [0 0 1] to [1 1 1] to obtain the variation in the cut off frequency of the multifunction filter. These simulated were recorded in Table 2 and were then plotted. Fig. 8(a), (b)

and (c) are the plots showing the variation in the cut off frequency with the control word. It is to be observed that the cut-off frequency showed a three by two variation with respect to the digital control word (k). Cut-off frequency varies from 128.03 kHz to 1.08 MHz for low-pass filter, 104.13 kHz to 1.36 MHz for high-pass filter, 112.62 kHz to 1.177 MHz for band-pass filter by varying the digital control word from [0 0 1] to [1 1 1], without changing the value of any of the passive components i.e. resistors and capacitors being used in the design.

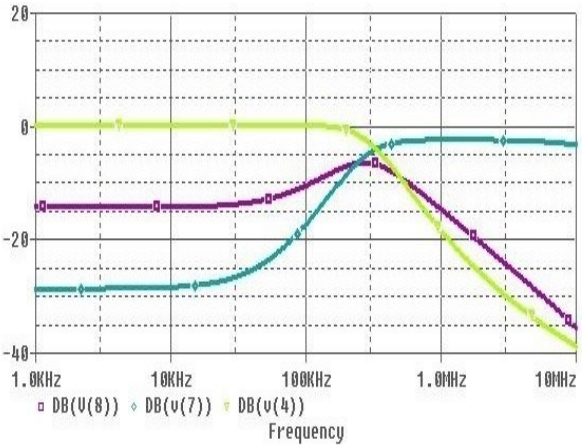

Fig. 7(a). Simulated magnitude responses (in dB) for control word [d_2 d_1 d_0 = 0 1 0]

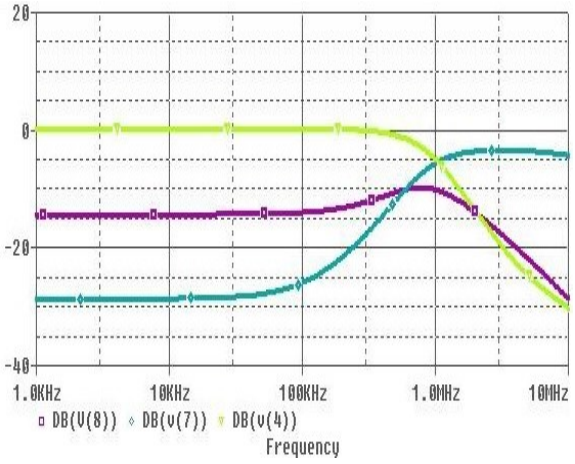

Fig. 7(b). Simulated magnitude responses (in dB) for control word [d_2 d_1 d_0 = 1 0 1]

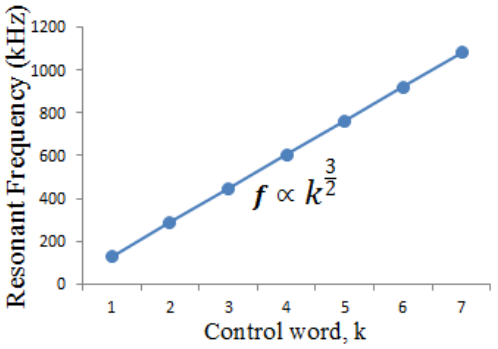

Fig. 8(a). Variation of Resonant Frequency of BPF with digital control word

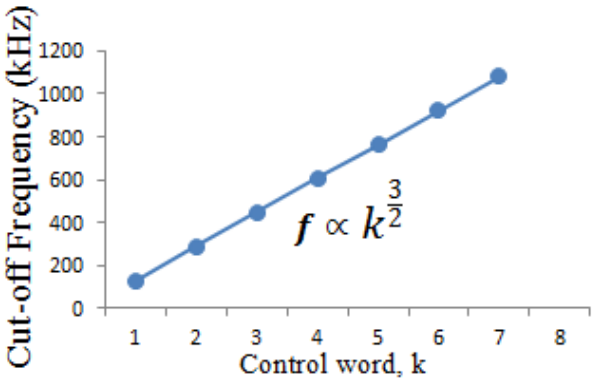

Fig. 8(b). Variation of Cut-off Frequency of HPF with digital control word

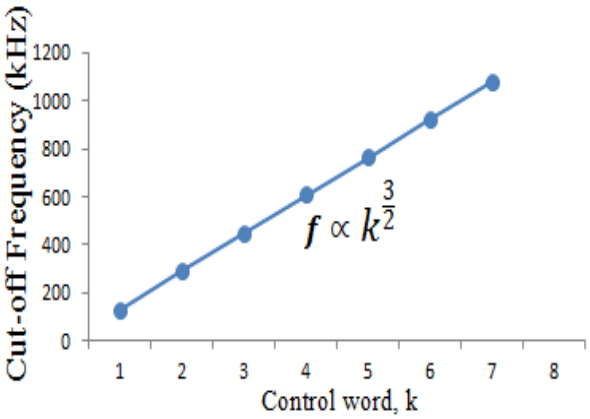

Fig. 8(c). Variation of cut-off Frequency of LPF with digital control word

Table 2. Simulated values of the variation in cut-off frequency with the control word

Control word, k	Cut-off frequency of LPF (kHz)	Resonant frequency of BPF (kHz)	Cut-off frequency of HPF (kHz)
1	128.04	112.619	104.137
2	288.994	270.557	273.059
3	447.593	438.466	470.631
4	605.610	617.053	682.987
5	763.274	794.328	903.970
6	921.355	977.963	1130.79
7	1080.08	1177.5	1361.23

7. CONCLUSION

In this paper, a digitally programmable voltage-mode multifunctional biquadratic filter based on three DVCCs was presented. Digital control has been achieved by the variation of 3-bit digital control word using a current summing network. Cut-off Frequency (ω_o) was digitally controlled by the 3-bit digital control word (k) and three by two variations with respect to the control word was observed. Standard low-pass, high-pass and band-pass filter responses were obtained simultaneously and their cut-off frequency was varied with digital control word. PSPICE simulations were carried out to verify the working of the digitally controlled multifunctional biquadratic filter. Thus as a result we obtained a multifunctional biquadratic filter giving low-pass, high-pass and band-pass filter responses of varying cut-off frequency at the same time without changing any of the circuit components or the topology. It is clear with the simulation figures shown that the filter responses have different cutoff frequencies for different k, Table 2 and plots 8 (a), (b) and (c), prove that the obtained results confirm the theoretical relations derived.

8. REFERENCES

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