A High Slew Rate Buffer Amplifier Employing MTCMOS Technique for Flat Panel Display

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ABSTRACT
This paper address a low power, high speed class AB buffer amplifier topology for liquid crystal display applications which offer a rail to rail common mode input range. The presented circuit use two comparator circuit inside it to enhance the slewing capabilities with a limited power consumption and it draw a very small quiescent current during static operation for rail to rail common mode input range. The circuit describes here the capacitive load behaviour with reduced distortion at the output node for swing characteristics. By applying MTCMOS (Multi threshold CMOS) reduction technique leakage current is reduced from 56nA to 52nA, power is reduced from 377.3 pW to 221pW, reduced slew rate and tranconductance of 4.363. A buffer circuit can run 1nF of load capacitance of achieving a rise time 800E-12, duty cycle is 4.5, Average group delay is 221E-3, unity gain frequency is 221.7E-3 and harmonic frequency is 1.532 at 20 Hz. The circuit has been demonstrated at 45 nm technology.

Keywords
Amplifier, Buffer circuit, Driver circuit, Settling time, Slew rate.

1. INTRODUCTION
A buffer amplifier circuit suggests a new compact reduced low power rail to rail configuration for large size LCD (Liquid crystal display) applications[1-2]. The proposed buffer circuit provides a phenomenal power efficiency improvement as comparison to the other reported solution [3]. The train drives of an LCD driving system contain the most significant role in achieving fast speed capabilities, high resolution and low power dissipation as well as the output buffer amplifiers essentially diagnose the speed, resolution, voltage swing and power consumption of the buffer amplifier circuit[4-5]. There are so many design challenges for the output buffer of an of an LCD (Liquid crystal display) driver [6]. The number of outputs to be achieved by using several column drivers of the buffer amplifier, so it should be used to minimize the system costs and increase the reliability of the circuit [7-8]. A flat panel display column driver three special requirements for the output buffer are to be needed. First a large number of output buffers are needed for a pixels column panel [9]. However it reduced the system cost and increases the reliability of the system. Second requirement is low power dissipation for the liquid crystal display (LCD) are commonly used in portable system that are battery powered [10-11].rd requirement is the input is always the step function of the output because the pixels are updated row by row [12]. Thus the power dissipation of the column driver is dependent on the image display [13]. In this paper we apply a reduction technique on the proposed circuit to reduced the size and getting a better power efficiency [14-15]. A variable bias current was used to reduce the power dissipation. However it wastes dynamic power when the grey level in a column driver does not change. Due to the finite response time of the comparator circuit final voltage is always smaller then the input voltage. Multi threshold CMOS (MTCMOS) is a variation of CMOS chip technology which has transistors with multiple threshold voltages (V_{th}) in order to optimize delay or power [16]. The V_{th} of a MOSFET is the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor. A common implementation of MTCMOS for reducing power makes use of sleep transistors. Logic is supplied by virtual power rail. Low V_{th} is used for fast switching speed and high V_{th} devices connecting the power rail and virtual power rails are turned on in active mode, off in sleep mode. High V_{th} devices are used as sleep transistors to reduce static leakage power.

2. PROPOSED CIRCUIT AND OPEREATION

2.1 Block Diagram
Figure Show the block diagram of the proposed two stage class AB buffer amplifier where C1and C2 are the current comparator which provide rail to rail input and output. MO1 and MO2 are the output complementary devices R_C represent the series resistors are mainly used for phase compensation at the output node. The load capacitance C_L is also connected to the output which is most portably used for swing characteristics of the output.

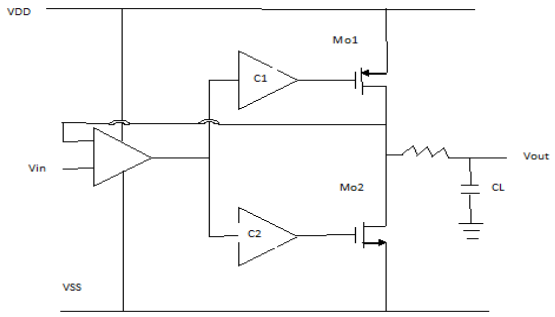

Fig.1:Block diagram of buffer amplifier

The basic comparator circuit are used to swing the output at the lightest difference between its inputs but there are many variations where the output is designed to switch between two other voltage values also. The input may be customized to make compares to an input voltage other then zero. The added comparators are used to reduce the power dissipation

2.2 Circuit Diagram
In the given circuit V_{out} is connected to the inverting terminal Vin-, while the input signal is applied to the non-inverting terminal Vin+. The circuit are divided into three main parts. MB1 to MB6 represent a biasing network, M1 to M14 represent a rail to rail stacked mirror differential amplifier,

MO1 to Mo2 represent a push pull output gain stages. Rc is series resistance are used to show the connection between amplifier output and the load capacitor. Finally the buffer amplifier is capable of driving a wide range of load capacitance; phase compensation is performed by introducing a left half plane zero, which is produced by the load capacitance C_L. The circuit consist of a comparator circuit which has been imposed in the buffer amplifier circuit for good swing characteristics having stronger current delivery for enhanced driving capability along with auxiliary transistors is apply to obtain the better driving of output without any distortion.

The transistor level enactment of the proposed output buffer is illustrated in fig.

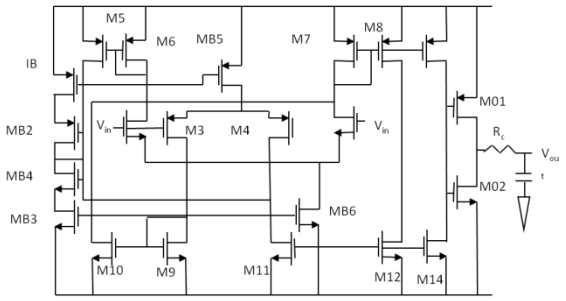

Fig.2:Circuit schematic of the proposed two stage rail to rail buffer amplifier

The current buffers are mainly use frequency compensation technique. In current buffer amplifier the most popular common gate or cascode transistor topology used as a positive current buffer. The basic configuration scheme of the buffer amplifier with zero compensation technique is shown below

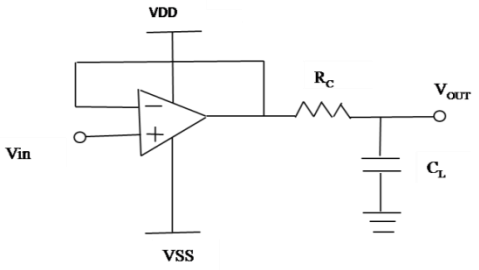

Fig.3:Buffer amplifier with zero compensation technique

To connect a capacitor across a high gain stage is the most significant compensation technique to improve the stability of the closed loop circuit. However to connect the capacitor in the output stage, a right half plane (RHP) zero is also created. The most commonly used method is dominant pole compensation which is also called as lag compensation. In open loop response pole is placed at an appropriate low frequency to reduce the gain of the amplifier to one (0db) for a frequency at or just below the location of the next highest frequency pole. This result the difference between open loop output phase and the phase response of a feedback network having no reactive elements never fall below -180^o while the amplifier has a gain of one or more , ensuring stability.

3. SIMPLIFIED IDENTICAL CIRCUIT REPRESENTATION OF THE PROPOSED OUTPUT DRIVING BUFFER

The simplified identical circuit of the proposed output buffer is depicted in fig.

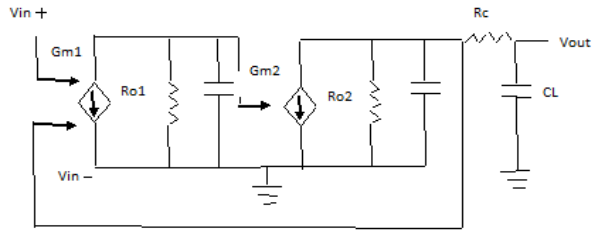

Fig.4:Simplified equivalent circuit of the proposed output driving buffer

Where gm1 and gm2 are the small signal tranconductance of the rail to rail stacked mirror differential amplifier and push pull output gain stages and Ro1and Ro2 represent the equivalent output resistances, Co1 and Co2 represent the output capacitances, whereas R_c represent the compensation resistor and C_L represent the equivalent capacitance of the LCD panel.

Assuming Ro1, Ro2 >> Rc and Co1, Co2 << C_L yields the following equations

$$A_V(S) = A_o \frac{1+\frac{S}{W_Z}}{\left(1+\frac{S}{W_{P1}}\right)\left(1+\frac{S}{W_{p2}}\right)\left(1+\frac{S}{W_{P3}}\right)} \quad (1)$$

Where Ao is the DC open loop gain is expressed by

$$A_0 = g_{m1}R_{01}g_{m2}R_{02} \quad (2)$$

While W_{P1} , W_{P2} and W_{p3} are the frequencies of the three amplifier real poles

$$W_{P1} = \frac{1}{(R_{o2}+R_C)C_L} \approx \frac{1}{R_{o2}C_L} \quad (3)$$

$$W_{P2} = \frac{1}{R_{o1}C_{o1}} \quad (4)$$

$$W_{P3} = \frac{1}{(R_{o2}\|R_C)C_{o3}} \approx \frac{1}{R_cC_{o3}} \quad (5)$$

And $W_Z$is the frequency of the left-plane zero.

$$W_Z = \frac{1}{R_cC_L} \quad (6)$$

Here we represent Wp3 is the third pole frequency; however the equivalent circuit has contain three poles, and its contribution to the amplifier transfer function is negligible. When we increase the value of Rc and CL the phase margin is automatically increases.

4. DESIGN ASPECTS AND OPERATING PRINCIPAL

The differential pair circuit are designed to draw the static current value ηIb, where Ib is the quiescent current which is supplied by the biasing network. The following relation is given below

$$\eta = \frac{(W/L)_{MB5}}{(W/L)_{MB1}} = \frac{(W/L)_{MB6}}{(W/L)_{MB4}} \quad (7)$$

The above specification requires the following design condition to be fulfilled.

$$\frac{(W/L)_8}{(W/L)_7} = \frac{(W/L)_{12} - \Delta(W/L)}{(W/L)_{11}} \quad (8)$$

$$\frac{(W/L)_{14}}{(W/L)_{11}} = \frac{(W/L)_{13} - \Delta(W/L)}{(W/L)_7} \quad (9)$$

In quiescent state, no input signal is applied, current flowing in both input pair transistor are ɳIb/2. Assuming M5-M6 and M9-M10 are the current mirror image, While M7 and M11, draw the same static current ɳIb, In the output NMOS device MO2 would be pulled down towards Vss. In PMOS device MO1 would pulled up towards Vdd. So we can say that at DC characteristics it consume no static power.

$$\Delta I_{13} = -g_{m1}\Delta V\frac{(W/L)_{13}}{(W/L)_7} \quad (10)$$

$$\Delta I_{14} = +g_{m1}\Delta V\frac{(W/L)_{14}}{(W/L)_{11}} \quad (11)$$

If ΔV is sufficiently large then we get the following expression

$$\Delta V > \frac{\eta I_B}{g_{m1}} \cdot \frac{\Delta(W/L)}{2(\frac{W}{L})_{13} - \Delta(W/L)} \quad (12)$$

$$\Delta I_8 = +g_{m1}|\Delta V\frac{(W/L)_8}{(W/L)_7} \quad (13)$$

$$\Delta I_{12} = -g_{m1}|\Delta V\frac{(W/L)_{12}}{(W/L)_{11}} \quad (14)$$

If the negative input step $\Delta V|$ is sufficiently large to get

$$\Delta V| > \frac{\eta I_B}{g_{m1}} \cdot \frac{\Delta(W/L)}{2(W/L)_{12} - \Delta(W/L)} \quad (15)$$

The power dissipated in the amplifier is of three types. The static power dissipation due to the dc bias current from the power supply of each transistor. The dynamic power dissipation due to the charging and discharging of the load capacitance and the direct path dissipation due to the current going through PMOS and NMOS transistor during transition.

The static energy dissipation for this circuit during a scanning period is expressed as

$$E_{static} = \frac{I_{bias}V_{DD}}{f_{scanning}} \quad (16)$$

Where Ibias is dc bias current, fscanning is the scanning frequency. So we can say that amplifier always consume static dissipation.

For dynamic power dissipation is expressed as

$$P_{charge} = (V_{DD} - V_o)I_L$$

$$= (V_{DD} - V_0)C_L\frac{dv_0}{dt} \quad (17)$$

The energy dissipated in PMOS is as

$$E_{charge} = \int_{V_L}^{V_H} P_{charge}\,dt$$

$$= C_L V_{DD}(V_H - V_L) - 1/2C_L({V_H}^2 - {V_L}^2) \quad (18)$$

And then the pdischarge is as

$$P_{discharge} = -V_0 I_L$$

$$= -V_0 C_L\frac{dv_0}{dt} \quad (19)$$

$$E_{discharge} = \int_{V_L}^{V_H} P_{discharge}\,dt$$

$$= 1/2C_L({V_H}^2 - {V_L}^2) \quad (20)$$

5. MTCMOS TECHNIQUE

In MTCMOS technique, transistor of low threshold voltage becomes disconnected from power supply by using threshold sleep transistor on the top and bottom of the logic circuit. Transistor having low threshold voltage is used to design logic as shown in fig. The sleep transistors are controlled by the sleep signal. During the active, the sleep signal is disserted, causing both Vt transistor to turn on and provide a virtual power and ground to the low Vt logic.

When the circuit is inactive sleep signal is asserted forcing both high Vt transistor to cut off and disconnect power lines from the low Vt logic. This result a very low sub threshold leakage current power to ground when the circuit is in standby mode. One drawback of this method is that portioning and sizing of sleep transistor is difficult for large circuits.

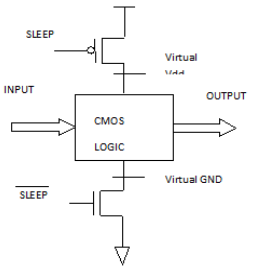

Fig.5:The proposed MTCMOS structure

6. NOISE, PHASE NOISE AND POLE ZERO ANALYSIS

The graphical presentation of noise (db), phase noise (dbc) and pole zero (db) versus frequency (Hz) is shown given below

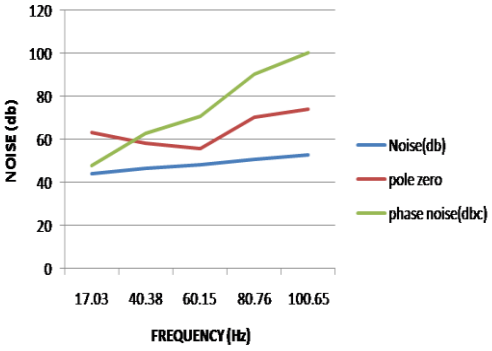

Fig.6: Parametric analysis of buffer amplifier with respect to frequency

The Harmonic Vs Frequency graph analysis is shown below in which the harmonic is in graded or degraded according to the frequency

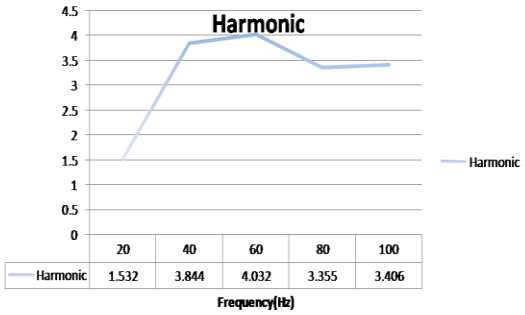

Fig.7:Harmonic analysis of buffer amplifier with respect to frequency

7. MODELLING AND SIMULATION

Figure8. show the reduced leakage current value by using MTCMOS (Multi threshold CMOS) reduction technique in which the value of reduced peak leakage current is 55.96nA is shown in given below at 45 nm technology by cadence virtuoso tool.

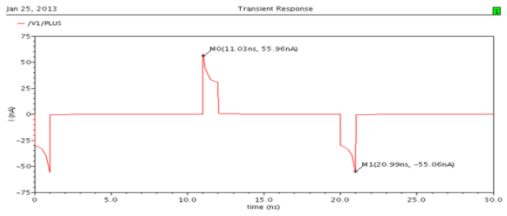

Fig.8:Reduced leakage current waveform using MTCMOS technique

Figure9. show the reduced power of peak value is 371.5pW by using MTCMOS(Multi threshold CMOS) technique to consume power for the maximum output at 45 nm technology is shown below by using cadence virtuso tool

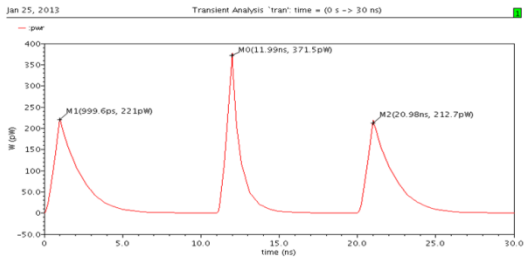

Fig.9:Active power waveform using MTCMOS technique

Figure10. Show the value of slew rate by using MTCMOS (Multi threshold CMOS) technique having the maximum peak value of 15.81nS is shown in given below at 45 nm technology by using cadence virtuoso tool.

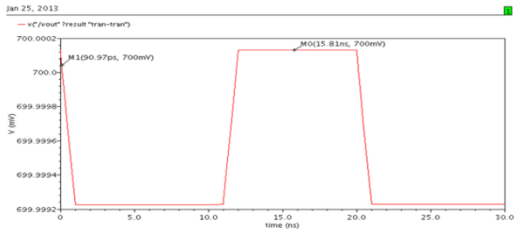

Fig.10:Slew rate analysis using MTCMOS technique

Figure11. Show the value of tranconductance by using MTCMOS (Multi threshold CMOS) technique having a value of 4.363×10^{-12} is given below at 45 nm technology by using cadence virtuoso tool.

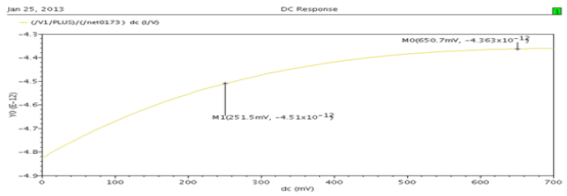

Fig.11:Waveform of tranconductance using MTCMOS technique

Figure12. Show the noise response curve having a value of 5.202db by using MTCMOS (Multi threshold CMOS) technique is shown below at 45 nm technology by using cadence virtuoso tool

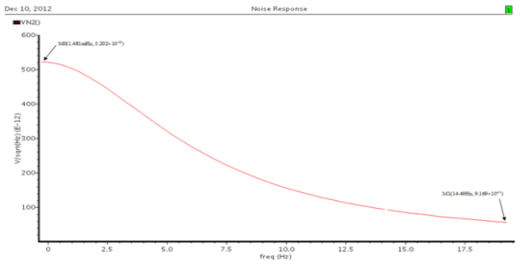

Fig.12:Noise response curve using MTCMOS technique

Figure13. Show the response curve of phase noise having a value of 52.75dbc/Hz by using MTCMOS (Multi threshold CMOS) technique at 45 nm technology by using cadence virtuoso tool.

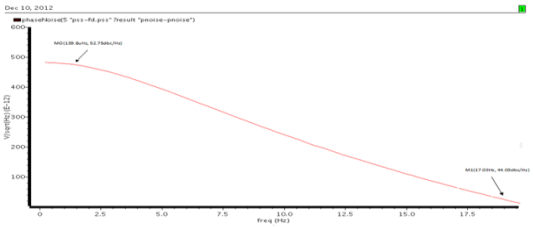

Fig.13:Phase noise response curve using MTCMOS technique

Figure14. Show the pole zero response curve of having a value of -55.5db by using MTCMOS (Multi threshold CMOS) technique in the circuit at 45 nm technology by using cadence virtuoso tool.

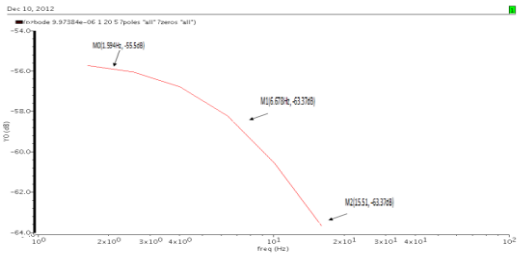

Fig. 14:Pole zero responsecurve using MTCMOS technique

8. TABLE

We have mention here a comparison table of a 45 nm technology and 45 nm technology with reduction technique of a given parameters are shown below.

S.N.	PARAMETERS	CONVENTIONAL	MTCMOS
01	Power (pW)	375.6	371.5
02	Slew rate (V/µ sec.)	15.81	15.41
03	Tranconductance (µs/µm)	9.83	4.51
04	Leakage current (nA)	56.66	55.96

Table1:CONVENTIONAL Vs MTCMOS

9. CONCLUSION

In this paper, we have observed a low power consumption, high speed, large output swing, high performance and offer a rail to rail common mode input range. The comparator circuit are added in this circuit for enhancing the driving capability of the rail to rail CMOS buffer amplifier in which it sense the rise and fall time of the input waveform and it consume the power dissipation. By using a reduction technique MTCMOS (multi threshold CMOS technique) reduced parameters are obtained. We observed noise 5.202, phase noise 52.75dbc/Hz and pole zero 55.57db at 45 nm technology. The proposed output buffer circuit is suitable for the application of flat panel display.

10. ACKNOWLEDGEMENT

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