Low Power Magnitude Comparator Circuit Design

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ABSTRACT
This paper presents a new low power 2-Bit magnitude comparator using full adder technique. The proposed magnitude comparator (PTL logic) has been compared with existing magnitude comparator (GDI technique). The performance analysis of both magnitude comparators is done on basis of power consumption with respect to input voltage, temperature, and frequency; using Tanner EDA tool version 12.6 at 45nm technology. The simulation results of proposed magnitude have shown remarkable performance in terms of power consumption, area and threshold loss in comparison to existing magnitude comparator. Thus proposed magnitude comparator can be viable option for low power application.

Keywords
Magnitude comparator, PTL logic, GDI technique, full adder and Low power.

1. INTRODUCTION
Now days, Low Power design have become a critical need of technologies due to high demand of portable devices. The magnitude comparator is one of the fundamental arithmetic components of digital system with many applications such as: Digital Signal Processors (DSP) for data processing, encryption devices and microprocessor for decoding instruction.

The simplest way to implement a comparator is by using trees structure with the all-n-transistor (ANT) dynamic CMOS logic. In this method three clock cycles is used to finish comparison which is not suitable for high performance processor design [1]. So to overcome this problem Huang et.al proposed a single cycle comparator based on priority-encoding algorithm [2]. The dynamic NAND fan-in of this technique has become the bottle neck of the performance of the comparator [3]. The parallel MSB checking algorithms, use NOR gate logic to improve performance by 22% faster. Further performance was improved by 28%with the help of MUX based structure [4] in comparison to [3]. This implementation achieves superior delay performance, at the cost of power dissipation and increases transistor count. Kim and Yoo [5] proposed comparator based on Bitwise Competition Logic (BCL) to achieve the lowest transistor count.

All the above mentioned works make use of dynamic logic to achieve high performance. But, Dynamic logic is not suitable for low power operation because the data activity factor of dynamic logic style is greater than static logic style [6]. Recent technology is moving toward low power, so this research is inclined toward static logic style. From last two decade static logic style has results many logic styles [7] and [8].The magnitude comparator was design, based on various topologies of static logic style is discussed by Anjuli and Satyajit Anand [9]. This magnitude comparator was design with help of conventional method but this method has a demerit; require large number of transistor to design circuit. So to overcome this problem a new technique evolved based on full adder to design magnitude comparator.

This paper is organized as follows: Section 2 describes the existing magnitude comparator and proposed magnitude comparator design based on full adder. Section 3 presents simulation and result of proposed and existing design. Finally, Section 4 concludes with some final remark and comment, this Section is followed by references.

2. 2-BIT MAGNTUDE COMPARATOR DESIGN

2.1 Existing Design
Let us assume two variable A and B of two bit binary number. Traditional method to determine whether A less than B (F1), A greater than B (F3) and A equal to B (F2), first step is to check the most significant bit.

Table 1. Truth Table of 2-Bit Magnitude Comparator

A1	A0	B1	B0	F2	F1	F3
0	0	0	0	1	0	0
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	0	1	1	0	0
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	1	0	0
1	0	1	1	0	1	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	1	0	0

If the most significant bit of A is greater than B then F3 is high, else if most significant bit of A is less than B then F1 is high. If both the condition is not true and the most significant bit of A and B is equal than, the check the next corresponding bit. Accordingly F1 and F3 bit will high and if both the bits are same then F2 output bit will be high. By using above

method truth table of 2-bit magnitude comparator is design (Table 1).

The logic diagram of 2-Bit magnitude comparator based on full adder consist of four XOR gate, two MUX, two AND gate and two NOT gate (Figure 1) [10]. When one of input applied to XOR gate is inverted, the act as an XNOR gate with respect to two original inputs. So to reduce the number of transistor the block shown in (Figure1) is replaced by XNOR gate. By using this logic diagram, schematic of 2-Bit magnitude comparator (Figure 2) is design with the help of GDI (Gate Diffusion Input) technique (30 transistors).

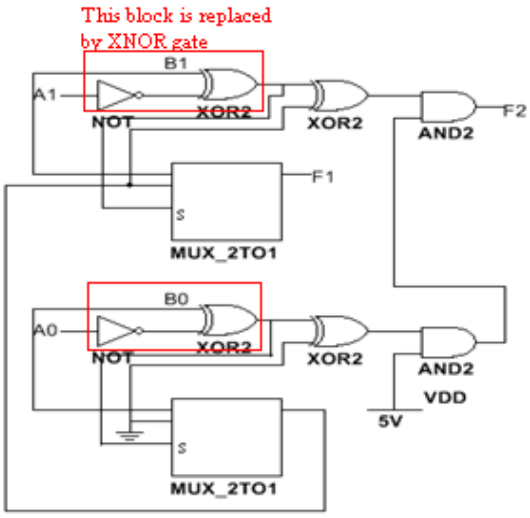

Fig 1: Logic Diagram of 2-Bit magnitude comparator using full adder

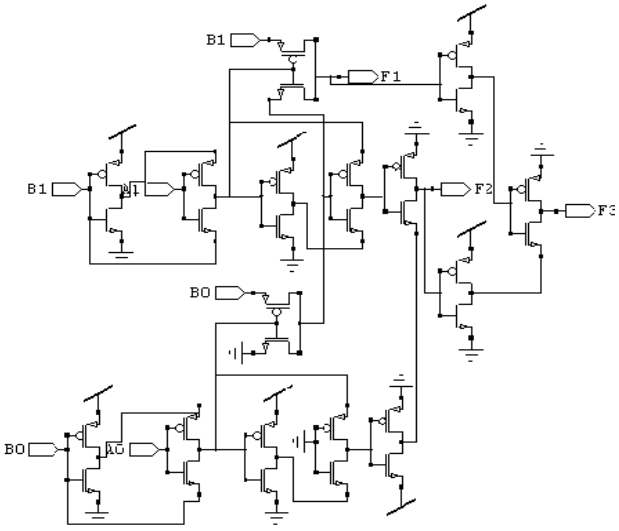

Fig 2: Schematic of 2-Bit magnitude comparator using GDI Technique

2.2 Proposed Design

GDI Technique suffers from some limitation like fabrication complexity in CMOS process and bulk connection [11] and [12]. Pass Transistor Logic (PTL) is the most popular logic style for low power circuit design [13]. It has advantage of: low power dissipation, high speed and lower interconnect effect due to small area required to design circuit. So schematic of 2-Bit magnitude comparator is constructed by using PTL logic with help of logic diagram based on full adder (Figure 3). The transistor count is reduced to 26 whereas magnitude comparator using GDI technique requires 30 transistors. Also threshold loss is improved from (13%-20%) existing magnitude to (7%-20%) proposed magnitude comparator using PTL logic.

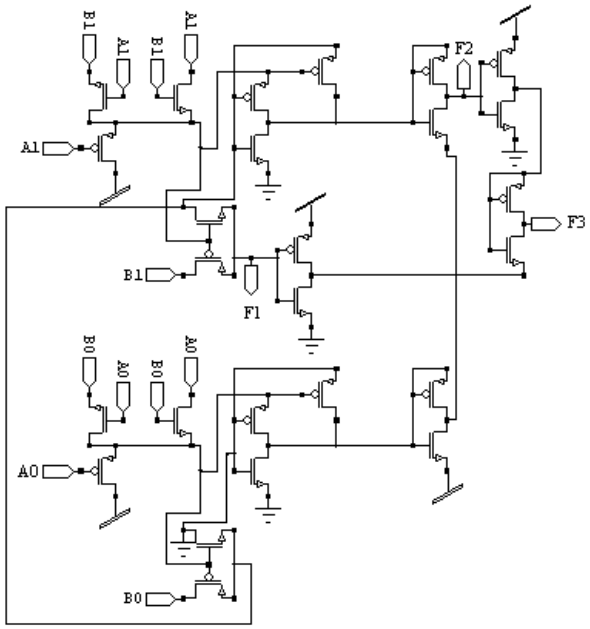

Fig 3: Schematic of 2-Bit magnitude comparator using PTL logic

3. SIMUALATION AND DISCUSSION

All the simulations of the proposed and existing magnitude comparator have been carried out using Tanner EDA tool version 12.6 at 45nm technology. The power consumption of proposed design is less (33.8%-45.7%) in comparison to existing design of magnitude comparator; this analysis is done with respect varying input voltage (Figure 4).

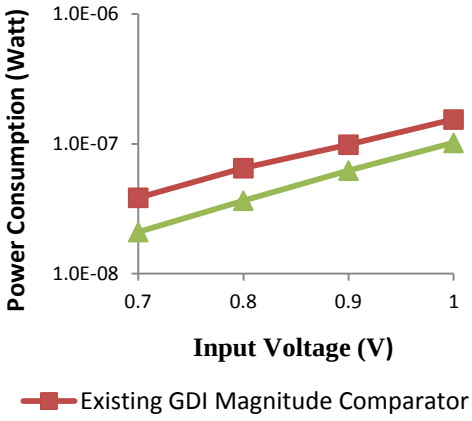

Fig 4: Power Consumption at various input voltage

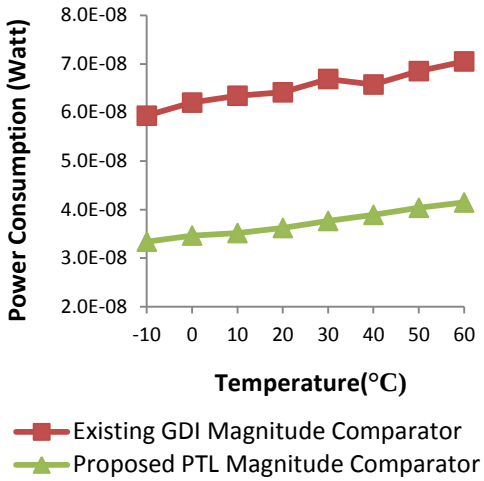

Fig 5: Power Consumption at different range of temperature

The power consumption of proposed magnitude comparator at various temperature (-10°C to 60°C) is less than the existing magnitude comparator (Figure 5).From this figure it can be notice that power consumption of existing magnitude comparator fluctuates with increases in temperature whereas proposed design show better sustainability.

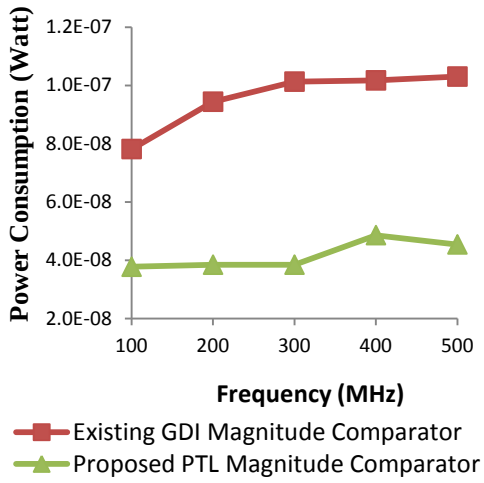

Fig 6: Power consumed at different range of operating frequency

Similar (Figure 6) reveals that power consumption proposed design is less than existing design with respect to operating frequency. Therefore, the proposed PTL magnitude comparator is better option for the high frequency application.

4. CONCLUSION

The PTL logic style has been used to design magnitude comparator instead of GDI technique, so as to reduce the fabrication complexity. The power consumption with respect to input voltage, temperature and operating frequency of proposed design is less in comparison to existing design. From this, it can be concluded that the proposed magnitude comparator circuit design is power efficient and area efficient as the transistor count of proposed design is reduced by four in comparison to existing design.

5. REFERENCES

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