Low Power-High Speed 11T Full Adder DSM Design

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ABSTRACT
Low power designs has become one of the primary focus in Deep Sub-Micron (DSM) Technology. Optimization of speed, power and area can be achieved by using Gated Diffusion Input (GDI) technique. In this paper an 11T Adder using GDI technique is proposed and it is compared with various existing adder circuits for Average Power dissipation, delay & PDP. Proposed circuit is designed using Cadence Virtuoso Tool for 180nm CMOS technology. Area has been evaluated by Microwind using TSMC BSIM 180nm technology. A comprehensive study and analysis of various Adder circuits has been done in this paper and comparison of proposed 11T adder (input 1 bit) with these circuits shows reduction in Average Power by 93.25%, 59.16%, 64.09%, and 85.28 % with respect to 28T, GDI, SERF & 8T circuits respectively. Proposed adder with 8 & 16 bit inputs are also implemented.

Keywords
Leakage power, GDI, SERF, transmission gate.

1. INTRODUCTION
With the explosive growth, the demand, and the popularity of portable electronic products, the designers are driven to strive for smaller silicon area, longer battery life, higher speed, and enhanced reliability is increases with technology scaling. As Technology scaling increases the transistor count and operating frequency, which push the market demand for more and more function in Integrated circuit. However scaling always increases leakage power dissipation. As channel length reduces which results in increase of power dissipation with respect to technology progresses. To reduce the power consumption different logic design techniques like CMOS complementary logic, Dynamic CMOS, Pseudo NMOS, Dynamic CMOS, CMOS Domino logic, Cascade voltage switch logic (CVSL), Modified Domino logic, Pass Transistor Logic (PTL) have been proposed [1-3]. Power dissipation depend on device structure property like gate oxide thickness, channel length, doping profile etc. as they are due to different physical phenomena Although Static CMOS Logic has been the most popular design approach for the past three decades [4-5]. By scaling down the feature size of MOSFET devices in nano-meter, the supply voltage should be scaled down to avoid hot- carrier effects in CMOS circuits. To enhance the speed of the CMOS circuits, threshold voltage of the circuits has to be scaled down. However, due to scaling of threshold increase in the stand by current. In over proposed circuit of 11T adder is a one-bit full adder core has three inputs (A, B, C_{in}) and two outputs (Sum S and Carry C_{out}).The proposed adder increases the speed of the circuit and mitigate the power consumption of the circuit.

The organization of the paper is as follows: The section II, describes previous work which consist of 28T, SERF, GDI, 8T Adder circuits. Section III, presents the proposed 11T full adder using Cadence virtuoso EDA. Section IV presents simulation result using Cadence EDA and Area description using Microwind. Conclusion is presented in section V.

2. PREVIOUS WORK
A digital signal full adder cell is defined as a logical cell that performs an addition operation on three one-bit binary numbers. This cell produces a two-bit output a carry and a sum [4]. Behavior of different adder circuits are studied and analyzed.

A. Conventional 28T CMOS Full Adder Circuit: The Conventional CMOS adder cell using 28 transistors based on standard CMOS topology. Due to large number of transistors, its power consumption also increase, speed reduces and it also occupies larger area. Large PMOS transistor in pull up network result in high input capacitances, which cause increase in dynamic power dissipation and larger delay. One of the most significant advantages of this full adder was ts high noise margins and thus reliable operation at low voltages.

B. Gate Diffusion Input (GDI): The GDI cell is basically implemented with the help of invertors, the combination of two inverter forms GDI cell which consists of NMOS and PMOS which reduces the area of the adder circuit as shown in Fig.1. A basic GDI cell contains four terminals – G (common gate input of NMOS and PMOS transistors), P (the outer diffusion node of PMOS transistor), N (the outer diffusion node of NMOS transistor), and D (common diffusion node of both transistors) [6].

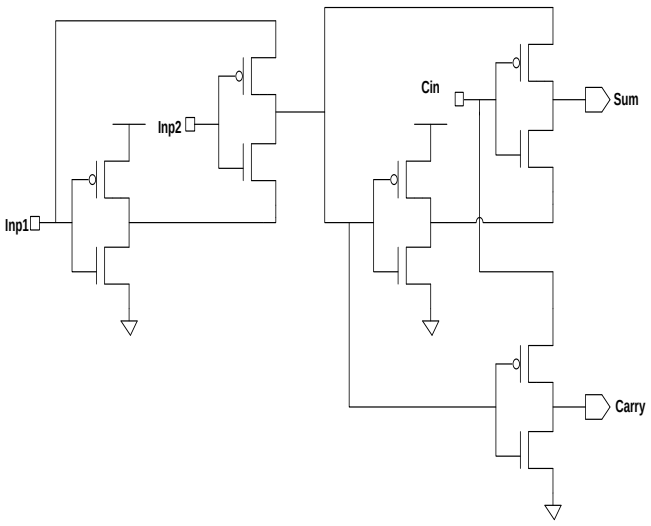

Fig 1: Schematic of GDI Full Adder

Table 1 In GDI cell we are providing input to all the three terminals from input, V_{dd} and GND. show how a simple change of the input configuration of the simple GDI cell corresponds to all the three terminal N, P, G at different Boolean functions. Referring to Table1 most of the functions

are realized using the function F1 and F2 since they are possible to realize using CMOS p-well process.

TABLE I. LOGIC FUNCTION IMPLEMENTATION WITH GDI TECHNIQUE.

N	P	G	Out	Function
0	B	A	$\overline{A}$.B	F1
B	1	A	$\overline{A}$+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\overline{A}$B+AC	MUX
0	1	A	$\overline{A}$	NOT

TABLE II. LOGIC FUNCTION IMPLEMENTED WITH MGDI TECHNIQUE.

N	P	G	Out	Function
A	B	B	A+B	OR
B	A	A	AB	AND
B	A	C	$\overline{C}$A+CB	MUX
0	1	A	$\overline{A}$	NOT

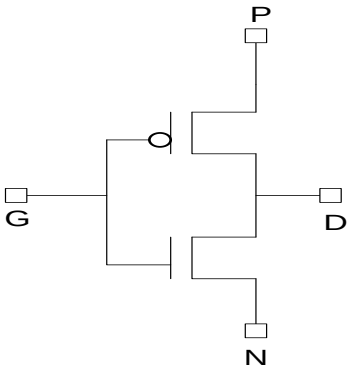

Fig 2: Symbol of GDI cell

C. Static Energy Recovery Full Adder (SERF): SERF is Static Energy Recovery Full adder is basically 10T full adder it is made from XNOR gate full adder design, SERF reduces the area of the circuit and enhance the speed of the circuit to achieve proper logic of SUM and Carry wave form of Adder circuit [8]. In SERF when logic level is high charge applied to the load capacitance during low logic charge flow from drained to ground. It should be noted that the new SERF adder has no direct path to the ground. The capacitor stores the charge is reapplied to the control gates [9]. The combination of not having a direct path to ground and the re-application of the load charge to the control gate makes the energy recovering full adder an energy efficient design. The SERF reduces the hardware of the circuit increases the speed with the help of new design to achieve proper logic of SUM and Carry of the adder circuit.

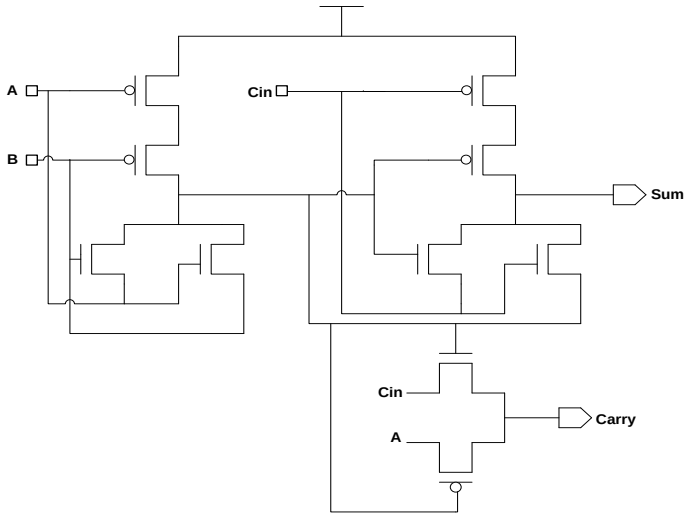

Fig 3: Schematic of SERF Full Adder

D. 8 T Full Adder Circuit : The basic of 8T full adder consists of 3 modules, Carry and two XOR. The two XOR block is used to generate the SUM operation. For the carry section GDI based 2TMUX is used and (A XOR B) as the selection signal. The C_{out} and Sum the module need 2 and 6 transistors respectively [10]. The transistor level implementation of the eight transistor full adder. From the diagtam of 8T it is obvious that both SUM and C_{out} has larger delay of 2T. It doesn't suffer from threshold voltage loss problem. By applying proper sizing of the transistor we increase the noise margin 3T XOR gate. The area reduced by 8T transistor, PDP also reduces to increase the speed of the circuit than other existing circuit.

3. PROPOSED 11T FULL ADDER

In this section we introduce a novel Low-Power Full Adder, which has good characteristic in term of speed and power. The circuit of 11T adder is a one-bit full adder core has three inputs (A, B, C_{in}) and two outputs (Sum S and Carry C_{out}). The adder is made of three CMOS inverter. Input A is directly connected to first inverter & Input B is connected to parallel PMOS network. The output of the first inverter generate compliment of C_{out} and SUM Compliment is generated with the help of C_{out} which is feed to the second inverter, C_{in} is feed to the third inverter so as to generate the SUM. Another transistor which is stacked to the inverter second and third to reduce the leakage power dissipation in the circuit and to enhance the speed of the circuit by mitigating the power consumption of the circuit. The stacking transistor generates the proper output logic of the circuit which we face in GDI technique. The circuit is further incorporated in 8-bit & 16-bit Adder So as to enhance the speed of the circuit as shown in Fig.4.

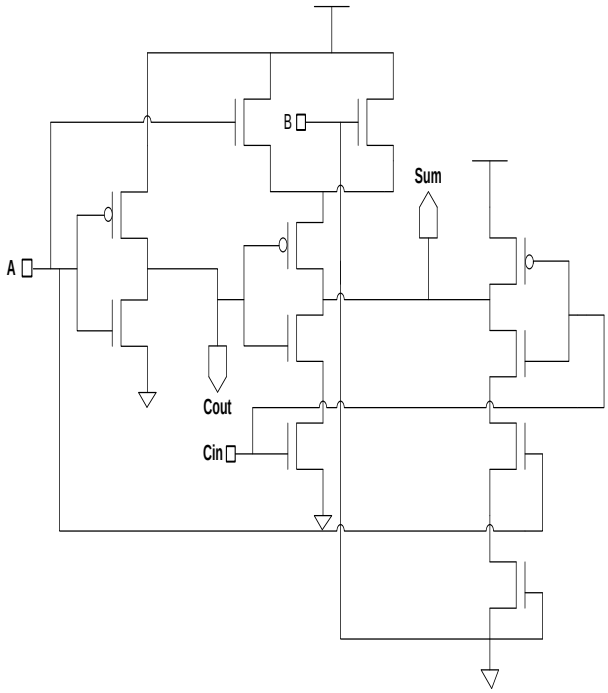

Fig 4 : Schematic of Proposed 11T Full Adder

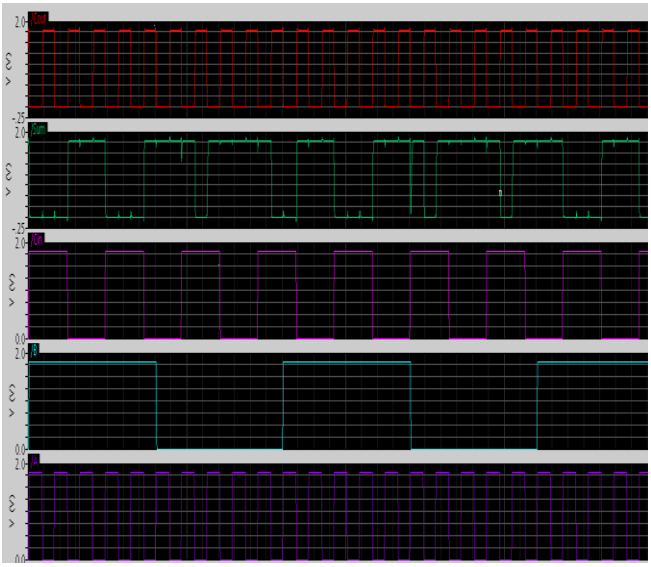

Fig 5: Output wave form of the proposed Circuit

4. SIMULATION ANALYSIS

The Power Consumption of proposed circuit is remarkable reduced than the other Approach at 180nm technology with supply voltage of 1.8v. The circuit is simulated at the temperature of 27^0c. All transistor have minimum length (L_{min}=180nm according to used technology), while their width are typically design parameters. In order to prove that which designs consume less power and have high performance, Simulation is carried out for Power, delay and Power delay Product.

TABLE. III. Comparison of Power, Delay, PDP of 28T, SERF, GDI, & 8T adder with proposed circuit

Parameters	Average Power(us)	Delay(ns)	PDP(fs)
28T	47.6	3.235	153.98
SERF	8.94	2.186	19.569
GDI	7.86	2.176	17.1033
8T	21.82	2.20	48.00
Proposed 11T	3.21	.03929	.12612
8 Bit full Adder from 11T	42.23	6.028	254.56
16 Bit full Adder from 11T	86.83	2.024	175.39

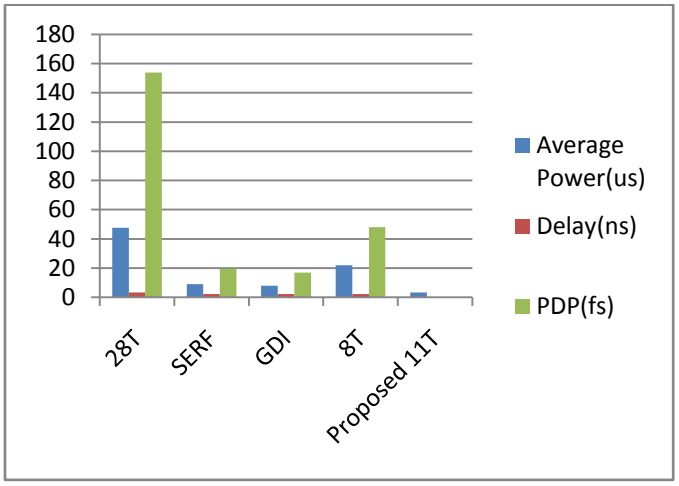

Fig 6: Comparison of different Adder circuit with Proposed 11T Adder

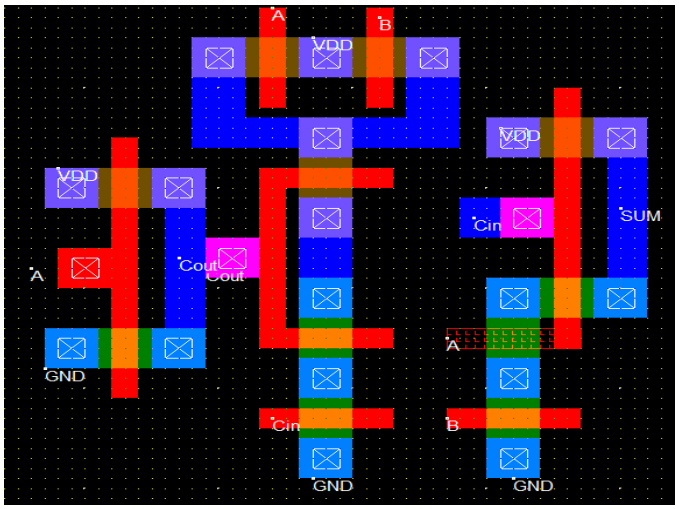

Fig 7: Layout diagram of Proposed 11T Adder

5. CONCLUSION

Adder circuits are basically used to implement wide Arithmetic circuits. These circuits are used in Dynamic RAMs, Static RAMs, high speed processors and other high speed circuits and GDI technique reduces the area of the Arithmetic circuits. This paper has concluded with the proposed efficient design of Adder Circuit on 180nm technology in terms of leakage and speed. Comparison of proposed 11T adder (input 1 bit) with these circuits shows reduction in Average Power by 93.25%, 59.16%, 64.09%, and 85.28 % with respect to 28T, GDI, SERF & 8T circuits respectively. From proposed circuit we have also implemented full adder with 8-Bit &16-Bit inputs and mitigate the average Power consumption and enhance the speed of the circuit.

6. REFERENCES

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