A High Speed Explicit Pulsed Dual Edge Triggered D Flip Flop

Manan Joshi
IIMT COE, Gr. Noida
India

D.S.Chauhan
UTU, Dehradun
India

B.K.Kaushik
IIT, Roorkee
India

ABSTRACT
This paper presents an efficient explicit pulsed static dual edge triggered flip flop with an improved performance. The proposed design overcomes the drawbacks of the dynamic logic family and uses explicit clock pulse generator approach to achieve dual edge triggering. The proposed flip-flop is compared with existing explicit pulsed dual edge triggered flip-flops. Based on the simulation results overall improvements of 12.67% and 10.15% are observed in delay and power delay product respectively.

General Terms
VLSI, optimisation, explicit pulse generator, embedded logic, clock network.

Keywords
Power delay product, flip flop, power consumption, propagation delay, CMOS logic, transmission gate, explicit pulsed.

1. INTRODUCTION
Flip Flops and latches form part of clock distribution network, timing elements, memory etc in digital systems. Reducing delay and power consumption will have a deep impact on the performance of digital systems. Flip Flops affect the clock frequency, since their delay occupies a significant fraction of the clock cycle, especially in fast micro-architectures with low logic depth. Together with the circuits devoted to the clock generation and distribution, Flip Flops are part of the clock network that is responsible for 30%-50% of the whole chip energy budget [1]. Power consumption has become a significant issue in modern IC designs, especially for high-end processors and energy-aware mobile devices.

During recent past a lot of advancements have been observed in the field of Flip Flops. The earliest work on edge triggered D-Flip Flop gives the Yuan-Svensson D-Flip Flop [2] that was proposed in the year of 1996. The transistors in this flip flop have conflicting requirements and hence this circuit cannot be optimised well. The sense amplifier based flip flop [3] consisting of a sense amplifier and slave latch is very similar to a master slave flip flop. Here only one transistor is active during clock transition that increases the driving capability of the output stage and reduces power dissipation. But being a two stage, circuit it cannot reduce delay efficiently. The conditional capture flip flop [4] is an innovation where the internal nodes switch only when the output needs to be switched. This approach can save power dissipation in a circuit. Another flip flop introduced has the advantage of being able to avoid stacking of PMOS transistors. As a consequence, low voltage and low power operation becomes feasible. The low swing clock double edge triggered flip flop [5] uses a data sampling front end and a data transferring back end and the internal nodes switch only when there is a data change. It results in reduced power consumption. Conditional discharge flip flop [6] introduced another innovation where output switches off the discharge path of first stage to prevent it from discharging and doing evaluation in succeeding clock cycles as long as the input does not change. Thus the flip flop reduces power consumption further. The conditional precharge flip flop was also introduced to save power consumption by not allowing precharging to take place as long as D and Q have similar input and output respectively. Similarly the conditional data mapping flip flop [7] reduces the dynamic power consumption by mapping the inputs to a configuration that eliminates redundant internal transitions. The data mapping is conditional *i.e.* when the applied input is the same as the output that results in no internal transitions. A clock branch sharing flip flop [8] reduces the number of clocked transistors and thus reduces the power consumption. In clocked Pseudo NMOS level conversion flip flop [9], Pseudo NMOS has been used for conditional discharge. The benefits of level conversion are also used. The energy efficient dual edge triggered level converting flip flop [10] has the benefits of level conversion and data retention in sleep mode that are used to reduce switching activity and hence power consumption.

There are four main flip flop classes: master slave (MS), implicit-explicit pulsed (IP and EP), differential and dual edge triggered [11]. Recently used Transmission Gate Flip Flop is an example of Master Slave Flip Flop. Hybrid Latch Flip Flop and Transmission Gate Pulsed Latch refer to the Pulsed Flip Flop that can be used for both Implicit(IP) and Explicit(EP) operation respectively. Likewise, Conditional Capture Flip Flop is a Differential Flip Flop and Conditional Discharge Flip Flop is a Dual Edge Triggered Flip Flop. Pulse triggered flip flops have a simple structure, negative setup time and soft edge. The pulse generator of explicit pulsed flip flop is shared by neighbouring flip flops [12]. Ultra Low Voltage Logic based D Flip Flop using sub threshold voltage operated Schmitt Trigger has very low power consumption [15]. Ultra Low voltage circuits suffer from insufficient noise margin, setup timing constraints and hold time violations that require special consideration [16]. The conventional CMOS logic and pass transistor logic (PTL) styles [17] are two major architectures that are used to implement logic circuits. The PTL family [18] primarily resulted in (1) complementary PTL (CPL) (2) Transmission gate (TG) Logic. However, these pass transistor logic styles become very slow when cascaded due to the increased delay and insertion of buffers (CMOS inverters) is necessitated. This negates the advantage of low power consumption that PTL logic has over other logic styles. A logic style that uses a combination of PTL and CMOS will have lesser power consumption due to use of PTL and lesser delay due to drive capability of CMOS logic.

The design of the proposed D Flip Flop uses both Transmission gate Logic as well as CMOS logic styles in such a way that it not only reduces the number of transistors used but also the drive capability that in turn reduces delay.

This paper introduces a new dual edge triggered Flip Flop using CMOS logic, transmission gate and pulse generator. This architecture is capable of embedding logic functions [19] and can be used for designing control units and pipelined datapath structures. It also performs charge sharing free operation more efficiently. This dual edge triggered flip flop that uses the clock pulse based approach reduces power consumption drastically in comparison to earlier reported research works [12-14]. The proposed flip flop avoids MOS transistor stacking, reduces internal node switching and as a consequence low voltage and low power operation is possible. The two stages *i.e.* the input stage and the output stage are basically CMOS inverters that switch only when there is a data change and hence result in reduced power consumption. The pass transistors, NMOS and PMOS are used to construct the transmission gate that provides edge triggering. It results in reduction of the number of clocked transistors and power consumption.

The rest of the paper is organised as follows. Section II presents the proposed D Flip Flop with its functionality. Section III gives the Simulation Set-up used. Section IV compares the proposed D Flip Flop with architectures proposed earlier [12-14]. Finally, conclusions are drawn in section V.

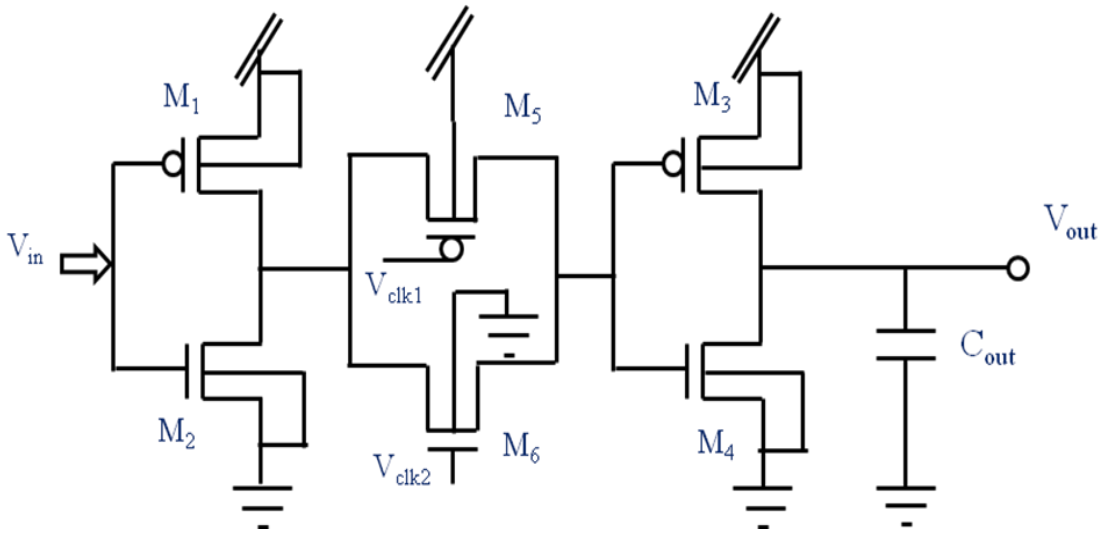

Fig 1: Proposed Dual edge triggered Flip Flop

2. THE PROPOSED FLIP FLOP

The proposed D Flip Flop shown in Figure 1 consists of an input and output stage that is an inverter, whereas the middle stage that allows the input to pass through only at the clock edge. The two inverters invert the signal twice and hence the output is the same as input. Two clock pulses that are generated from pulse generator are applied to the MOSFETs (M_5 & M_6). The parasitic capacitance at the input of the output stage inverter holds the charge/signal. The NMOS (M_6) serves as a good pull down device and brings the input of the output stage inverter to zero volt, whereas the PMOS (M_5) serves as a good pull up device and brings the input of the output stage to V_{dd}. The Figure 1 above shows the proposed D Flip Flop and Figure 2 ahead shows the clocks. In Figure 1 clock V_{clk1} is generated from V_{clk2} by passing it through an inverter.

The clock V_{clk2} is generated from the clock with 50 percent duty cycle using an explicit pulse generator shown in Figure 3. The explicit pulse generator produces a pulse at every clock edge (V_{clk2}). The three inverters serve to delay the clock pulse applied at input of the XNOR gate and provide complementary inputs. When V_{clk} switches from low to high or vice - versa the inputs to the XNOR gate are momentarily same. Otherwise the two inputs are complementary in nature. This produces a pulse at every clock transition. It is essential to ensure that inverters I_1 & I_2 delay the effect of change in clock edge. This is achieved by increasing the length (L) of the NMOS and thereby weakening it so that its turn ON is delayed. When length (L) increases the resistance increases allowing NMOS to remain OFF for a longer time. The inverter also will have a longer falling edge delay. V_{clk2} is generated at node X.

The clock pulses shown in Figure 2 are derived from the explicit pulse generator. Figure 3 shows the circuit of the pulse generator. These pulses are applied to the transmission gate formed by M_5 and M_6 as shown in Figure 1 causing edge triggering. Power consumption of a particular clocking scheme can be represented as [5]

$$P_{clk\text{-}scheme} = P_{clk\text{-}network} + P_{FF} \quad (1)$$

where $P_{clk\text{-}network}$ and P_{FF} represent power consumptions in the clock network and flip flops respectively. The total power dissipation of the clock network depends on both the clock frequency and the data rate that can be expressed as [11].

$$P_{clk\text{-}network} = V_{dd}^2[\, f_{clk}(C_{clk} + C_{ff,.clk}) + f_{data}\, C_{ff.data}] \quad (2)$$

where f_{clk} , f_{data} , C_{clk} , $C_{ff,.clk}$, $C_{ff,\ data}$ represent the clock frequency, the average data rate, the total capacitance seen by clock network, the capacitance of the clock path seen by the flip flop, the Capacitance of the data path seen by the flip flop respectively. The total power dissipation in the flip flop is as follows [5]

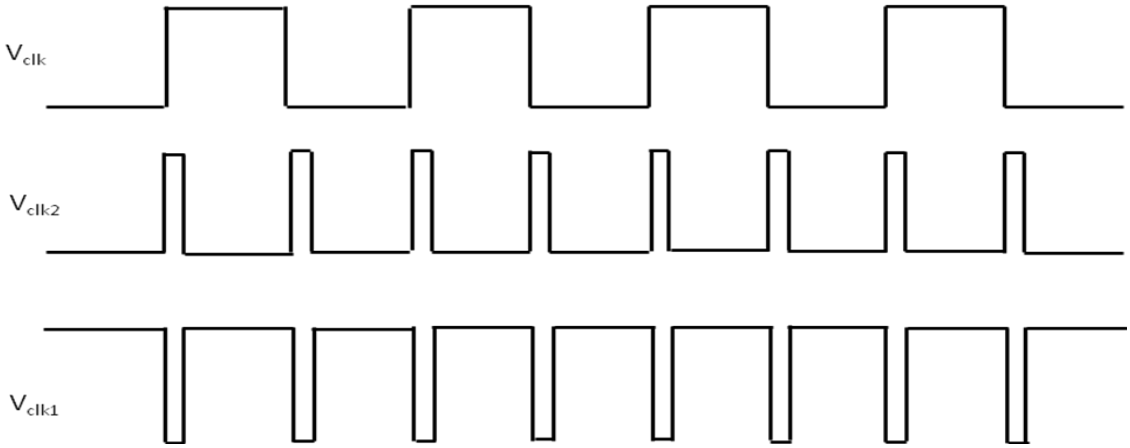

Fig 2: Clocks applied to proposed D Flip Flop

$$P_{FF} = \{(\alpha_i . C_i . \gamma + \alpha_o . C_o . \gamma + C_{clk\text{-}buf}).V_{dd}^2 \quad (3)$$

where C_i , C_o , α_i , α_o , $C_{clk\text{-}buf}$ is the internal node capacitance of the FF, the output node capacitance of the flip flop, the internal node transition activity ratio, the output node transition activity ratio, the capacitance of the clock buffers repectively. γ is 2 for double edge triggered flip flops and 1 for single edge triggered flip flops.

From the above expression (2) it is obvious that the clock power can be reduced if any of the parameters can be reduced. The reduction of V_{dd} is already the trend of contemporary design and has the strongest impact on the $P_{clk\text{-}scheme}$ expression. By reducing the overall capacitance of the clock network, the power dissipation is reduced. Similarly, by reducing the capacitance inside a flip flop, $C_{ff.clk}$ and $C_{ff,.data}$, power is reduced.

From the expression (3) it is clear that power dissipation in the flip flop is reduced if any of the parameters in the expression is reduced. The internal node capacitance is reduced by keeping the number of nodes as less as possible and keeping the dimensions of the MOSFETs as small as possible. The internal node transition activity α_i and output node transition activity α_o is reduced by designing the circuit in such a way that the internal and external nodes switch only when the data change takes place.

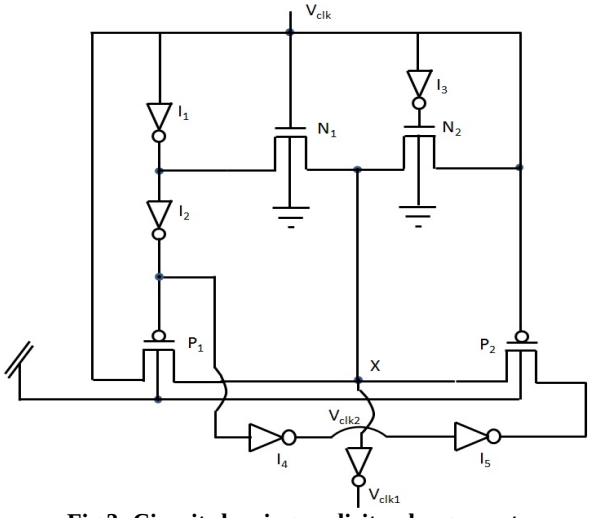

Fig 3: Circuit showing explicit pulse generator

The conclusions from the above three expressions are used while designing the proposed Flip Flop. Attempt is made to keep the MOSFETs M_3, M_4, M_5 and M_6 as small as possible to reduce power consumption in the data path network. Moreover the design of the Flip Flop is such that the internal nodes switch only when the data change takes place and hence α_i and α_o are reduced.

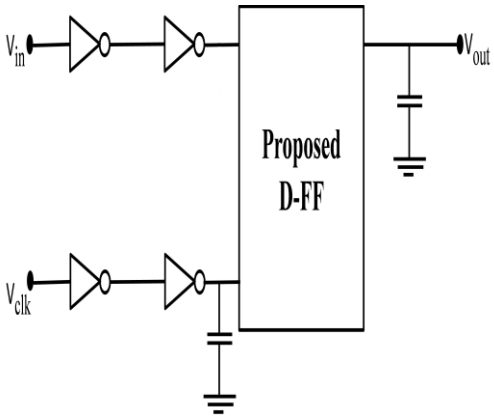

Fig 4: Set up used for simulation

3. SIMULATION SETUP

The set-up used in our simulations is as shown in the Figure 4. The circuits are simulated in real environment, where the buffers (inverters) drive the flip flop inputs (data and clock) and the output drives a capacitive load of 21fF. An additional capacitance of 3fF is placed after the clock driver. We have applied at the D input, an input data with an activity factor of 25% to reflect the average power consumption. Power consumed in the data and clock drivers is included in our measurements. Clock frequency used is 125 MHz.

4. RESULTS AND DISCUSSIONS

The simulation results are obtained using Tanner EDA in TSMC 180nm CMOS Technology. The design is simulated using the circuit at the schematic level. Table 1 presents the comparison between SEDNIFF Flip Flop and the proposed D Flip Flop. We analyse the two designs in view of Power Delay Product, DQ delay, CQ delay and Power Consumption.

Table 1. Comparing the flip flops in terms of delay, power consumption and power delay product

Design Name	Tran count	DQ Delay (ps)	Power (μW)	PDP (fJ)	% change in PDP
SCDFF	29(17)	234.5	41.97	9.8	-
DEPFF	29(14)	230.2	37.05	8.53	12.95
SEDNIFF[1]	29(11)	217.7	34.44	7.49	12.19
Proposed	22(6)[2]	190.1	35.42	6.73	10.15

[1]FlipFlop proposed in [12]
[2]In parenthesis is the transistor count of its latch

The primary drawback of flip flop SEDNIFF is that it is composed of twenty nine transistors out of which eleven are in the latch. The pulse generator has eighteen transistors that continuously switch with clock. This results in higher average power dissipation. The pulse generator and the latch consist of stacked transistors that reduce the efficiency of the flip flop. In the proposed Flip Flop pass transistors that are used to construct the transmission gate have length (L) and width (W) that are sized to reduce delay. The inverter at the output also has optimum sized transistors [18] so that pass transistors and the transistors of the input inverter have W and L as small as possible. Moreover the pulse generator consists of sixteen transistors and the latch part consists of six transistors. This results in lower average power dissipation. Due to symmetry, scaling of the proposed flip flop is simple. Proper design of the pulse generator ensures low power consumption. To convert this flip flop into a latch a keeper transistor is required at the output.

A waveform of D making a 0 → 1 and 1 → 0 transition.

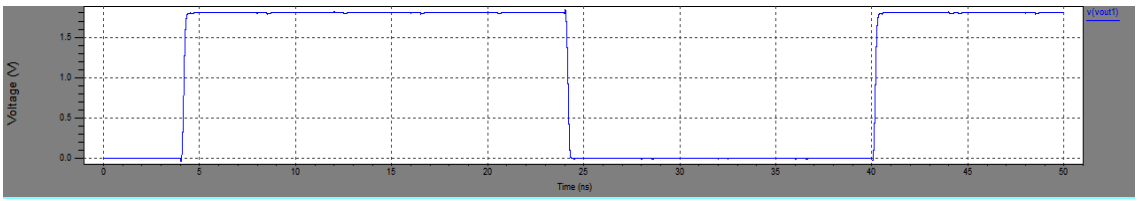

Fig 5: Output of proposed Flip Flop V_{out}

5. CONCLUSION

This paper presented the design of a new explicit pulsed double edge triggered D Flip Flop. This flip-flop has reduced redundant switching and short current and hence reduced power consumption. The flip flop has least number of clocked transistors and lowest power consumption and is therefore suitable for use in high performance and low power environments. In addition to this, it is also capable of embedding logic functions and performs charge sharing free operation more efficiently.

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