Low Power Domino Full Adder

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ABSTRACT
With the advancement of technology, power consumption and higher speed becomes major concern for VLSI systems. In this paper, a new hybrid domino XOR is proposed and compared with existing domino XOR cell. As an application of proposed XOR cell, 1-bit full adder has been designed and compared with a full adder circuit using existing XOR cell. Both proposed designs XOR and full adder show better results in terms of power, delay and power-delay product. All the simulations have been performed on 45nm technology using tanner EDA tool version 13.0.

Keywords
Domino, low power, PDP, XOR, XNOR and full adder.

1. INTRODUCTION
Low power has become main constrain for portable systems. These systems require more feature and high battery life time. The total power of the electronic circuit is the sum of static power, dynamic power and short circuit power [1]. In nanometer regimes, dynamic power consumption becomes significant contributor to over all power consumption [2], [3]. Hence, the reduction of power consumption is compulsory.

After studying various techniques in literature found that domino circuits require less power consumption than static circuits [4], [5], [6]. The operation of domino circuits is based on charging and discharging of output node capacitance. These circuits are applied for higher speed of the system [7].

XOR cell is essential to drive various digital circuits such as adder, comparator, multiplier, parity bit generator and checker circuit etc. [8], [9]. This paper proposes a new domino XOR cell using hybrid network technology. This network requires both nMOS and pMOS to design circuits [10].

The paper is organized as follows: Section 2 describes the N-type domino XOR cell reported in literature. Section 3 introduces the proposed domino XOR cell. Section 4 illustrates domino full adder circuit using exiting and proposed XOR cell. Simulation results and their comparisons are included in Section 5 and finally Section 6 concluded the paper.

2. PREVIOUS WORK
Fig. 1 shows standard N-type domino XOR cell [11]. The pull down network consists of n-type MOSFETs and two inverters are connected to give inverted input signals. M1 and N1 act as a precharge and evaluation transistor. They will charge/ discharge the dynamic node respectively. M2 acts as a keeper transistor to avoid charge sharing problem. This cell generates two output signals for XNOR and XOR at dynamic and output node.

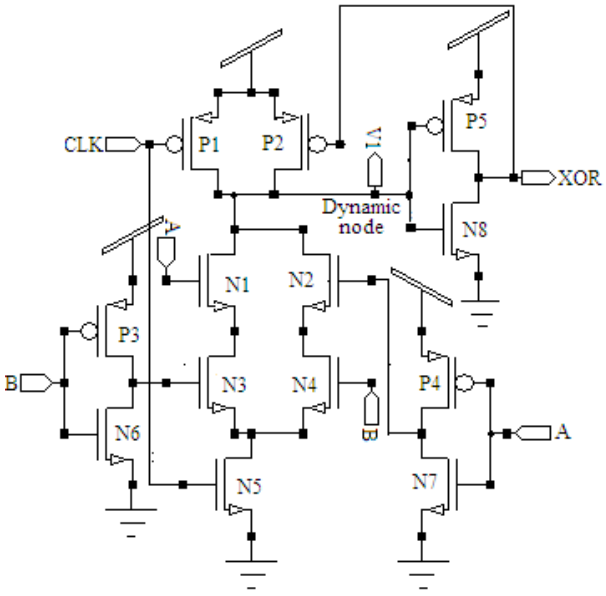

Fig. 1: Standard N-type Domino XOR Cell.

The working of existing cell is follows: when the clock signal is low, the circuit is in precharge phase gives high logic at dynamic node and low logic at output node. When the clock signal is high, the circuit is in evaluation phase. In this phase, the charging and discharging of dynamic node depends upon input signals. There are 4 possible combinations of 2 input signals. When input signals are 00 or 11, gets high logic at dynamic node and low logic at output node. When input signals are 01 or 10. Now there will be a conducting path between dynamic node and ground. This will discharge the dynamic node. Hence, the dynamic node gets low logic and high logic at output node.

3. PROPOSED XOR CELL
Fig. 2 shows the structure of proposed domino XOR cell. The pull down network of this cell is designed by hybrid network. Both pMOS and nMOS transistors are used in PDN. Here, nMOS keeper transistor is used instead of pMOS to increase the speed of circuit. Two nMOS transistors are connected at dynamic node (V1) to give high logic at dynamic node and low logic at output node in evaluation phase. This circuit does not require extra inverters to invert input signals. Hence the transistor count and performance of proposed XOR cell is better then existing cell.

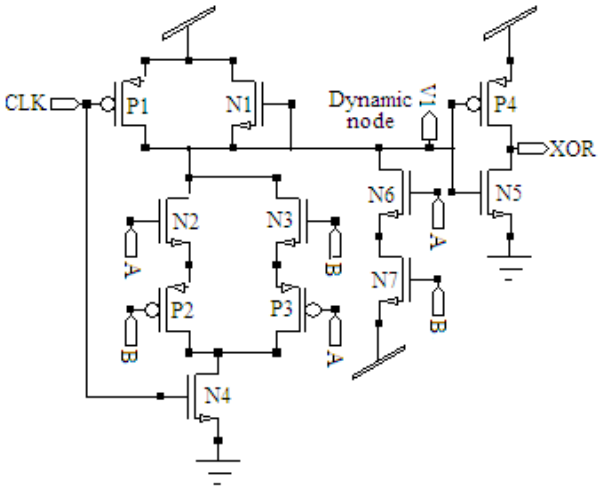

Fig. 2: Proposed Domino XOR Cell.

Whole circuit is driven by single clock signal. In the precharge phase, this cell gives high logic at dynamic node and low logic at output node for all input signal. In the evaluation phase, the output signals for dynamic node and output node depends on input signals. When AB are 00, now high logic at dynamic node and low logic at output node. When AB are 01 or 10 then one of series combination of PDN network will be turn on. This will discharge the dynamic node at low logic and charge the output node at high logic. When AB are 11, nMOS transistor N5 and N6 turns on. In this case, dynamic node will charge at high logic level and output node discharge at low logic level.

Table 1 illustrates the performance of domino XOR cell. Here this circuit gives XNOR logic at dynamic node (V1) and XOR logic at output node (OUT). Thus, the proposed circuit gives output for all possible input combination.

Table 1. Performance table of domino XOR cell.

Clock	Inputs		Output	
	A	B	XNOR	XOR
0	0	0	1	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

4. FULL ADDER

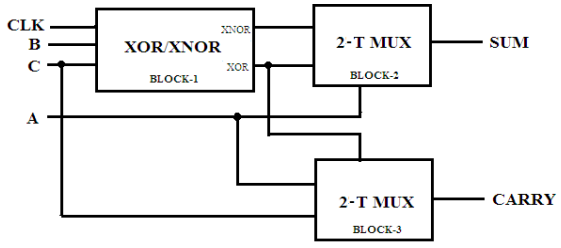

Fig. 3: Design technique of Full Adder

The expression of full adder is follows:

$$SUM = \bar{A} (B \text{ xor } C) + A (B \text{ xnor } C) \quad (1)$$

$$CARRY = AB + BC + CA. \quad (2)$$

Equation (1) and (2) show the logical expression of full adder for SUM and CARRY.

The operation of full adder is to add three binary bits. It takes three input signals A, B, C_{in} and gives two output signals SUM and CARRY. Fig. 3 shows one design technique of full adder. It consists of 3 blocks which are described as follows:

a) First block takes two input signals, clock signal and gives two output signals. It performs XOR and XNOR operation on inputs B and C.

b) Second block is designed using 2T multiplexer. It consists of one nMOS and one pMOS transistor. It has two input signals and one selection line. The output signals of first block act as input signals to this block. This block is designed for the expression shown in Eq. (1). Here A is selection line and XOR and XNOR are two inputs respectively from first block. If A is 0 then XOR logic is the output otherwise XNOR logic.

c) Third block is also designed using 2T multiplexer and it follows the expression shown in Equation (2). It has A, C as input signals and output of XOR as selection line. If XOR signal is 0 then output follows signal C otherwise signal A at output.

4.1 Full Adder using Existing Domino XOR Cell

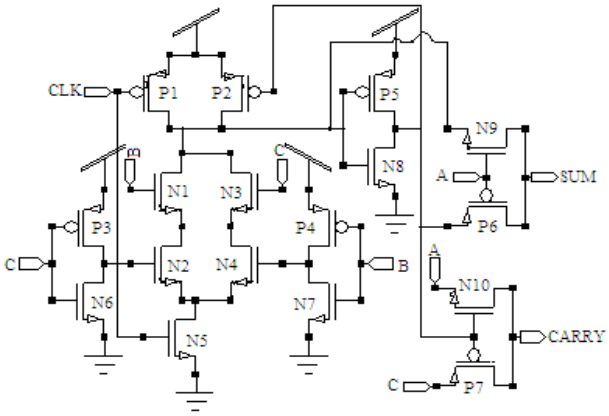

Fig. 4: 1-Bit Domino Full Adder using existing XOR cell.

Fig. 4 shows 1-bit domino full adder designed using existing domino XOR cell. The aspect ratios of all transistors are taken as one.

This circuit is designed by same technique as shown in Fig. 3. When the clock signal is high, the circuit gives correct output levels for all possible input combinations. But when the clock signal is alternate 01, this circuit does not give correct output level for input combinations100 and 110.

4.2 Proposed Domino Full Adder

Fig. 5 shows 1-bit domino full adder using proposed domino XOR cell. This circuit is designed by technique shown in Fig. 3. To remove drawbacks of existing full adder an efficient design of domino full adder is proposed. The drain of P7 and N10 are connected to source of N8. The source of P7 is connected to ground and source of N10 is connected to dynamic node. The drain of P8 and N11 are connected to P6

the source of P8 is connected to ground and the source of N11 is connected to input signal C.

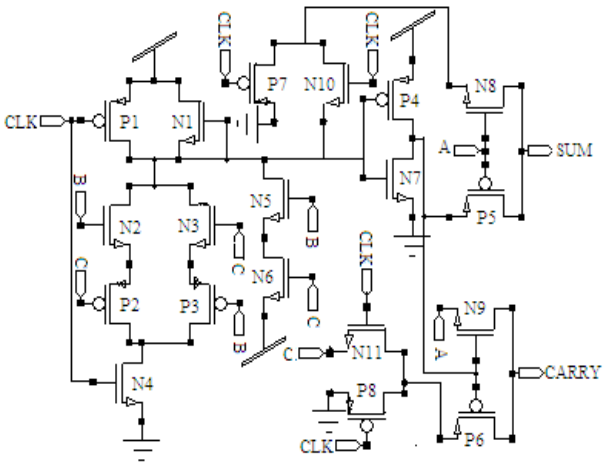

Fig. 5: Proposed 1-Bit Domino Full Adder.

The operation of this circuit is as follows: When clock signal is low i.e. in precharge phase, transistors P1, P7 and P8 are turn on. This gives low logic at the output of XOR cell and at the source of P6, N8. Therefore, this circuit gives low logic at SUM and CARRY.

When clock signal is high i.e. in evaluation phase N4, N10 and N11 transistors are turned on. In this phase, the output of proposed design depends on input signals. For first MUX input signal A acts as a selection line. If A is 0: P5 turns on then XOR output selects for SUM. If A is 1 then N8 XNOR output selects for SUM. For second MUX output of XOR gate act as a selection line. If B XOR C is 0 then C selects as an output of CARRY. If B XOR C is 1 then A acts as an output of CARRY.

By adding transistor, a new circuit is obtained that exhibits better performance. Thus, the proposed design works properly for both active high and active low clock signal.

5. SIMULATION AND COMPARISON

All simulations have been performed on tanner EDA tool version 13.0 at 45nm technology. The input and supply voltages are ranging from 0.5 to 1V in steps of 0.1V. The simulations are carried out for PDP with increasing input voltage, temperature and operating frequency.

Equation (3) shows the expression for dynamic power consumption [1]. From this Eq. it is clear that power consumption is directly proposal to switching activity, square of supply voltage, clock frequency and load capacitance. Thus, power consumption increases with increasing all this components.

$$P = \alpha . V_{DD}^2 . f_{CLK} . C_L \qquad (3)$$

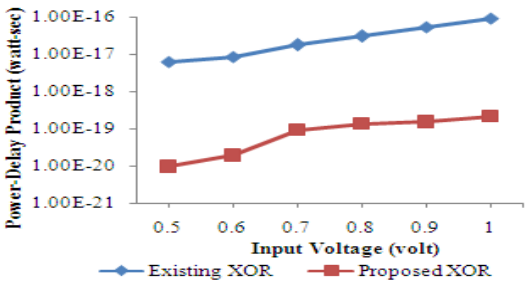

Fig. 6: Power-Delay Product with increasing input voltage.

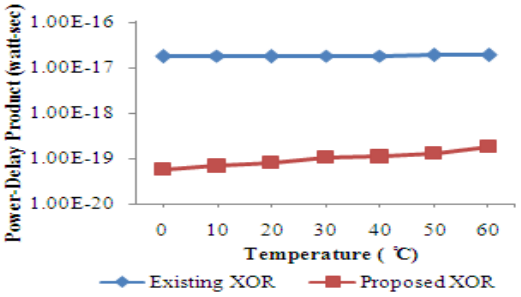

Fig. 7: Power-Delay Product with increasing temperature.

Fig. 8: Power-Delay Product with increasing frequency.

The graphs in Fig. 6 – Fig. 8 show PDP of both proposed and existing XOR cell with increasing input voltage, temperature and frequency. The graph in Fig. 6 reveals that the PDP of proposed XOR cell is remarkably less than existing XOR cell because in the evaluation phase, proposed design turns on fewer transistors. So it consumes less power. The graph in Fig. 7 depicts the PDP of both designs increasing with increasing the temperature. As temperature increases it increases the thermal generation of majority and minority carriers. Since proposed design has less transistor count. So the generation and recombination rate of carriers will be less. Fig. 8 shows PDP of both designs with increasing frequency. Thus, the proposed design of Domino XOR cell is the viable option for low power applications.

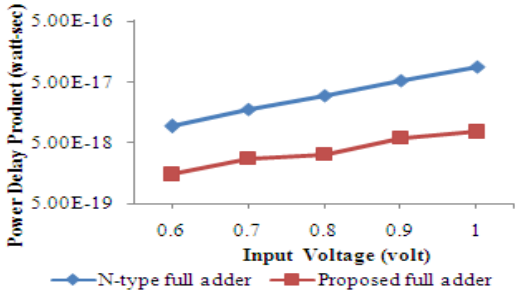

Fig. 9: Power-Delay Product with increasing input voltage.

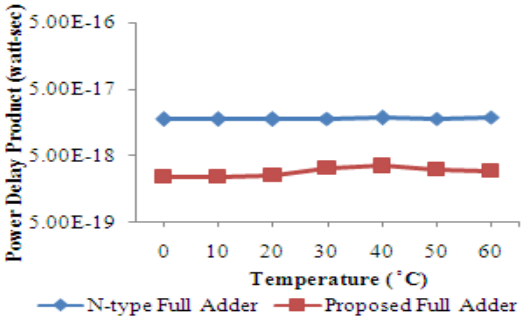

Fig. 10: Power-Delay Product with increasing temperature

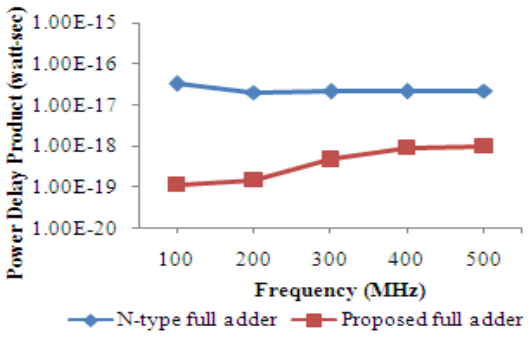

Fig. 11: Power-Delay Product with increasing frequency.

The graph in Fig. 9 – Fig. 11 shows PDP of both proposed and N-type full adder circuit with increasing input voltage, temperature and frequency. The graph in Fig. 9 shows the circuit performances of both designs are evaluated in terms of increasing input and supply voltage. There are two advantages of proposed full adder: first one is the proposed full adder consists of proposed XOR cell. Since, it takes less power than existing cell. Second is in precharge phase, the whole circuitry is not required to turn on. So the proposed full adder consumes less power. The graph in Fig. 10 depicts that proposed full adder design has better temperature sustainability then existing full adder design. The graph in Fig. 11 reveals that the proposed design operates efficiently at higher frequencies.

Thus the proposed design gives better PDP and voltage levels then existing design.

6. CONCLUSION

In this paper, a new hybrid domino XOR cell and its application domino full adder is proposed. Both proposed designs are working properly for all possible input combinations. The results show that PDP of proposed designs are better than existing designs with varying input voltages, temperature and operating frequency. Thus, these circuits can be used for low power and high speed complex circuit design and their applications.

7. REFERENCES

[1] S. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits, Analysis and Design", 2003, Tata McGraw-Hill, New York, NY, USA.

[2] A. Bellaouar and M. I. Elmasry, "Low-power Digital VLSI Design: Circuits and Systems", Kluwer Academic Publishers, 2nd ed.

[3] C. Cornelius, S. Koppe and D. Timm., "Dynamic circuit techniques in deep submicron technologies: Domino logic reconsidered", *IEEE conference on ICICDT*, 2006, pp. 1-4.

[4] P. K. Verma, S. K. Singh, A. Kumar and S. Singh "Design and Analysis of Logic Gates Using Static and Domino Logic Technique", *International Journal of Scientific & Technology Research*, June 2012, Vol. 1, No. 5, pp. 122-125.

[5] M. Kishor and J. P. Gyvez, "Threshold Voltage and Power-Supply Tolerance of CMOS Logic Design Families", IEEE, 2000, pp. 349-357.

[6] S. Jia, S. Lyu, Q. Meng, F. Wu and H. Xu, "A New Low-Power CMOS Dynamic Logic Circuit", IEEE conference on EDDSSC, 2013, Hong Kong.

[7] H. F. Dadgour and K. Banerjee, "A Novel Variation-Tolerant Keeper Architecture for High-Performance Low-Power Wide Fan-In Dynamic OR Gates", IEEE Trans. on VLSI Systems, Nov. 2010, Vol. 18, No. 11, pp. 1567-1577.

[8] S. Mishra, S. Wairya, S. Tiwari and R. K. Nagaria, "New deisgn methodologies for high speed low power XOR-XNOR circuits", Journal of World Academy of Science, Engineering and Technology (WASET), July 2009, Vol. 55, No. 35, pp.200-206.

[9] D. Wang, M. Yang, W. Cheng, X. Guan, Z. Zhu, and Y. Yang, "Novel low power full adder cells in 180nm CMOS technology", IEEE Conference on Industrial Electronics and Applications (ICIEA '09), May 2009, pp. 430–433.

[10] S. Wairya, R. K. Nagaria, and S. Tiwari, "Performance Analysis of High Speed Hybrid CMOS Full Adder Circuits for Low Voltage VLSI Design", VLSI Design, 2012, pp. 1-18.

[11] Wang. J, Gong. N, Hou. L, Peng. X, Geng. S and Wu. W, "Low power and high performance dynamic CMOS XOR/XNOR gate design", Microelectronics Engineering, 2011, Vol.88, pp.2781-2784.