

Design and Implementation of PCM-to-PWM Data Converter

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ABSTRACT

Pulse width modulation (PWM), a member of pulse time modulation (PTM) techniques, has been found advantageous for transmission of digital signals over optical fiber links. Most of the data is often found in Pulse Code Modulated (PCM) form and therefore needs to be converted into Pulse width modulation. A simple and low-cost circuit for the conversion of pulse code modulation (PCM) to Pulse Width Modulation (PWM) is proposed. The circuit has been tested in hardware and the experimental results are quite satisfactory. The circuit for the conversion of PWM to corresponding PCM is also proposed.

KEYWORDS:

Optical fibre, PCM, PWM

1. INTRODUCTION

Due to tremendous availability of bandwidth, optical fiber is increasingly becoming popular, as large number of signals are being transmitted simultaneously through optical fiber by using various pulse time modulation techniques. Pulse Width Modulation technique, a member of pulse time modulation techniques, has been found fruitful and is widely used for transmission of data over optical fibre without the disadvantage of the high bandwidth overheads associated with purely digital modulation [1,2,5]. In Pulse width modulation the width of the pulse is varied in accordance with the amplitude of the message signal as shown in Fig. 1.

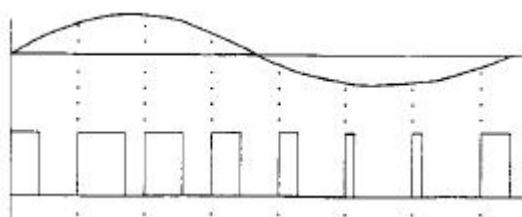


Fig.1: PWM signal

For an analog message signal, the PWM is implemented usually in two forms Naturally Sampled PWM and Uniformly Sampled PWM [3]. In naturally sampled PWM, as shown in Fig 2(a), the input signal is directly compared with the ramp signal by using generally an operational amplifier as comparator. The performance of the resulting signal depends on how linear the ramp is generated. Since the ramps are not perfectly linear, therefore this results into generation of harmonics at the receiving end and hence limits the modulation index less to than 50% [2].

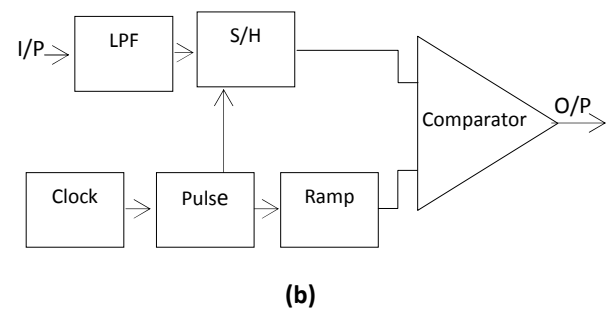
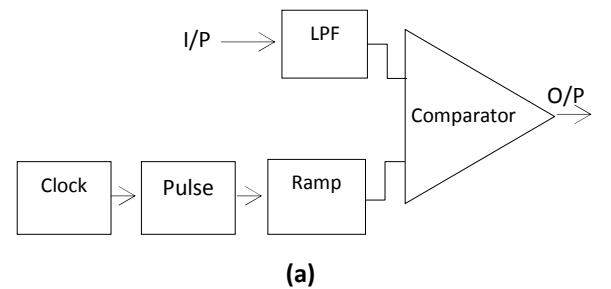
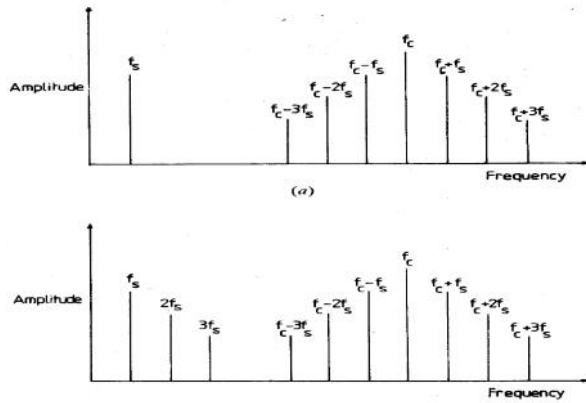


Fig.2 (a) Naturally sampled PWM
(b) Uniformly sampled PWM

The modulation index can be improved by using uniformly sampled PWM, wherein the input signal is first sampled uniformly as shown in Fig 2(b). Although a good modulation index and superior signal to ratio can be achieved, however the system implementation is more complicated as shown in Fig. 2(b). Besides, frequency spectrum of uniformly sampled PWM contains a series of additional harmonics than naturally sampled PWM, as shown in Fig.3. However, this disallows the demodulation using a simple low pass filter [3]. The spectral analysis and other characteristics of PWM have been discussed in detail by Wilson *et al* [3,4] and Suh [7]. It may be mentioned that at the receiving end, the demodulation is carried out by converting the received PWM signal into PAM signal employing another S/H circuit and ramp generator. The ramp generators used at the transmitter and receiver must generate the same shapes of ramps. This often leads to a complex situation in any electronic communication system to maintain such kinds of synchronization.



**Fig.3: (a) Spectrum of naturally sampled PWM
(b) Spectrum of uniformly sampled PWM**

The problems associated with the above techniques, for generation and transmission of analog PWM, have been solved by using digitally generated pulse width modulation signal [2], wherein the ramp signal has been replaced by a counter and the input analog message has been converted into digital format instead of applying directly to the converter. There are also situations where the message is already available in PCM form and needs to be transmitted using PWM for the benefits associated with PWM [7]. The message then needs to be converted into PWM. The circuits for PCM-to-PWM conversion, usually based on DSP implementation [6], are complex and have rarely been discussed in open literature. The authors present a simple and low cost circuit for the conversion of PCM-to-PWM form using a purely digital circuit implementation. The circuit for reproducing the corresponding PCM data at the receiving end has also been presented in this paper.

2. PROPOSED CIRCUIT

Fig. 4 shows the circuit diagram of the proposed PCM to PWM converter. Message words used are generated by a word generator, which generates all the eight 3-bit words in almost random manner. Each message word is continuously compared with all the possible states of the 3-bit linear counter. When the corresponding bits of a message word and that of the linear counter are same, the comparator output X becomes low (otherwise it is always held high). Further, the output Y of the OR gate also depends upon the input R received from the most significant bit (MSB) of the modulo-9 counter. This bit also clears all the flip flops of 3-bit linear counter and supplies a clock signal to the message source. Since the clock signal of the message generator is supplied through the MSB of the modulo-9 counter, therefore the clock frequency of the counters is 9 times the message clock frequency. Hence the width of the message word interval will be equal to nine sub-intervals, each sub-interval being equal to the counter state interval. As the 3-bit linear counter goes through only eight different states and occupies only eight subintervals, the ninth sub-interval is thus used as the guard-band between two successive words.

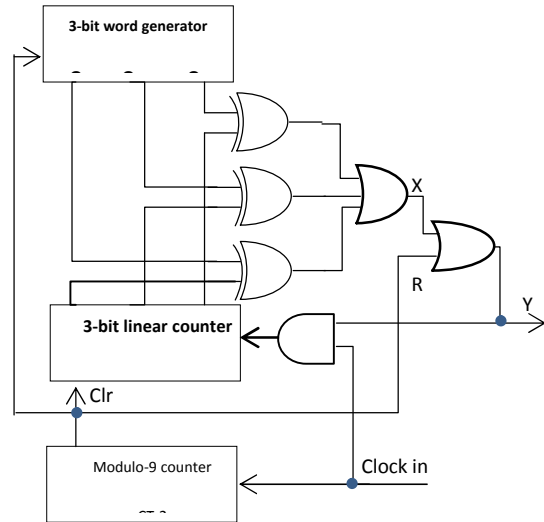


Fig. 4: Proposed PCM to DPWM Converter

This guard-band helps in recovering the PCM data at the receiver faithfully. To clarify the function, suppose the message word is '100' and both the counters have started from their clear states. The output will be high till the 3-bit linear counter (CT-1) reads as '100'. As soon as the fourth clock pulse appears at the input of the counter and it counts '100', the corresponding bits of the message word generator and the 3-bit linear counter become the same and therefore the output Y becomes low (the input R of the OR gate being low at this instant). Therefore the width of the output pulse (Y) becomes equal to four sub-intervals (corresponding to message word '100'). Further the counter (CT-1) stops counting the rest of the states because no more pulses are supplied, as one of the inputs of the AND gate is held at logic 0 during rest of the states of the counter CT-2. This holds the output Y at logic 0 for the input message period to complete. Now, when the modulo-9 counter assumes '1000' state, the output Y becomes high and this is where the excursion of next output pulse for the next message word commences. However, the 3-bit linear counter maintains the state '000' till the modulo-9 counter comes in all zero state. At this instant of time the message generator receives a high to low pulse and thus is enabled to pass in the next message word.

2.1 Receiver Circuit

The circuit diagram for PWM-to-PCM converter is shown in Fig.5. The received PWM signal is directly applied to the clock inputs of the D-flip flops. The flip flops are connected to a modulo-9 counter. Both the modulo-9 counters at receiver as well as used at transmitter are synchronized with each other. When the received PWM signal changes from high to low state, the data at the inputs of the D-flip flops gets latched at the output. Since both the modulo-9 counters used at the transmitter as well as at the receiver are synchronized, the instant at which the transitions from high to low take place the data at the output of these counters is same as the data at the output of the message generator at the transmitter. Therefore the latched data at the outputs of the D- flip flops is the recovered PCM data.

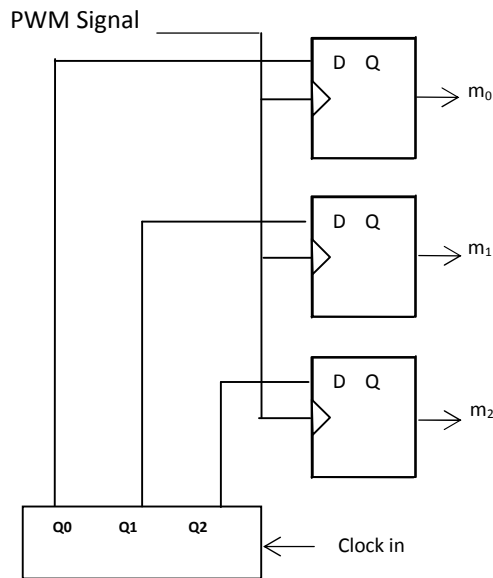


Fig. 5: PWM to PCM converter

3.

The hardware prototype module of the proposed circuit has been fabricated for experimental investigation. Modulo-9 counter as shown in Fig. 4 has been implemented using four JK flip flops using IC7476 and NAND gates using IC7400. This specially designed four stage counter starts from the state '0000' and counts upto state '1000' and then attains again an all zero state. Message words used have been generated by a specially designed counter, which generates all the eight 3-bit words in almost random manner. The waveforms obtained from the circuit are shown in Fig.6. The high frequency clock signal required by the circuit has been applied externally. The recovered PCM data (original message) was found to be correctly received using static test by setting the clock frequency at 1 Hz.

4. CONCLUSION

Pulse width modulation has been found a good choice for transmission of digital data over optical fiber links. Since the data is often found in PCM form, there it needs to be converted into PWM form. Techniques, for conversion, discussed in open literature, are usually based on DSP implementation and are complex. A simple and low cost circuit for PCM-to-PWM conversion has been proposed in this paper. The circuit is implemented using purely digital circuits and thus making it suitable for IC implementation.

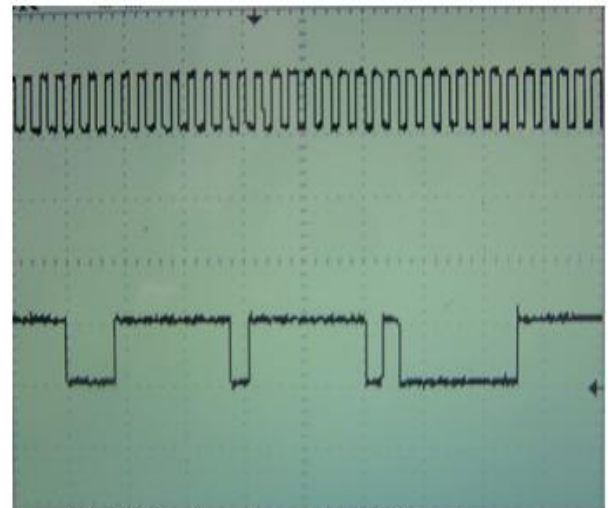


Fig. 6: Waveform of generated PWM signal
 (Upper: Clock Signal)
 (Lower: DPWM signal)

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