A Novel Power Reduction Technique for CMOS Circuits using Voltage Scaling and Transistor Gating

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ABSTRACT
The colossal portion of power in CMOS circuits is consumed during switching which is termed as dynamic power consumption. This absorbs more than 60% of the overall power in the circuit. However as the technology scales down, subthreshold leakage becomes commensurable to dynamic power dissipation. This happens as a result of reduction in threshold voltage and device geometry. In this brief, a high performance and power efficient technique is proffered which operates in subthreshold region. The proposed (VS-TG) technique curtails both dynamic and static power dissipation. The dynamic power dissipation is reduced by deploying Voltage Scaling technique while leakage or static power dissipation is lowered with Transistor Gating technique. The total power consumption is reduced by 30% to 90%. The proposed technique is implemented on 2-input NOR gate at different voltages at 10 °C, 20 °C and 30 °C. Tanner Tool EDA at 45nm process is used for simulation.

General Terms
CMOS, Power Consumption, Performance.

Keywords
Subthreshold, Voltage Scaling, Transistor Gating.

1. INTRODUCTION
The power consumption has become a major concern for the VLSI designers. This concern has aroused because of increase in the use of System On Chip (SOC) designs in mobile applications. The SOC design incorporates millions of transistors on a single chip which causes a huge amount of power dissipation in the circuit. With ever increasing demand of portable devices, PDAs and Personal Communication devices, the abatement of power will play a pivotal role in improving the battery life.

Recent years have shown that for ultra-low power applications, subthreshold logic circuit appears to be a favorable technique [1], [2]. In subthreshold logic design, the device operates at a supply voltage which is less than the threshold voltages of the transistors. This helps in abatement of both dynamic and leakage power. However, an excessive scaling of the supply voltage may degrade the performance of the circuit and can make it highly sensitive to process variations and temperature [3].

The total power dissipation (P_{TOTAL}) in any CMOS design is composed of two parts, dynamic power (P_{DYN}) and static power dissipation (P_{LEAK}). P_{TOTAL} is the sum of P_{DYN} and P_{LEAK}. The dynamic power is given by the equation $P_{DYN}=CV^2f$ [4], where C is the circuit loading, V is the supply voltage (V_{DD}) and f clock frequency. V_{DD} supplies the circuit's parasitic capacitance during switching and hence most of the power is consumed as dynamic power. So this voltage should be controlled in order to keep dynamic power within tolerable levels. The static power dissipation occurs when the input(s) applied to a logic gate and the corresponding output of that logic gate is not changing. Current trends show that the static power dissipation becomes comparable to the dynamic power dissipation as the supply voltage and technology scales down.

In this paper, a new technique is proposed that combines Voltage Scaling and Transistor Gating technique to suppress both dynamic and static power dissipation and hence reducing the overall power consumption. The Voltage Scaling technique reduces dynamic power dissipation without degrading the circuit performance. The static power is repressed through Transistor Gating technique. The circuit operates in subthreshold region which will further curtail the total power consumption. The proposed technique (VS-TG) consumes 30% to 90% less power than its CMOS counterparts. The rest of the paper is organized as follows: Section 2 presents a review of the related work. Section 3 analyzes Voltage Scaling technique. Section 4 analyzes Transistor Gating technique. Section 5 presents the proposed work and its operation. This is followed by Section 6 which comprises of simulation results. It also includes the comparison of proposed design with its CMOS counterparts. The quantitative description is also shown. Section 7 concludes the paper and presents the future scope of the proposed technique

2. LITERATURE SURVEY
Many techniques have been devised to reduce subthreshold leakage. The Power Gating [4] technique is one of them where the supply voltage is cut off when the circuit is in standby mode. This technique involves the use of PMOS and/or NMOS transistors called sleep transistors, which are interpolated in between power supply or ground and circuit. When the circuit is in active mode, these sleep transistors are turned on and are turned off when the circuit is in idle state.

Another technique to suppress leakage power is Multiple Threshold Voltage CMOS (MTCMOS) technique [5]. It is an alteration to Power Gating technique. The sleep transistors are high threshold devices which are connected to low threshold transistor of logic gates. This enhances the performance of the circuit by using low threshold transistors while at the same time it curtails the power consumption through high threshold sleep transistors. In [6] Dual Threshold Voltage (DTV) technique is proposed. Low threshold transistors are used in the critical paths to maintain the performance of the circuit while non-critical paths incorporate high threshold transistors to reduce leakage power.

To curtail dynamic power dissipation switching activity or supply voltage has to be lowered. In [7] a high performance and low power consumption technique is proposed. This technique incorporates Voltage Scaling and Stacked transistor technique for the abatement of overall power dissipation and the performance of the circuit has been improved. In [8] a hybrid approach is proposed which combines Dual Threshold Voltage (DTV) and Voltage Scaling technique. This technique is able to reduce overall power dissipation while maintaining the circuit performance.

3. VOLTAGE SCALING TECHNIQUE

Figure 1 shows the Voltage Scaling technique which helps in reducing the dynamic power dissipation without degrading the circuit's performance by voltage scaling and charge sharing.

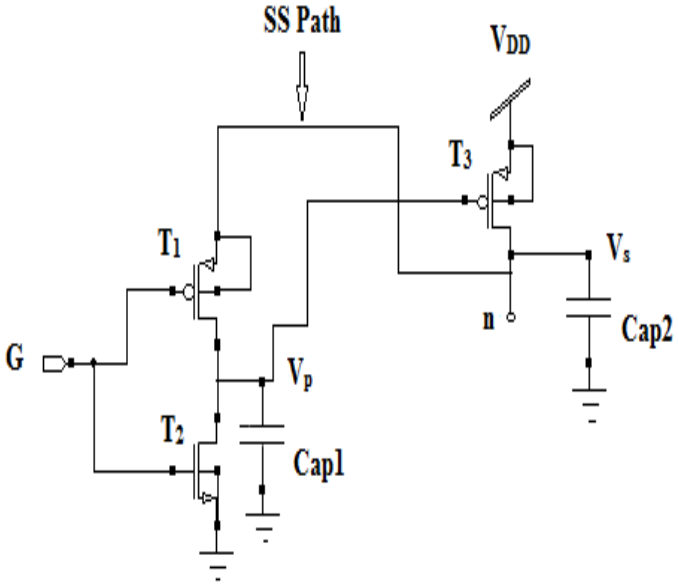

Fig 1: Voltage Scaling and Charge Sharing Circuit

In above technique the signal G is applied to transistors T_1 and T_2. When G is high, transistor T_1 is off while transistor T_2 turns on. This discharges the capacitor Cap1 and transistor T_3 gets turned on due to low voltage level of V_P. As a result the power supply voltage V_{DD} is fully supplied to the main circuit. When G goes low, transistor T_1 becomes active and transistor T_2 is in cut-off state. Now the current in T_3 will be determined by gate to source voltage difference in PMOS transistors. In this situation, the V_{sw} declines from V_{DD} to a lower voltage level. The capacitor Cap1 and Cap2 share charge through SS path known as Self Stabilization path. Hence the Voltage Scaling technique can be effectively utilized to abate dynamic power dissipation.

4. TRANSISTOR GATING TECHNIQUE

Subthreshold leakage increases as the technology scales down. Transistor Gating technique can be used to reduce static power dissipation. Figure 2 shows the Transistor Gating technique. In this technique, a high V_T PMOS transistor named gating transistor is placed in between the Pull-up network (PUN) and Pull-down network (PDN). Both PUN and PDN consists of low V_T transistors to maintain the performance.

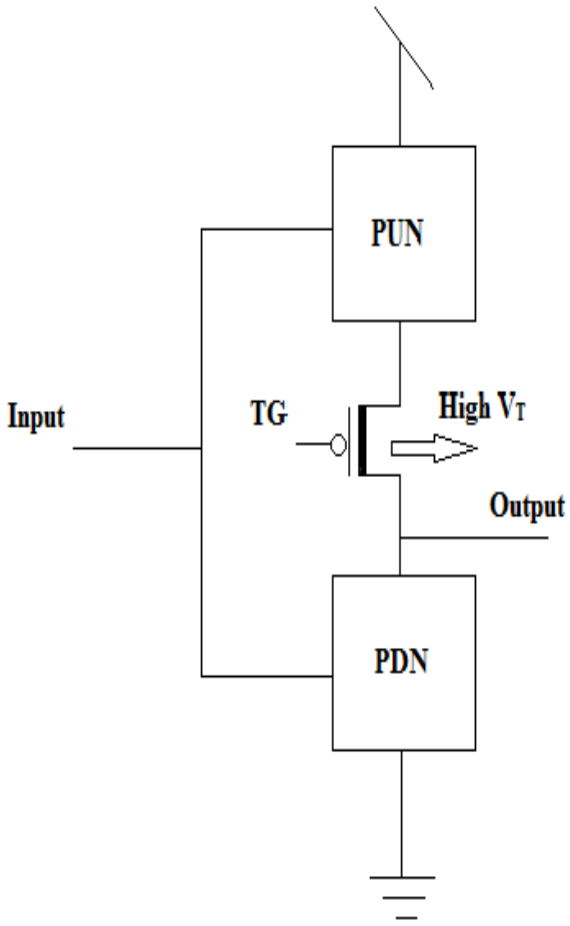

Fig. 2: Transistor Gating Approach

When the circuit is in active mode of operation, the gating transistor is turned on applying logic low signal TG at its gate. The circuit works as a normal CMOS circuit. During standby mode, the gating transistor is turned off. This increases the resistance of V_{DD} to ground path and hence minimizing the flow of leakage currents, resulting in reduction of leakage power.

5. PROPOSED TECHNIQUE

The proposed technique incorporates Voltage Scaling and Transistor gating (VS-TG) technique as shown in figure 3. The present technique employs Voltage Scaling technique to abate dynamic power while leakage power is reduced by Transistor Gating technique.

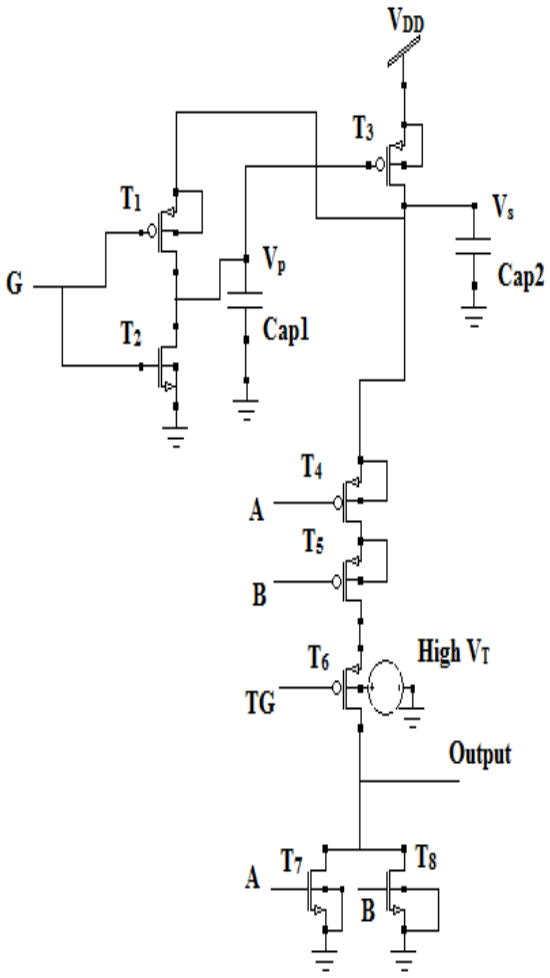

Fig 3: Proposed VS-TG Technique

The designed circuit operates in two modes: active mode and standby mode. During active mode of operation the gating signal TG is set to zero. The circuit will behave as a normal CMOS circuit when TG is set to 0. When G is high, transistor T_2 turns on which discharges the capacitor Cap1 and hence the low level of V_P makes the transistor T_1 to work in active region. Complete supply voltage V_{DD} is given to the circuit. When G becomes low, transistor T_3 will turn off. This causes the voltage level of V_S to decline and is governed by $V_{DD} - V_{T3}$ where V_{T3} is the threshold voltage of the transistor T_3. Capacitor Cap2 shares charge with capacitor Cap1 through the SS path when G goes low. During charge sharing the value of V_P gets too low which turns on the transistor T_3. This raises the voltage level of V_S and at the same moment it keeps the variations in V_{SW} to a low level. This reduces the dynamic power dissipation which is the primary aim of Voltage Scaling technique.

Apart from dynamic power dissipation, CMOS circuits have static power dissipation which occurs when the input(s) applied to a logic gate and the corresponding output of that logic gate is not changing. To abate static or leakage power Transistor Gating technique is proposed. When TG is 0 the circuit operates in active mode. In standby mode the TG is set to 1 which turns off the transistor T_6. This creates a high resistance path between supply V_{DD} and ground which helps in minimizing the flow of leakage currents. Ultimately, the leakage power is reduced.

Therefore the overall power consumption is reduced by the combined effect of Voltage Scaling and Transistor Gating technique. The present technique consumes less power as compared to conventional CMOS and Voltage Scaling approach.

6. SIMULATION RESULTS

The proposed design and other existing techniques are implemented on a 2-input NOR gate using Tanner EDA Tool for 45nm technology. The designs are simulated at 10 °C, 20 °C and 30 °C over various supply voltages. Power consumption for Conventional CMOS, Voltage Scaling and proposed technique at different temperatures is given in Table 1, 2 and 3.

The power consumed at 10°C by proposed technique outshines the Conventional CMOS and Voltage Scaling technique. VS-TG technique consumes 60.50% less power than Conventional CMOS at 0.6v while at 0.5v it saves 82.78% power. When VG-TS examined on 0.4v and 0.3v, the reduction in power consumption is 92.39% and 96.37%

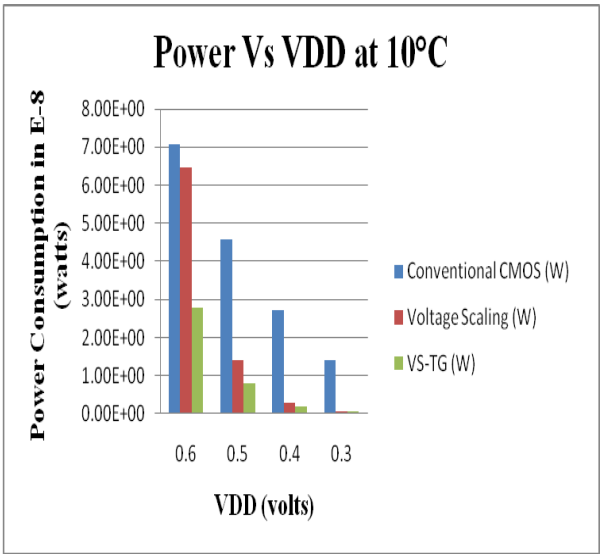

Fig 4: Power Consumption Vs VDD at 10°C

The same circuit consumes 56.79% less power than Voltage Scaling technique when operated at 0.6v. When examined on 0.5v the power consumption is reduced by 43.47%. At 0.4v and 0.3v the proposed method shows a 32.29% and 31.08% decrease in power consumption when compared to the Voltage Scaling technique.

Table 1. Power consumption of 2-input NOR gate at 10 °C

Power Consumption (W)			
V_{DD} (V)	**Conventional CMOS**	**Voltage Scaling**	**VS-TG**
0.6	7.067E-8	6.460E-8	2.791E-8
0.5	4.588E-8	1.397E-8	7.896E-9
0.4	2.734E-8	2.981E-9	2.078E-9
0.3	1.405E-8	7.382E-10	5.087E-10

Table 2 shows power consumption values of proposed and other techniques at 20°C. The proposed method reduces power by 61% to 95% as compared to the power consumption values of Conventional CMOS. The same circuit consumes 34% to 58% less power than Voltage Scaling technique when operated in subthreshold region.

Table 2. Power consumption of 2-input NOR gate at 20 °C

Power Consumption (W)			
V_{DD} (V)	**Conventional CMOS**	**Voltage Scaling**	**VS-TG**
0.6	7.598E-8	6.776E-8	2.895E-8
0.5	4.691E-8	1.524E-8	8.437E-9
0.4	2.792E-8	3.492E-9	2.303E-9
0.3	1.443E-8	9.140E-10	6.006E-10

Similar results are obtained when the designed circuits are operated at 30°C. The power is reduced by 51.61% and 57.27% as compared to the other techniques when operated on 0.6v. The proposed method shows a tremendous reduction in power consumption at 0.4v and 0.3v as compared to Conventional CMOS and Voltage Scaling technique. At 0.4v, the circuit consumes 96.18% and 29.04% less power and at 0.3v the power is reduced by 94.83% and 32.09%. Figure 5 and 6 shows the comparison of existing and proposed technique.

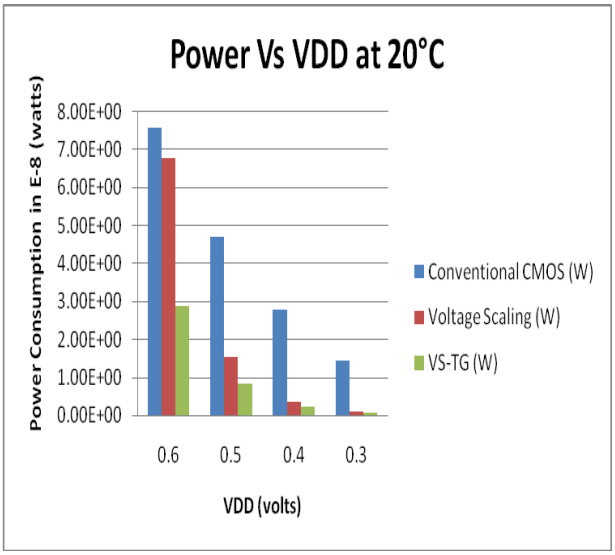

Fig 5: Power Consumption Vs VDD at 20°C

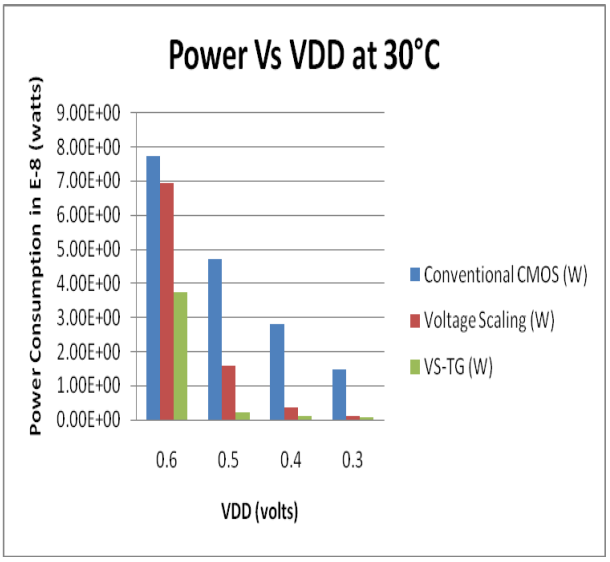

Fig 6: Power Consumption Vs VDD at 30°C

Figure 7 shows the variation in power consumption values at different temperature values for Conventional CMOS, Voltage Scaling and proposed VS-TG technique. The designed circuits are operated at 0.5v. The figure results show that the variation in power consumption values at different temperature values is least for the proposed technique. The proposed VS-TG methodology is less sensitive to temperature variations.

Table 3. Power consumption of 2-input NOR gate at 30 °C

Power Consumption (W)			
V_{DD} (V)	Conventional CMOS	Voltage Scaling	VS-TG
0.6	7.731E-8	6.934E-8	3.741E-8
0.5	4.712E-8	1.596E-8	8.711E-9
0.4	2.824E-8	3.693E-9	1.076E-9
0.3	1.463E-8	1.022E-9	7.553E-10

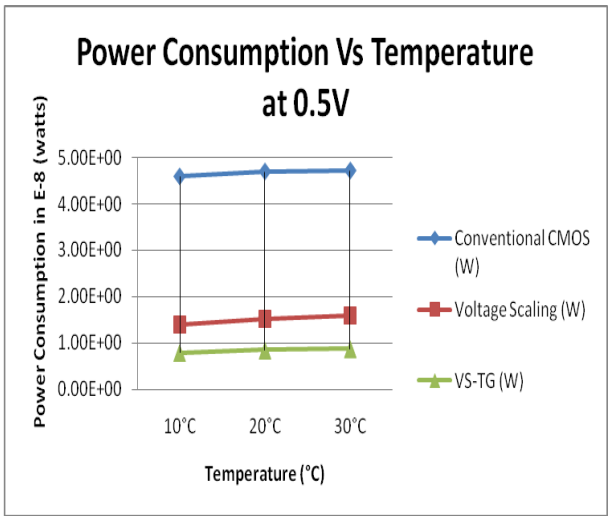

Fig 6: Power Consumption Vs Temperature

7. CONCLUSION

In this brief, a novel power efficient methodology using Voltage Scaling and Transistor Gating technique has been presented. Both static and dynamic power dissipation can be reduced by using additional circuitry that has been proposed in the present model. The proposed technique has reduced total power consumption by 30% to 95% and is superior to the existing design techniques. The variation in power consumption values at different temperatures is less, i.e. the circuit is less sensitive to temperature variations.

In future, the high threshold gating transistor will be optimized to study the effect of process variations on the performance and power consumption in CMOS circuits.

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