Low Power 3T XOR Cell using IDDG MOSFET

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ABSTRACT
In this paper, a new design of three transistor XOR gate is proposed using Independent Driven Double Gate MOSFET to achieve ultra-low power in sub threshold conduction. The proposed design has been compared with the three transistor XOR implemented using Symmetrical Driven Double Gate MOSFET in sub threshold region. A three transistor XOR gate designed using Independent Driven Double Gate MOSFET is showing improved results in terms of power consumption with varying input voltage, temperature and operating frequencies. The simulation has been carried out on SPICE tool at 45 nm technology.

General Terms
Integrated circuits, MOSFET scaling.

Keywords
DG MOSFET, low power, sub threshold, XOR gate.

1. INTRODUCTION
The MOSFET has continually been scaled down over the past decades. Channel lengths of typical MOSFET were once several micrometers, but modern integrated circuits are incorporating MOSFETs with channel lengths of tens of nanometers. As a consequence of this minimum feature size of ICs, the number of transistors has increased over the time. When channel lengths are aggressively scaled down for high density integration and high performance, the practical and fundamental limits of MOSFET scaling poses tremendous challenges beyond the 45nm technology node [1]. These limits are mainly identified to be severe short channel effects including threshold voltage roll off, sub threshold slope degradation and strong drain induced barrier lowering. These effects lead to unacceptably high leakage current and constitute the limiting factors of MOSFET scaling. As dimensional scaling of transistors is reaching its fundamental limits, various researches have been actively carried out to find an alternative way. Among these efforts, Double Gate MOSFET (DG MOSFET) devices have been well recognized for their advantages in deep sub 45nm technology [2]. DG MOSFET is a newly emerging device that can potential further scale down MOSFET technology owing to its excellent control of short channel effects.

The DG MOSFET is of the same material as the bulk MOSFET i.e. silicon but it has a different structure. It has two gates namely front gate and back gate. DG MOSFET comprised of a conducting channel (usually undoped) surrounded by gate electrodes on either side [3]. It offers better control of short channel effects [4] arising from the use of the two gates with an ultra-thin body and high drive current per device width resulting from high mobility due to low transverse electric field and higher inversion carrier density from the two channels. The DG MOSFET need not require drastic changes in the existing CMOS process technology. The thin channel is sandwiched between the two gates. When the properties of both gates such as gate work function, gate oxide thickness and bias are identical, the device is called Symmetrically Driven Double Gate (SDDG) MOSFET otherwise it is an asymmetrical or Independent Driven Double Gate (IDDG) MOSFET [5]. There are two operating modes of DG MOSFETs: three terminal or SDDG and four terminal or IDDG mode. The SDDG mode refers to the situation where the two gates of DG MOSFET are electrically connected and switched simultaneously whereas in IDDG mode, the two gates are biased differently with only one gate switching.

Sub threshold design for digital applications has been gaining momentum over the past decade. In sub threshold circuits, the supply voltage is reduced well below the threshold voltage of a transistor. Due to quadratic reduction in power with respect to supply voltage, sub threshold circuits are classified as ultra-low power circuits. The use of sub threshold circuit designing is always needed in digital circuits like full adder, multiplier, comparator and parity checker. The XOR gate is one of the most significant parts of these digital circuits. The aim is to propose a new topology for a simple XOR function using DG MOSFETs for design that can be adapted to operate in sub threshold region for various operating conditions. Two Single Gate MOSFET transistors have been connected in parallel in such a way that their source and drain are connected together to construct and design Double Gate MOSFET using equivalent approach [6], [7].

The paper is organized into five sections. Section 1 discusses about the general picture and introducing concepts of DG MOSFET. Section 2 illustrates the three transistor XOR gate design with Symmetrically Driven Double Gate MOSFET. A new topology of three transistor XOR gate with Independent Driven Double Gate MOSFET is proposed in section 3. Through simulation results, the behavior of proposed design is analyzed and compared with SDDG based 3T XOR gate at various operating conditions in section 4. Finally, section 5 summarizes the work and reflects on the results of the simulated designs.

2. 3T XOR WITH SDDG MOSFET
The circuit diagram for the three transistor XOR gate using Symmetrically Driven Double Gate MOSFET is presented in Fig 1. The three transistor XOR gate with SDDG MOSFET is obtained by replacing conventional Single Gate MOSFET devices with new Symmetrically Driven Double Gate MOSFET devices in 3T XOR gate proposed by S. R. Chowdhury et al. in [8]. In this XOR gate, minimum sizing is used for p-type SDDG MOSFET and n-type SDDG MOSFET. The W/L ratios for both p-type SDDG MOSFET and n-type SDDG MOSFET transistors are taken as 1/1.

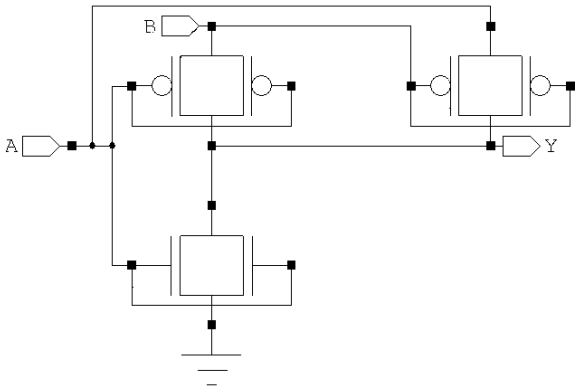

Fig 1: Schematic of 3T XOR gate using Symmetrically Driven Double Gate MOSFET

The design of this XOR gate consists of a modified version of a CMOS inverter using SDDG MOSFET and a p-type SDDG pass transistor. The operation of the whole circuit is like a two input XOR gate but with double control of gate of both p-type and n-type SDDG MOSFET transistors that leads to enhancement of the on state drain to source current and prevents the leakage current to flow between drain and source terminals in the off state.

3. PROPOSED 3T XOR DESIGN USING IDDG MOSFET

The schematic of the new three transistor XOR gate using Independent Driven Double Gate MOSFET have been proposed in Fig 2. The back gates of p-type IDDG MOSFET and n-type IDDG MOSFET are connected to their respective sources. The output signal that passes at any given times is decided by two gate (control) signals. As input A and B changes only twice for complete set of inputs in a XOR function, power consuming transitions are more in SDDG 3T XOR gate. By connecting the back gate of n-type IDDG MOSFET constantly to ground will reduce these power consuming transitions. The W/L ratios for all IDDG MOSFET transistors are taken as 1/1. The proposed design reduces the threshold loss problem significantly as exists in SDDG implementation of 3T XOR gate. The independent gate control in DG devices is effectively used in proposed design to improve the power consumption.

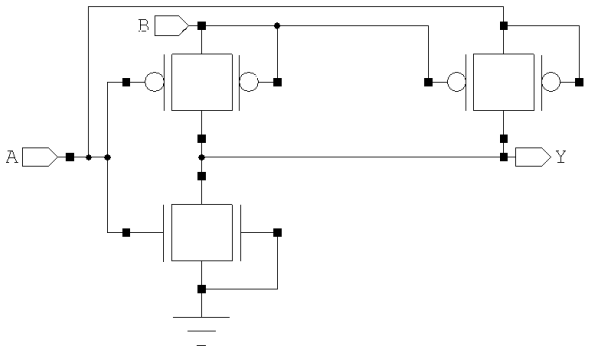

Fig 2: Schematic of 3T XOR gate using Independent Driven Double Gate MOSFET

4. SIMULATIONS AND COMPARISON

Extensive simulations have been carried out to analyze and compare the behavior of proposed 3T XOR gate using Independent Driven Double Gate MOSFET with the 3T XOR gate using Symmetrically Driven Double Gate MOSFET. Each circuit is simulated with same testing conditions. The circuits are simulated using SPICE tool at 45nm technology in sub threshold region.

Fig 3 shows the simulated waveform of the three transistor XOR gate with SDDG MOSFET and proposed design of 3T XOR gate with IDDG MOSFET. The waveform indicates that there is less degradation in the proposed 3T XOR gate using IDDG MOSFET output voltage with respect to the full scale input voltage value as compared to 3 transistor XOR gate using SDDG MOSFET. This could pave way for many new digital circuits using Independent Driven DG MOSFETs and allow for development of new generation circuit designs.

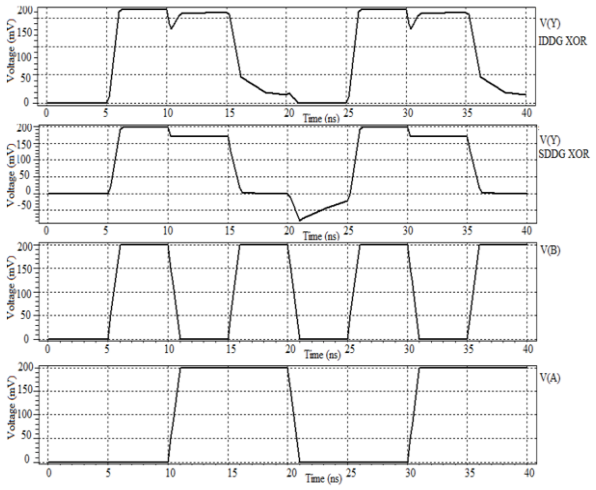

Fig 3: Simulated Waveform of 3T XOR gate with SDDG IDDG MOSFET

4.1 Variation with Voltage

Power consumption of the device increases with the rise in voltage. The supply voltage and input voltages are kept always less than the threshold voltage in order to operate in sub threshold region. The parameters like temperature and frequency are taken as 25˚C and 100 MHz respectively for voltage variations.

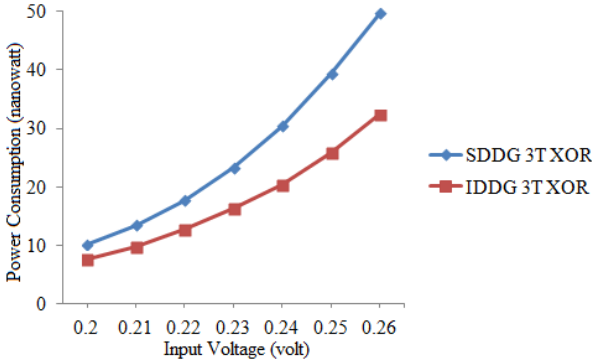

Fig 4: Power consumption versus input voltage

There is approximately 30% decline in power consumption of proposed 3T XOR design using IDDG MOSFET in comparison to 3T XOR implemented using SDDG MOSFET as depicted from the graph given in Fig 4. So these results reveal that the design using IDDG MOSFET can be better option for sub threshold operation.

4.2 Variation with Frequency

The SDDG and IDDG 3T XOR designs behavior are examined at increasing frequency as power consumption changes consistently when operating frequencies are varied. The value of the frequency variations are taken at a sub threshold voltage of 0.2V and room temperature i.e. 25˚C. The designs are compared up to the 300 MHz frequency.

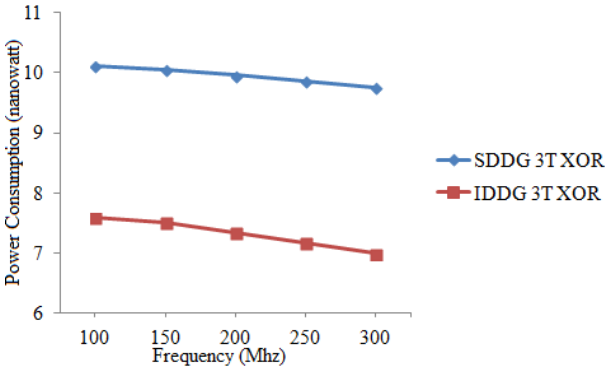

Fig 5: Power consumption versus frequency

It can be noticed from the graph plotted in Fig 5 that there is around 26% fall in power consumption when three transistor XOR designed with IDDG MOSFET. Hence proposed 3T XOR design using IDDG MOSFET can be more appropriate for high frequency applications.

4.3 Variation with Temperature

The response of SDDG and IDDG 3T XOR designs for incrementing temperatures are taken at a sub threshold voltage of 0.2V and frequency 100 MHz.

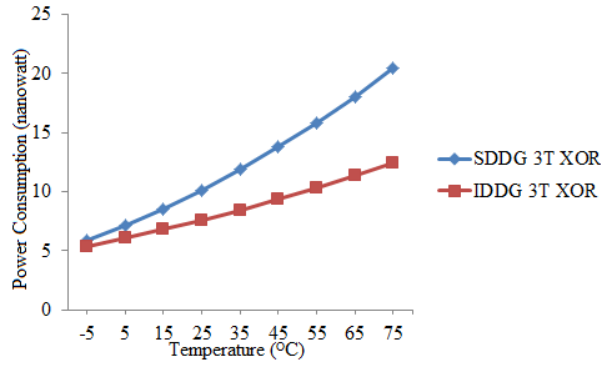

Fig 6: Power consumption versus temperature

As temperature varied in Fig 6, initially there is very small decrement in power consumption but on moving towards higher temperature there is a decrease of 25% to 35% in power consumption of 3 transistor XOR cell with Independent Driven Double Gate MOSFET when compared with the three transistor XOR cell using Symmetrically Driven Double Gate MOSFET.

5. CONCLUSION

A low power three transistor XOR cell using Independent Driven Double Gate MOSFET has been proposed and compared with SDDG implementation of 3T XOR gate in sub threshold region. The proposed design achieved around 20% to 30% less power consumption compared to the SDDG MOSFET implementation of 3T XOR cell at varying input voltages, increasing frequency and incrementing temperatures. Thus, the proposed design successfully corroborates the benefit of using independent gate control of Double Gate devices to achieve ultra-low power in digital circuit design in sub 45nm regime. The IDDG MOSFET has given better performance in terms of power consumption for sub threshold conduction. Many new digital circuits can be implemented in future for the development of new generation low power circuit design.

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