Modification in the Construction of Non-Binary LDPC Decoder using Stochastic Computation

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ABSTRACT

Low-Density Parity Check (LDPC) codes are linear block codes which perform closer to Shannon's limit. It is defined by the parity check matrix (PCM) which contains only a few ones in comparison to the number of zeros (sparsity). Stochastic based computation is a method to design low-precision digital circuits. In stochastic computing, probabilities are encoded by random sequences of bits. In this paper, we focus on the design of Relaxed Half Stochastic (RHS) based algorithm for Non-Binary LDPC decoder, with reduced hardware complexity and optimal decoding performance. Here Sum Product Algorithm (SPA) based variable nodes and stochastic based check nodes are integrated. Thereby the convergence speed of the algorithm is improved. The limitation of the complete stochastic decoder is based on the field order and the degree of variable node. This could be overcome by the method of RHS algorithm. The PCM (Parity Check Matrix) which defines the strength of the LDPC codes contains the non-zero elements. Increasing the sparsity of the PCM, helps in reducing the computation complexity. We propose two modifications in the PCM namely, LDM (Lower Diagonal Matrix) and DDM (Doubly Diagonal Matrix). Decoding performance measured in terms of bit error rate shows that non binary LDPC decoder outperforms than binary LDPC decoder.

General Terms

Algorithms, Decoder.

Keywords

LDPC, SPA, Stochastic computation, RHS, PCM.

1. INTRODUCTION

LDPC codes have become one of the most attractive error correction codes due to its excellent performance and suitability in high data rate applications. Stochastic decoding was used to decode binary LDPC codes in [1]. The number of operations per iteration required by the stochastic decoders and their complexity are less than FFT based decoder. SPA is an iterative algorithm for decoding LDPC codes in [2]. SPA uses soft information (probabilities) received from the channel and iteratively processes them. SPA makes decision by comparing final probabilities to a threshold value (hard-decision) at the end of the decoding process in [3]. Edge Memories (EM) are memories assigned to edges in the factor graph [4]. EMs are used to break the correlation between stochastic streams using re-randomization to circumvent the latching problem. Purely stochastic algorithm is designed to work over non-binary LDPC codes with some restrictions on the field order and variable node degree. To overcome this limitation, we prefer RHS algorithm. Non-binary RHS offers error-correcting performance matching that of the SPA with fewer iterations than the purely stochastic algorithm without restrictions on decodable codes.

Section II discuss about LDPC codes. Section III explains about the basics of stochastic computing. Section IV briefs about the construction of LDPC decoder and its basic blocks. Section V gives an overview about RHS algorithm. Section VI discuss about the modifications in PCM and its advantage over other algorithms. Section VII highlights the Performance analysis of the work. Finally we conclude the paper under Section VIII.

2. LDPC CODES

LDPC codes are defined over finite field referred to as Galois field (GF). In particular GF (q=2^p) = {0, 1…q^p – 1}, where q is a prime number or a power of a prime number. LDPC codes over GF (2^m), for m>1 consist of parity check matrix with Galois field elements {0, 1, 2 …2^{m-1}}.These are referred to as non-binary LDPC codes in [6]. LDPC code is a linear block code whose parity check matrix H has sparse i.e. number of non-zero elements. Specifically H contains a small fixed number of non-zero elements in its column and rows. The number of non-zero elements in its column and row referred to as column weight (w_c) and row weight (w_r) respectively. If the block length is N, then H characterizes an (N, w_c, w_r) code. These codes may be referred to as regular LDPC codes to distinguish from irregular codes. If the row weights and column weights of Parity check matrices are same size, then it is said to be regular LDPC codes. If the row and column weights vary for each row and column in the parity check matrix, then it is said to be irregular LDPC codes. Parity check matrices are mainly used for regeneration of code word, here there are many types of modified parity check matrices are proposed which corresponds to the size of the matrix.

3. STOCHASTIC COMPUTING

Stochastic computing (SC) is a collection of techniques that represent continuous values by stream of random bits [5]. Complex computations can then be computed by simple bitwise operations on the stream. A basic feature of SC is that numbers are represented by bit-streams that can be processed by very simple circuits, while the numbers themselves are interpreted as probabilities under both normal and faulty conditions. Multiplication can be performed by a stochastic circuit consisting of a single AND gate. Stochastic numbers are treated as probabilities; they fall naturally into the interval [0, 1]. This makes the normal add operation inconvenient because the sum of two numbers from [0, 1] lies in [0, 2]. Fig.1 shows the multiplication of two stochastic numbers which is simply using AND gate.
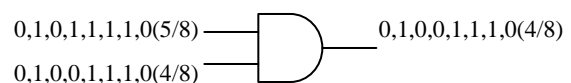

0,1,0,1,1,1,1,0(5/8) —— 0,1,0,0,1,1,1,0(4/8)
0,1,0,0,1,1,1,0(4/8)

Fig 1: Multiplication of two numbers using stochastic computing

4. ARCHITECTURE OF LDPC DECODER

Architecture of Non binary LDPC Decoder consists of following blocks which is shown in Fig.2. Non binary symbols are converted to stochastic numbers in non binary to stochastic converter block then the converted stochastic numbers are processed through Decoding block which consists of Check Node Unit (CNU) and Variable Node Unit (VNU).
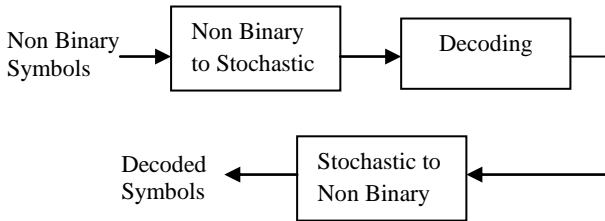

Fig 2: General block diagram for Non binary LDPC decoder

Finally the stochastic to non binary converter block converts non binary numbers to decoded symbols as output.

4.1 Non Binary to Stochastic Number Converter

Non binary to stochastic number converter converts a non binary number into a stochastic stream of binary numbers 0's and 1's respectively as shown in Fig.3. It consists of a random number generator and a comparator. A random number generator is the one which generates a number randomly for each clock cycle, for generating a random number Linear Feedback Shift Register (LFSR) is used. A linear feedback shift register (LFSR) is a shift register whose input is a linear function of a previous state. Mostly used linear function of a single bits is XOR, thus normally it is a shift register whose input is driven by XOR of some bits of the overall shift register value. When the given input binary number is greater than the random number, then the output is 1 otherwise it is 0. This forms a stream of binary data for various randomly generated sequences which is the stochastic number.
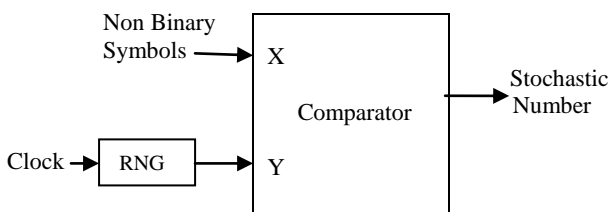

Fig 3: Non Binary to Stochastic Number Converter

Here Random Number Generator (RNG) is used to generate random numbers corresponding to the given clock pulse.

4.2 Design of Decoding Unit

The decoding unit consists of two units, a Check Node Unit CNU) and a Variable Node Unit (VNU).The converted output i.e. binary to stochastic number is given as input to the decoder block. In this block the channel probabilities are processed through CNU and VNU.

4.2.1 Check Node Unit

The stochastic number obtained as the output from the converter used in section B is fed as input to the Check node unit which primarily consists of the XOR gate and Flip-flop as

shown in Fig,4. This XOR gate realizes addition operation. The outputs obtained from the XOR gate is fed into the D-flip-flop, whose output is given to variable node unit.
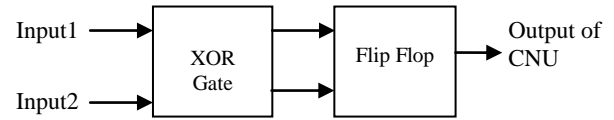

Fig 4: Check Node Unit

$$r_{nm}^a = \sum_{c:c_n=a} P[z_m \mid c] \prod_{i \in N(m)/n} q_{m_i}^{c_i} \qquad (1)$$

Where z_m, is the check node equation and c is codeword representation. If c satisfies check equation z_m, the value of $P[z_m \mid c]$ is 1, otherwise it is 0. r_{nm}^a is the received output of the Check node unit.

4.2.2 Variable Node Unit

After finishing the message update, VNU's outputs are written back into CNU's in next decoding iteration. VNU is the column wise processing also known as vertical step [7]. The following equations represent variable node updates. For each m and n,

$$q_{mn}^{a(i)} = a_{mn} f_n^a \prod_{m' \in M(n)\backslash m} R_{m'n}^{a(i)} \qquad (2)$$

Where a_{mn} is a normalization factor chosen such that $\sum_{a=0}^{q-1} q_{mn}^a = 1$. The equation computes the product of all the variable node (apart from the one to whom the message is directed) who "vote" for a ($q_{mn}^{a(i)}$ messages), weighted by the prior f_n^a. $q_{mn}^{a(i)}$ is the received output of Variable node unit. Architecture block diagram for the variable node unit is shown in the Fig.5.It has three blocks namely two multipliers, adder and reciprocal block.
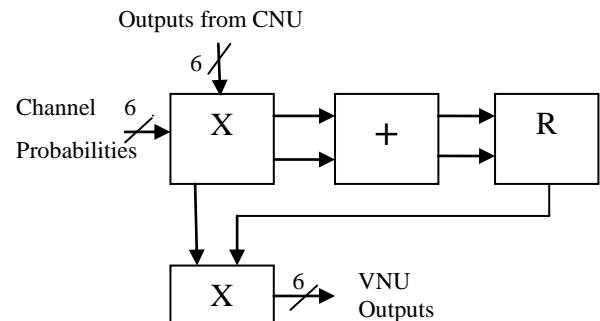

Fig 5: VNU architecture block diagram

Here the inputs are channel probabilities and from the CNU they are multiplied, added and then their results are reciprocated. The outputs of the reciprocal block with the

product of the inputs are again multiplied with Channel probabilities which give the VNU outputs.

4.3 Stochastic to Non binary Number Converter

Stochastic to Non binary number converter consists of a counter. This forms the last block in the non binary LDPC decoder architecture as shown in Fig.6. A stochastic number obtained from the variable node update is given to the counter in the converter. Thus the transmitted non binary data is decoded successfully using the stochastic computation technique.
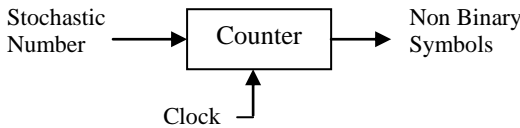

Fig 6: Stochastic to Non Binary Number Converter

5. RELAXED HALF STOCHASTIC ALGORITHM

RHS based LDPC decoder uses an SPA variable node and a stochastic check node. Using the SPA variable node removes the speed bottleneck from the decoder, thereby significantly decreasing the number of iterations required by the decoder compared to the stochastic one; while the stochastic check node reduce the complexity compared to the SPA decoder. Non-binary RHS decoder follows a similar approach; it uses SPA variable nodes, but a stochastic check node as shown in Fig.7. [9].$\overline{U}_{pc}$ is a Probability Mass Function (PMF) message, from node p to node c in the direction of a check node. V_{cp} is a similar message, but in the direction of a variable node. There are two message types in the RHS decoder: SPA (PMF vectors) and stochastic (GF (q) symbols) messages.

Also there are two types of conversions are discussed. They are as follows:

- SPA-to-Stochastic Message Conversion
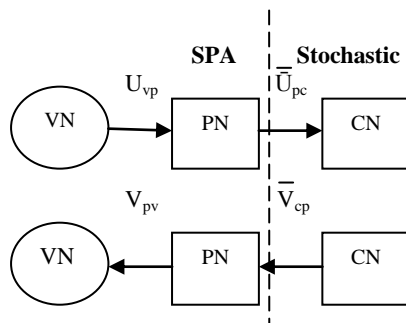
- Stochastic-to-SPA Message Conversion

Fig 7: Non Binary RHS based LDPC Decoder

5.1 SPA-to-Stochastic Message Conversion

The output message of a permutation node is used as a PMF to generate a GF (q) symbol which becomes the input stochastic message, U_{vp} to a check node. It should be noted that only one stochastic message is generated from an SPA message per iteration. This significantly reduces the routing complexity of the RHS decoder compared to the SPA one since in the former; a message sent to a check node is a GF (q) symbol.

5.2 Stochastic-to-SPA Message Conversion

The permutation nodes are SPA nodes, the stochastic output of check nodes, Vcp must be converted into a PMF message, Vcp. This is performed using successive-relaxation method. The PMF message Vcp is stored in memory and is initialized to an equiprobable distribution at the beginning of the decoding process. Thus RHS algorithm works as a reduced complexity algorithm for decoding codes over large fields without sacrificing error-correcting performance. It is a versatile algorithm which works for codes over different fields, rates, and construction methods.

6. MATRIX CONSTRUCTIONS

In general the PCM is generated in random for the coding purpose. With the randomly generated PCM, we propose two modifications to reduce the computation complexity, retaining the structural properties of PCM in [11]. We also analyze the decoding performance of the corresponding codes using proposed modified PCM structures. The two modifications are namely

- Lower Diagonal based PCM (LDM)
- Doubly Diagonal based PCM (DDM)

6.1 Lower Diagonal based PCM

First structure, LDM has two parts, second part consist of identity matrix. In the first part, the lower left corner half of the matrix has its diagonal element as '1'.

The following steps explain the LDM structure.

- Divide the PCM into two parts.

- First part consists of Random matrix in which the lower left corner half of the diagonal elements are set as '1'.

- Second part of the matrix is set as Identity matrix.

$$H_{LDM} = [R_{ML} | I_M] \qquad (3)$$

Second part of the matrix is the identity matrix and in the first part lower left corner half of the diagonal element is '1'.The importance of the placement of IM defines the computation complexity and decoding performance of this kind of Non binary LDPC code. With the better modifications, the merging of the I_M and R_{ML} can be done to improve the efficiency of the matrix structure framed. The combination of identity matrix and the random parity matrix, RM is introduced in the structure.

6.2 Doubly Diagonal based PCM

Second structure, DDM has its second part similar to LDM i.e. identity matrix. In the first all the diagonal elements are '1' and elements below to the diagonal elements are also '1'.

$$H_{DDM} = [R_{MD} | I_M] \qquad (4)$$

7. PERFORMANCE ANALYSIS

The significance of the proposed matrix structures are analyzed with the computation complexity involved in it. The analysis of the strength of each proposed modified PCM structures are done for the matrix size of (324 × 648). The simulation results of Non Binary LDPC codes were performed using MATLAB. The number of bit errors is the number of received bits of a data stream over a communication channel that has been altered due to noise, interference, distortion or

bit synchronization errors.Non-binary LDPC decoder has better decoding performance compared to binary LDPC codes. Among the decoding algorithms of non-binary LDPC, we infer that FFT-SPA based decoder has the better performance. Two modifications to the PCM structures are proposed, to reduce the computation complexity and thereby also improving the decoding performance. Two proposed matrices namely LDM and DDM were defined for the code (324,648) over GF (4). The decoding performances of the code with proposed matrices are analyzed in terms of the BER.
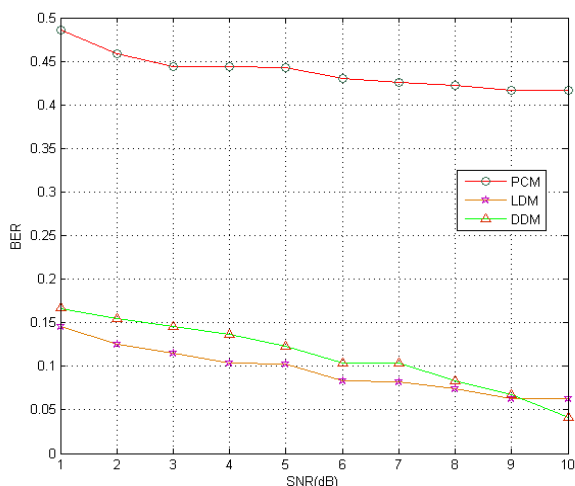

Fig 8: Comparison of PCM, LDM and DDM with reduced configurations for GF (4) for code length 648

It is interesting to note that the proposed matrices based Non-binary LDPC decoder provides a far better performance than the random PCM based decoder. Analyzing the decoding performance of the Non-binary LDPC decoder with different matrices from fig.8 , it is evident that the decoding performance of LDM based non-binary decoder is excellent compared to the DDM based Non-binary LDPC decoder. Another significant analysis to be done with respect to the decoder architecture is the computation complexity. The major computations involved in the decoding process are the multiplication unit and adder unit. The analysis on the number of computing blocks needed is presented in Table 1. The factors which identify the computation strength are the field order and the row weight of the PCM. The formulation on the computation strength is also given in the Table 1.

Table 1. Computation analysis of PCM, LDM and DDM

Processing Unit	Computations	PCM	LDM	DDM
CNU	Multiplications $[qmw_r(w_r-2)]$	31104	3888	5184
	Additions $[2(q-1)qmw_r]$	46656	31104	31104
VNU	Multiplications $[qnw_c(w_c-1)]$	15552	5184	15552
	Additions $[(q-1)w_cn]$	5832	5184	3888

From the above tabulated results we can infer that the CNU multiplications, the percentage has reduced up to 87.5% in LDM and up to 83.3% in DDM when compared with the PCM.The percentage of multiplications in VNU has reduced up to 66.67% in LDM and DDM when compared with PCM.

8. CONCLUSION
Non Binary LDPC Decoder based on stochastic computation, has been constructed with the proposed two different matrix structures. The decoding capability of the designed decoder with these code construction methods is analyzed. The corresponding variations in the computation strength of the algorithm are evaluated. The inferences are the improved decoding performance with the inclusion of the proposed matrix structures. The computation strength of the LDM structures are less compared to the DDM structures. It can be concluded that LDM based Non-binary LDPC decoder provides the optimized performance in terms of improved decoding capability and reduced computation complexity. In future the parameters like area, timing and throughput are to be evaluated with respect to the targeted device, Xilinx Spartan 3E. The design of architecture can be extended for the codes of higher order Galois Field and its hardware complexity will be analyzed.

9. REFERENCES
[1] Davey.M and MacKay.D , 1998, 'Low-density parity check codes over GF (q),' IEEE Communication Letters, vol. 2, no. 6.

[2] Declercq.D and Fossorier.M ,2007, "Decoding Algorithms for non-binary LDPC codes over GF (q)", IEEE Transactions on communication Letters, vol.55, no.4.

[3] Tehrani.S.S, Naderi.A, Kamendje.G.A, Hemati.S,Mannor.S, and Gross.W.J ,2010, "Majority-based tracking forecast memories for stochastic LDPC decoding," IEEE Transactions on Signal Processing, vol. 58, no. 9.

[4] Sarkis.G and Gross.W , 2012, "Efficient stochastic decoding of non-binary LDPC codes with degree-two variable nodes," IEEE Communication Letters, vol.16,no. 3.

[5] Gabi Sarkis, Saied Hemati, Shie Mannor and Warren J. Gross , 2013,"Stochastic Decoding of LDPC Codes over GF (q)", IEEE Transactions on communication Letters, vol.61, no.3.

[6] Guojun Han, Yong Liang Guan and Xinmei Huang , 2013,"Check Node Reliability-Based Scheduling for BP Decoding of Non-Binary LDPC Codes", IEEE Transactions on communication letters, vol. 61, no.3.

[7] Gallager R.G , 1962," Low-Density Parity-Check Codes", IRE Transactions on Information Theory.

[8] François Leduc-Primeau, Saied Hemati, Shie Mannor and Warren J. Gross , 2013," Relaxed Half-Stochastic Belief Propagation", IEEE Transactions on communications, vol.61, no.5.

[9] Gaudet.V and Rapley.A , 2003, "Iterative decoding using stochastic computation," Electronics Letters., vol. 39, no. 3.

[10] Tehrani.S.S, Gross.W, and Mannor.S , 2006, "Stochastic decoding of LDPC codes," IEEE Communication Letters, vol. 10, no. 10.

[11] Jingyu Kang, Qin Huang, Li Zhang, Bo Zhou, and Shu Lin, 2010, "Quasi-Cyclic LDPC Codes: An Algebraic Construction" IEEE Transactions,International Conference, vol.58, pp.1383-139

[12]