Design Techniques for Self Voltage Controllable Circuit on 2:1 Multiplexer using 45nm Technology

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ABSTRACT
Reduction of power dissipation is one of the most important challenges in VLSI circuit design. Due to scaling, sub threshold leakage current plays a dominant role in total power dissipation. This paper illustrates application of power saving SVL technique on 2:1 NAND MUX architecture. This application offers significant reduction in leakage power and leakage current viz-a-viz previous techniques. Self controllable Voltage Level Circuit (SVL) technique drastically reduces stand by leakage power and leakage current of CMOS logic circuits. This technique compare the optimization of leakage current and leakage power using two different design of 2:1 MUX. First is conventional MUX and other one is NAND based 2:1 MUX. The performance of this designed circuit is realized on a standard 45nm technology by using 0.7v supply voltage. It is easily concluded that this 2:1 nand based MUX achieves 651.9 Pw leakage power (Pst) and leakage current 1.020nA in standby mode, Where as conventional MUX achieved 2.04nA leakage current and 0.5nW leakage power.

Keywords
SVL, LSVL, USVL, Stand- by mode

1. INTRODUCTION
Battery driven system needs low leakage power [1]. The two well known techniques that reduces leakage power (Pst) are Multi –threshold-voltage CMOS (MTCMOS) and Variable-threshold-Voltage CMOS (VTCMOS) [2]. MTCMOS reduces leakage power (Pst) effectively by disconnecting the power supply through high Vt MOSFET switches. In spite of this, there are major drawbacks with the use of MTCMOS technique.[3] these drawbacks are non retention of data by memories and flip-flop. The other one is Variable-Threshold-Voltage CMOS (VTCMOS) [4]. It reduces leakage power (Pst) by increasing the substrate biases. It also faces some valuable problems, such as large area and lower power due to substrate bias supply circuits. For solving the problem of both these techniques, a small leakage current reduction circuit called Self- Controllable-Voltage level circuit (SVL) has been developed, that not only reduces leakage power but also retains data during stand by period. In this paper this technique is applied on 2:1 NAND based MUX that is heart of VLSI designed circuits.

1.1: In digital circuit, power dissipation takes place during three stages of the circuit: static, dynamic and short circuit. Between these power dissipation stages, dynamic switching power plays major role in modern digital circuits [5].

$$\text{Pswitching} = \text{Cpd} \times \text{V} \times \text{f1} \qquad \text{eq 1}$$

Here C_{pd} is dynamic power dissipation capacitance. In this equation, V is the supply voltage and f1 is the input signal frequency. Now days the battery operated circuits are in demand and device's power consumption has become a major concern of integrated circuit designers. To reduce the overall power consumption, the well known technique is to scale supply voltage, but this scaling results into exponential increase in the leakage current [6]. The sub threshold leakage current (I leakage) can be assessed as (approximately) [7]

$$\text{.Ileakage} = \text{Ioe}(\text{Vgs} - \text{Vth})/\eta\text{V}\tau \qquad 2$$

Where

$$I_0 = \mu_0 \text{ Cox } (W/L)V^2\text{Te}^{1.8}$$

C_{ox} is the gate oxide capacitance; (W/L) is the ratio of width to length of the leakage MOS device. μ_0 is the zero bias mobility. Vgs is the gate to source voltage, V_T is the thermal voltage that is about 26mv at T= 300K and η is the coefficient of sub threshold given by 1+(Cd/Cox) where Cd being the depletion layer coefficient [8]. Voltage scaling is an effective method to reduce energy-per-operation due to the association between switch energy and supply voltage. In microprocessors to scale down the supply voltage, dynamic voltage scaling has been used where a task is completed just before the deadline and which leads to saving of significant quantum of energy [9],[10].

$$Isub = \mu.Cox.\frac{W}{L}.(m-1).V^2\tau.\exp\left(Vgs - \frac{Vth}{mV\tau}\right).(1-\exp(-\frac{Vds}{V\tau}) \qquad 3$$

Where

μ - Mobility,

Cox - Oxide capacitance,

W - Width,

L - Length,

m - Sub threshold slope factor,

V_T - Thermal voltage,

V_{th} - threshold voltage,

V_{gs} - Gate-source voltage,

V_{ds} - Drain-source voltage,

n - Length of inverter chain,

η - Fitting coefficient,

Recent publications shows that microprocessors operate at clock frequencies of hundreds of KHz at 300-400mv [11]-[14].

2. "SELF CONTROLLABLE VOLTAGE LEVEL CIRCUIT" (SVL)

When the load circuits are in active mode, the SVL circuit supplies the maximum DC voltages to ($Vdc_{)}$ them through switches that are turn ON. Thus the load circuit can operate rapidly. Otherwise when the load circuits are in standby mode, it supplies slightly lower V and relatively higher V to them through "ON SW", so the drain-source voltages of the "0ff MOSFETs" in the states and Vsub decreases. So Vth increases consequently sub threshold current decreases. It results into reduction of power in static stage (Pst) whereas data are retained and noise immunity will be high. The amount of gate leakage current has increased gradually and is probable to become analogous or even superior to the sub threshold leakage for future CMOS devices [15]. This has been proposed to decrease sub-threshold leakage in SRAM cells of the numerous techniques [16], [17], [18], apply a self-controllable switch (SVL) [19] in active mode which allows full supply voltage to be applied and decreased supply voltage appears to be proficient for reducing gate leakage currents as well.

2.1 Upper SVL (USVL)

The upper SVL circuit contains two PMOS connected in series and one NMOS in parallel of these two. A Clk is given to the NMOS. Both the PMOS are connected in series and there substrate are connected to each other and grounded

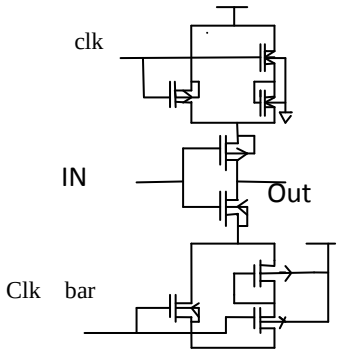

Fig 1 SVL technique on inverter

2.2 Lower SVL (LSVL)

It contains two NMOS connected in series and one PMOS connected parallel to them. Substrates of both the NMOS are connected to the Vdc and clock is given by PMOS connected parallel to the NMOS.

2.3 2:1 Mux (Conventional& Nand Based)

Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A Multiplexer is also called the data selector. They are used in CCTV and almost every business establishment that has CCTV installed. An electronic multiplexer makes it possible for several signals to share one device or resource, for example using one A/D converter or communication line instead of having one device per input signal. An electronic multiplexer can be considered as a multiple input, single output switch. In telecommunications and signal processing, an analog time division multiplexer (TDM) may take several samples of separate analogue signal and combine them into one pulse amplitude modulated (PAM) wide-band analogue signal. Alternatively a digital TDM multiplexer may combine a limited number of constant bit rates digital data streams into one data stream of a higher data rate. This is possible only by forming data frames consisting one time slot per channel. In case of 2-to-1 multiplexer, a logic value of 0 would connect to I_0 to the output while the logic value of 1 would connect I_1 to the output. 2-to-1 multiplexer has a Boolean equation where A and B are two inputs, Sel (S) is the selector input and Vout is the output

$$\text{Vout} = (\text{AS0} + (\text{BS1})$$

NAND based MUX contains three NAND gate and one inverter only. We have applied SVL technique on it basically for saving leakage power. Fig 5 shows the schematic of nand gate MUX. In this circuit when upper NAND gate in ON state then lower NAND gate will be in OFF state and in next cycle its vice- a-versa takes place. In the circuit, S is select line. Fig 8 shows the transient response of 2:1 nand based MUX. Fig 7 shows the layout of nand based 2:1 MUX. It has 14 transistors only. Fig 4 shows the diagram of conventional MUX form by 20 transistors. Whereas NAND based MUX contains 14 transistors only. Conventional MUX formed from AND gate, two OR gate and one inverter. Whereas NAND based MUX formed from one inverter and three NAND gates only.

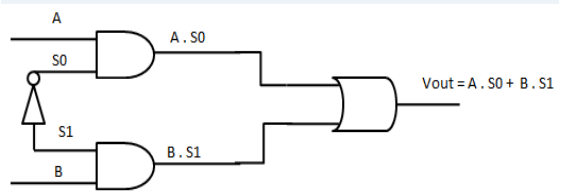

Fig 2 Schematic of conventional2:1 MUX

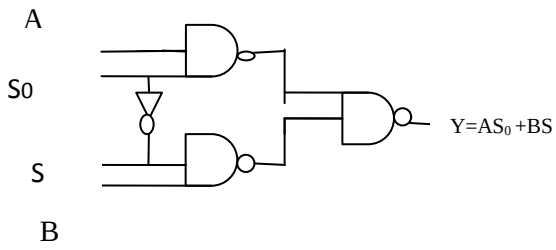

Fig 3 Schematic of NAND based 2:1 MUX

In the above Fig 2&3 shows two structures. Both are 2:1 MULTIPLEXER. In fig 2 schematic is formed by one OR gate, two AND gate and One inverter only. This structure contains 20 gates. Fig 3 shows schematic of 2:1 NAND based MUX. It is formed by three NAND gates and one inverter only. So the total no of gate in this schematic are 14 only. It shows that schematic of conventional MUX contains more gate in comparison to schematic of 2:1 NAND based MUX..

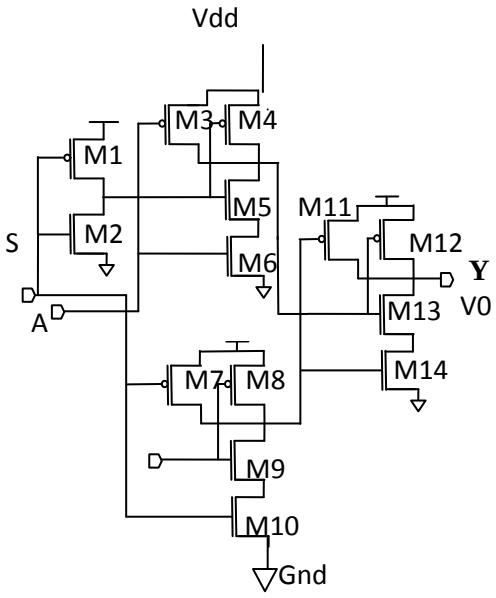

Fig 4 Shows schematic of 2:1 NAND based MUX

Due to these parameters such as leakage current, leakage power, and active power also vary or may be different for both the structures

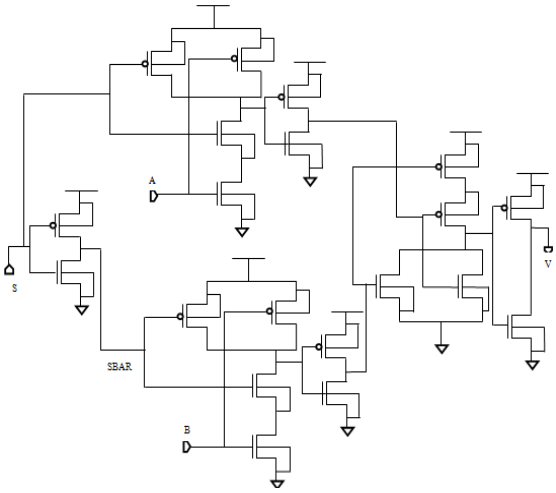

Fig 5 Shows schematic of 2:1 conventional MUX

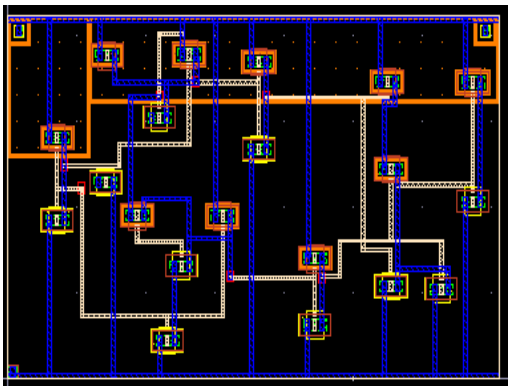

Fig 6 layout of convebtional 2:1 MUX

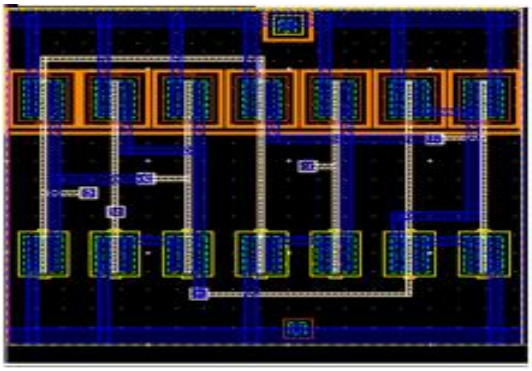

Fig 7 layout of NAND based 2:1 MUX

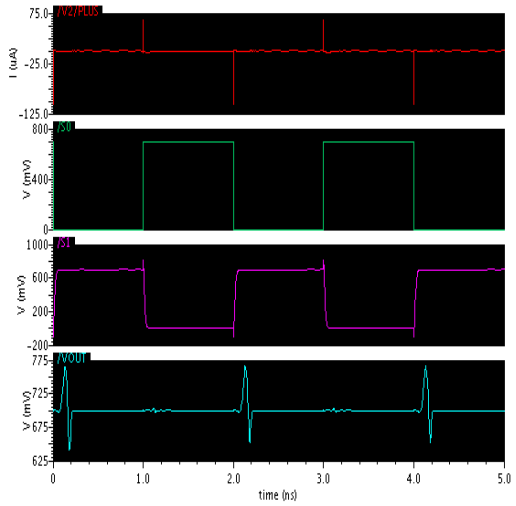

Fig 8 Transient response of NAND based2:1 MUX

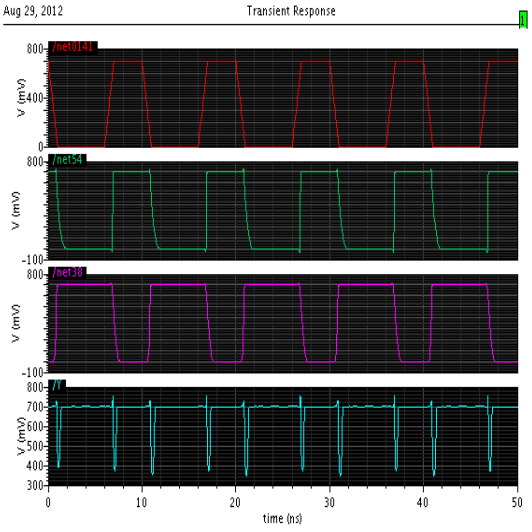

Fig 9 shows transient response of conventional 2:1 MUX

The self controllable voltage level (SVL) is known as a circuit for leakage power and the leakage current reduction .It consists of an (U-SVL) upper SVL circuit and (L-SVL) lower SVL circuit, where 2:1 MUX has been used as the load circuit.

2.4 SVL Circuit

In active mode of MUX circuit built-up SVL circuit supplies the maximum DC voltages (V_{DD} & V_{SS}) to the circuit through U-SVL and L-SVL circuits both are turned on simultaneously. Because of this the 2:1 MUX circuit can operate quickly .Whereas, when the MUX circuit is in standby mode, it supplies to some extent lower V_{DD} and relatively higher V_{SS} to them through "on SVL", so the drain source voltages of the "off MOSFET" in the standby MUX circuit decreases and Vsub increases. So, Vth increases and consequently, sub threshold current decreases, so (standby power) Pst is reduced, while data are retained and noise immunity will be high. In the "cut-off" condition of MOSFETs the increase in VBGs will increase the Vts. The schematic of 2:1 MUX with SVL circuit is shown in Fig 9 and Output Waveform of 2:1 MUX with SVL Circuit is shown in Fig 10. The DIBL effect on nmos 1v in the stand-by MUX circuit incorporating the SVL circuit is further decreased, since Vdsn in this expression

$$Vdsn = Vdd - mv \qquad (4)$$

Accuracy of the circuit is validated by measurements in [20] and [21].

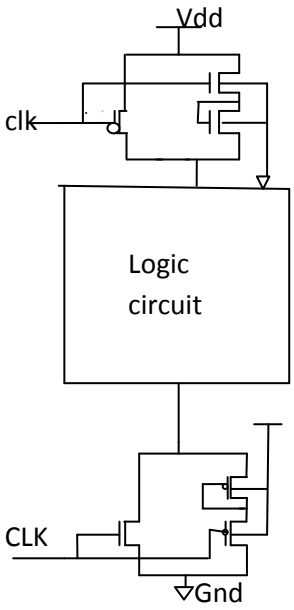

Fig 10 Schematic of SVL circuit on 2:1 MUX

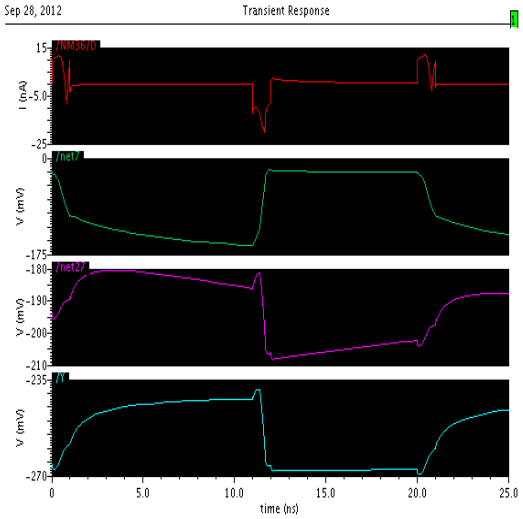

Fig 11 Transient response of MUX NAND based SVL circuit

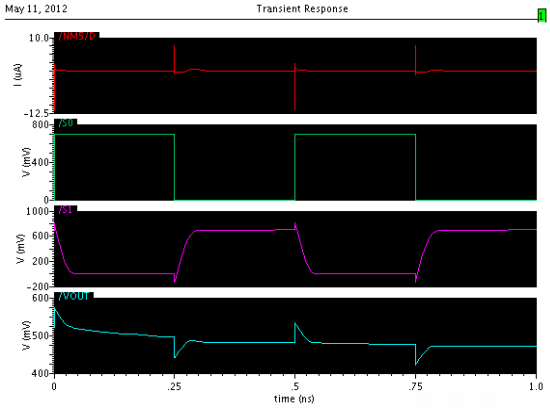

Fig 12 Output Waveform of 2:1 MUX with SVL Upper SVL Circuit

Upper SVL consists of a single pmos1v (PM18) and m-nmos1v (NM19,NM20) connected in series. The "on-pmos1v" connects a power supply (V_{DD}) and the MUX circuit is in active mode on demand, and "on nmos1v" connect power supply (V_{DD}) and the MUX circuit is in standby mode.The schematic of Upper SVL (U-SVL) is shown in Fig12 and the leakage power waveform of 2:1 MUX with U-

SVL is shown in Fig13Circuit

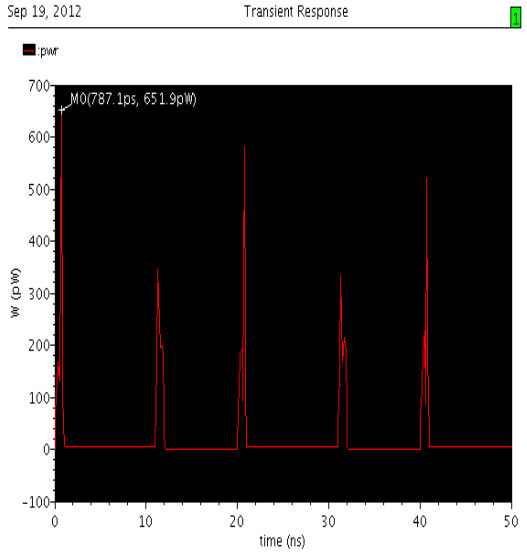

Fig 13 Power graph of 2:1 NAND based MUX

While gate voltage (Vg) of the stand-by MUX circuit is kept at "0", the pmos1v is turned on while the nmos1v is turned off. When control signal (USVLin) turns on nmos1v (NM19) and turns off pmos1v (PM18) V_{DD} is supplied to the MUX circuit through m-nmos1v. Thus, a drain-to-source voltage (Vdsn), that is, a drain voltage (V_D) of the "off nmos1v", can be expressed as

$$Vdsn = Vdd - mv \quad (5)$$

Where v is a voltage drop of the single nmos1v and Vdsn can be changed by varying m or v (or both). Reducing Vdsn by rising mv will increase the barrier height of the "off nmos1v"; that is, it will reduce the drain induced-barrier-lowering (DIBL) effect and, as a result, increase Vthn. This results in a decrease in the sub threshold current of the nmos1v (Istn); that is, the leakage current through the MUX circuit decreases.

2.5 Lower SVL circuit

The lower SVL circuit consists of single nmos1v (NM15) and m-pmos1v (PM16, PM17). Both pmos1v (PM16, PM17) are connected in series and nmos1v (NM15) is connected parallel to both pmos (1v). Substrate of both the pmos (1v) are connected together and connected to Vdd.. The L-SVL circuit not only ground connection V_{SS} to the active MUX circuit through the "on nmos1v" but also supplies V_{SS} to the standby MUX circuit through the use of the " on pmos1v".The schematic of 2:1 MUX with L-SVL Circuit is shown in Fig14 and the output waveform of 2:1 MUX with L-SVL is shown in Fig14. A negative control signal (LSVL in) turns on pmos1v (PM16) and turns off nmos1v so that V_{SS} is supplied to the stand-by MUX circuit with Vg of "0" (i.e., mv) through m-pmos1v. Thus, according to Equation (1), reduced Vdsn reduces Istn. Furthermore, source voltage (Vs) is increased by mv, so the substrate bias (i.e., back-gate bias) (Vsub), expressed by

$$\text{Vsub} = -\text{mv} \quad (6)$$

Both the reduction in the DIBL effect and the increase in the back-gate bias (BGB) effect lead to further increase in Vthn

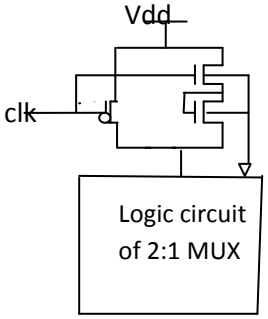

Fig 14 Schematic of USVL on 2:1 NAND based

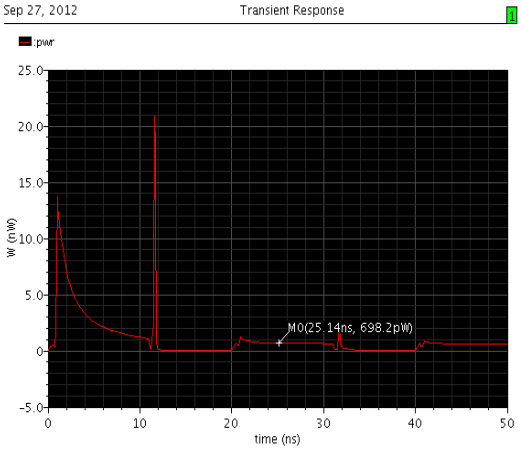

Fig 15 power graph of USVL on 2:1 NAND MUX

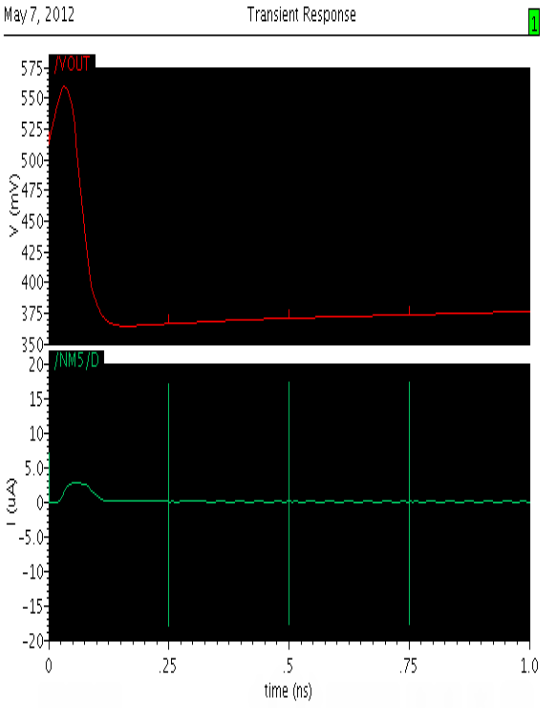

Fig 16 Output Waveform of conventional 2:1 MUX with U-SVL Circuit

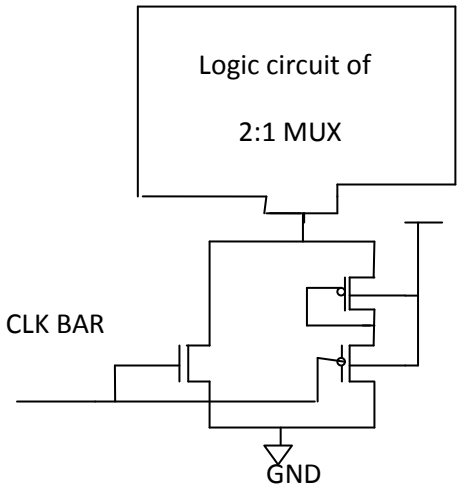

Fig 17 Schematic of LSVL circuit on 2:1 MUX

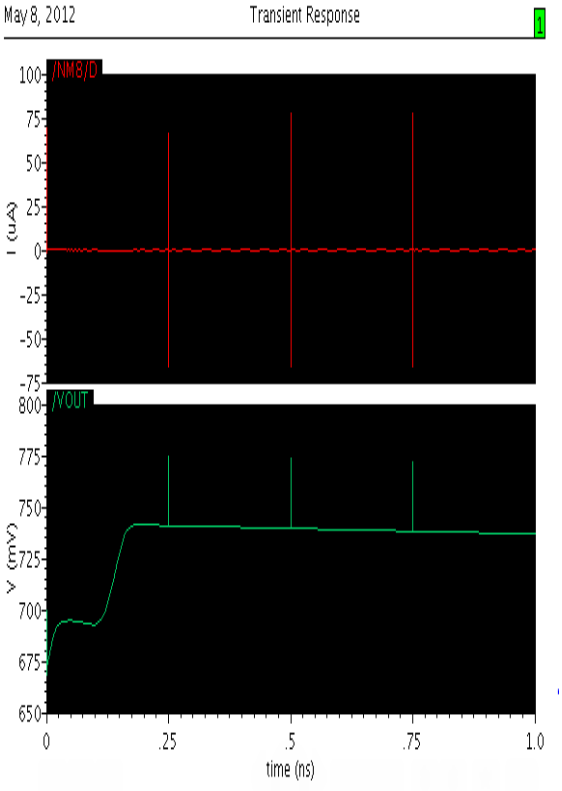

Fig 18 Output Waveform of conventional 2:1 MUX with LSVL Circuit

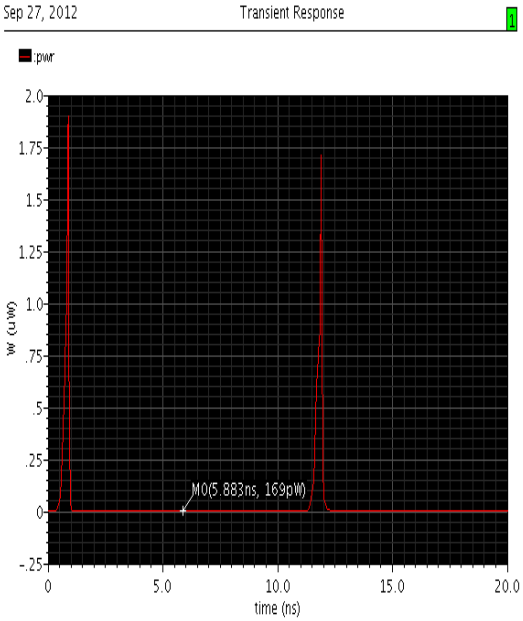

Fig 19 Leakage power graph of LSVL on 2:1 MUX

3. SIMULATION RESULT

This paper compares the result obtain by conventional 2:1 MUX and NAND based 2:1 MUX. There are two methods of structuring 2:1 MUX. Conventional MUX contains more no of transistor as compared to NAND based 2:1 MUX. it has only 14 transistors . Result shows that leakage power in pw when applying SVL circuit on nand based MUX, where as leakage current shows result in nA range. For the conventional MUX leakage power in nw and leakage current in nA range, when applying SVL circuit .Simulation result is measured by CADENCE VIRTUOSO Tool.

Table 1

Simulated Result Summary

Table Head	APPLIED TO 2:1 NAND based MUX			APPLIED TO CONVENTIONAL 2:1 MUX		
	USVL	LSVL	SVL	USVL	LSVL	SVL
Process technology	45nm CMOS	45nm CMOS	45nm CMOS	45nm CMOS	45nm CMOS	45nm CMOS
Supply Voltage	0.7V	0.7V	0.7V	0.7V	0.7V	0.7V
Leakage Power	698.2pw	169pw	651.9pw	1.915nW	1.03nW	0.5nW
Leakage Current	1.09nA	1.028nA	1.020nA	3.88nA	3.95nA	2.04nA

4. CONCLUSION

In this paper the effect of optimization of leakage current and leakage power is observed by application of SVL circuit on two different MUX structures such as 2:1nand based MUX and 2:1 conventional mux has been measured. The optimization of leakage current and leakage power through nand based MUX has been examined. The SVL circuit of 2:1 nand based MUX were designed using 45nm technology on CADNCE TOOL. The optimization of leakage power (stand-by-power) Pst and leakage current (stand-by-mode) has reduced significantly by applying SVL circuit on 2:1 nand based MUX. The result shows leakage power Pst as 651.9pw for 2:1 NAND based MUX, where as leakage current as1.020nA in the stand –by mode applying SVL circuit on 2:1 nand based MUX. For the conventional MUX these values are 0.5nW and 2.04nA only.

5. ACKNOWLEDGEMENT

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