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Selective Compression Techniques using Variable-to-Fixed and Fixed-to-Variable Codes

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ABSTRACT
Ìn this paper, we propose two code based techniques: Variable-to-Fixed codes and Fixed-to-Variable codes for power efficient test data compression. The proposed scheme with the aim of achieving high compression ratio and low power consumption relies on reducing, the number of bits for representing the original test vector and the number of transitions per second. Simulation results on ISCAS'89 benchmarks demonstrate that this optimization methodology helps achieve reduced test data volume and power than previous schemes for cases where the number of specified bits in the test set is relatively few.

Keywords
Variable-to-Fixed codes, Fixed-to-Variable codes, Test data compression, Compression ratio.

1. INTRODUCTION
System-on-chip (SoC) revolution challenges both the fields of designing and testing, as it nowadays integrates multiple cores on a single piece of silicon to bring about a wide range of functionality on a single die. With the number of transistors increasing rapidly, chips emerge with billions of transistors, and this number continues to grow over the years. Testing devices with this number of transistors, quickly, efficiently and thoroughly is a very challenging task and requires proper strategies and systematic test approaches. Testing is one of the most expensive and problematic aspects in a circuit design cycle and are affected by several challenges, such as high test data volume and high power consumption[1].

A circuit consumes much higher power in test mode than in normal mode, as switching activity of all nodes is often several times higher, when in test mode, due to the very low correlation between successive test vectors. This results in high rates of current in power and ground lines, excessive noise, large resistive voltage drop and thus ultimately giving rise to severe hazards in circuit reliability or even instant circuit damage (due to excessive heat dissipation). This calls for the need of Low Power Testing, which makes power management a critical parameter that cannot be ignored in test development. Considering the CMOS ICs, power dissipation is caused by static power and dynamic power. Static power is caused by the leakage current and is negligible, when compared to dynamic power consumed when the circuit is switching its state. For test vectors, dynamic power consumption during testing depends on number of transitions that occur during scan-in & scan-out operations. Thus dynamic power consumption & thereby power dissipation can be reduced by reducing the switching activity. This technique is made of use in this paper. There exists techniques to control power consumption in test mode and to overcome the limitations of ATEs. An alternative solution to ATE based external testing is BIST (Built-In-Self-Test). Circuit Under Test(CUT) can test itself with the help of a built-in hardware, primarily designed for testing the rest of the hardware of the CUT. BIST reduces dependencies on expensive ATEs and it allows pre computed test sets to be embedded in test sequences generated by BIST hardware. But this technique can be applied only if embedded cores are BIST-ready which requires redesigning the IP cores. Hence a more plausible solution for lowering test power is by Test Data Compression.

The rest of the paper is organized as follows: Section 2 presents a brief note on the related research efforts for improved test data compression. The proposed methodology is discussed in Section 3. Simulation results are shown in Section 4 and finally, conclusions are presented in Section 5.

2. RELATED WORK
Unlike compaction methods [2,3] that reduces the number of test vectors, compression methods do not alter the number of test vectors. Instead they reduce the number of bits per test vector. Compression schemes based on LFSR reseeding [4], relies on random value filling of unspecified bits, thereby increasing the switching activity with increased number of transitions. With conventionally followed methods of run length compression techniques based on encoding runs of zeros, such as golomb [5,6] and FDR [7] which fails to compress low power test sequences characterized by both long runs of zeros and ones, are not tailored to exploit the specific properties of pre computed test sets. Nine-Coded Compression Technique [8] is flexible in utilizing both fixed- and variable length blocks to develop exactly nine code words, and is efficiently adopted for single or multiple-scan chain designs in the reduction of test application time. A Block Merging Technique [9] depends on reducing the test data volume by merging the consecutive compatible test blocks, and has smaller number of codeword for larger block size.

Code-based schemes, performed after the test generation process using a software program, can be applied to both full scan & non scan circuits, & also soft and hard cores. Here the main advantage being that test data compression can be done without requiring any structural information about the embedded cores, and can achieve a good compression ratio, without much trade-off in test power.

3. PROPOSED METHOD
3.1. Introduction
Unspecified bits ('X') form more than 90% in a given particular test cube, where test cubes are the collection of unspecified bits which are represented as test patterns and tend to be highly correlated, generated by deterministic ATPG tools [10]. Also the number of transitions in a test cube are

smaller than the number of specified bits. Taking these facts into consideration, the proposed method of compression consists of exploiting these don't care bits and their redundancy in test patterns. Test data compression can be classified into categories depending upon how test patterns are handled in compression method, such as Fixed-to-fixed test pattern [11] and variable-to-variable test pattern. Here, compression is not targeted for all the test patterns [12] and is a selective run length-based compression of two code-based schemes: Fixed-to-Variable (F-V) & Variable-to-Fixed (V-F) methods, developed to meet the need for low power consumption and to achieve low test data volume. The test patterns having large number of don't cares are selectively chosen for compression.

Analysis of power is carried out for encoded compressed pattern by considering its switching activity. Power dissipation is considered during scan testing, as a circuit or digital system consumes more power in test mode when compared to normal mode [13]. Thus the objective of this proposed technique is to reduce the test data volume and thereby the switching activity of transitions.The design flow for the proposed compression technique, consists of a sequence of 5 steps, as is given in Fig 1.

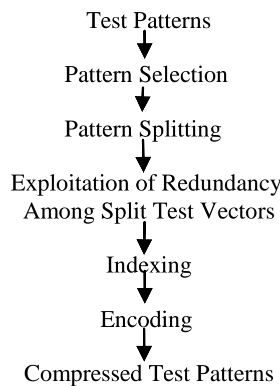

Fig 1: Design Flow for the Proposed Technique

3.2. Pattern Selection

The test vectors are initially input into the pattern selection block. Higher the probability of finding number of don't cares in a test vector, higher would be the maximum attainable compression ratio. Hence, the reference or critical value is calculated based on the higher and the most redundant count, which is obtained by the ratio of don't cares with the pattern length. With this being done, the test vectors can be selectively chosen into the next stage of compression, whereas the rest of the vectors remain as such, as can be shown from the example in Table 1. Here 5 vectors out of 7, are selectively chosen into the next stage, by taking thecritical value as 0.3. Those vectors having a value below the critical value are not taken into the next stage of compression, while the other test vectors are.

3.3. Pattern Splitting

The selected test patterns are being split into groups, preferably with suitable adding of zeroes for equal length split bit patterns, the pattern splitting being different for the formation of V-F & F-V codes. In V-F codes, the patterns are

Table 1. Pattern Selection

10X10X000X11000X001	MSS
1000XX0010101001X0X	MSS
X10X0101XX11XXX0111	MUS
01X11X1101110XX1XXX	MUS
1XX01XXX01101XX1110	MUS
1XX11X101X10XXX1XX0	MUS
XX1XXXXXXXXXXXXXXXX	MUS

randomly split and the final output code word can formed from different sets of the encoding table. While in F-V codes, the splitting is done with the intention of the resulting code word formed from a single set of the encoding table. Table 2 and Table 3 show the pattern splitting of the earlier shown vectors, for obtaining their V-F and F-V codes.

Table 2. Pattern Splitting of V-F codes

X10X0	101XX	11XXX	0111
01X11	X1101	110XX	1XXX
1XX01	XXX01	101XX	1110
1XX11	X101X	10XXX	1XX0
XX1XX	XXXXX	XXXXX	XXXX

Table 3. Pattern Splitting of F-V codes

X10X0101XX	11XXX0111
01X11X1101	110XX1XXX
1XX01XXX01	101XX1110
1XX11X101X	10XXX1XX0
XX1XXXXXXX	XXXXXXXXX

3.4. Exploitation of Redundancy among Split Test Vectors

Once Pattern Splitting is done, the frequency of occurrence of the code words, along a column, is maximized, thereby increasing the encoding efficiency of the statistical encoding. As defined in [9], two bits are *compatible* if they are the same or either one is a don't care bit (X), while two bits are *inverse compatible* if they are opposite or either one is an X. Therefore, two blocks are defined to be *compatible* (*inverse compatible*) if every corresponding bit is compatible (inverse compatible). For example, two 8-bit blocks 0XXX1010 and 010X10XX are compatible, while another two blocks 0XXX1010 and1X10XX01 are inverse compatible [14] These test patterns are compared with each other, found to be compatible and both transformed into 010X1010, by appropriate filling of the don't cares, to facilitate pattern similarity and taken into the next stage to facilitate similar indexing. This redundancy property of the split test vectors is exploited, in Table 4 and Table 5, respectively shown for the V-F and F-V codes, for obtaining similar patterns along a column.

Table 4. Exploitation of redundancy for V-F codes

X10X0	101XX	110XX	0111
01X11	X1101	110XX	1110
1X101	X1101	101XX	1110
1XX11	X101X	101XX	1110
1X101	X101X	101XX	1110

Table 5. Exploitation of redundancy for F-V codes

X10X0101XX	11XXX0111
01111X1101	110XX1XXX
1XX01XXX01	101XX1110
1XX11X101X	101XX1110
01111X1101	101XX1110

3.5. Indexing & Encoding

Table 6. Table for Encoding

	Conditions	Encoding results
Set 1	Tc≤2	0 1
Set 2	2 ≤Tc ≤4	00 01 10 11
Set 3	4 ≤ Tc ≤8	000 001 . . 110 111
Set 4	8 ≤ Tc ≤16	0000 0001 . . 1111
. . .	. . .	. . .
Set N	TNC ≤ M	M $\leq 2^N$

Next stage consists of Indexing the blocks of the test patterns (column wise). To similar test patterns, the same index values are given, starting from zero. As per the Total number of Compression(TC) decoding result (the limit of index values in the column), the next step of Encoding, column wise, is carried out, as per Table 6.

If TC decoding result, of indexing, is less than or equal to 2, the encoding will be done in single bit as per in set 1 and so on, as is shown in the specified encoding table 1. This encoded result, now considered row wise, forms the code words for the MUS test patterns.

With respect to compressed pattern if the variations are found in encoding bit value, then it is belongs to V-F category. If the pattern splitting is done according to encoding bit value, then it will come under F-V category. The Indexing and Encoding, and hence the final V-F and F-V code words for the test patterns, are shown in Table 7 and Table 8.

Table 7. Indexing and Encoding of V-F codes

Indexing	0	0	0	0
	1	1	0	1
	2	1	1	1
	3	2	1	1
	2	2	1	1

Encoding	00	00	0	0
	01	01	0	1
	10	01	1	1
	11	10	1	1
	10	10	1	1

Table 8. Indexing and Encoding of F-V codes

Indexing	0	0
	1	1
	2	2
	3	2
	1	2

Encoding	00	00
	01	01
	10	10
	11	10
	01	10

3.6. Calculation of Compression Ratio

The amount of compression using the V-F and F-V codes can be computed as follows:

$$CR\% = (T_D - T_E/T_D)*100 \quad (1)$$

where T_D, here refers to the original test patterns, before compression and T_E is the compressed test pattern obtained using the compression techniques.

3.7. Power Estimation

In this section, the impact of test set encoding on power consumption during scan testing, is examined. Scan in power is measured in terms of the number of transitions in the scan vectors. The weighted transitions metric (WTM) is used to estimate the power consumption due to scan vectors. This models the fact that the scan in power for a given vector depends not only on the number of transitions in it but also on their relative positions. For example, consider a scan vector v1v2v3v4v5= 01000, where v1 is first loaded into the scan chain. The 0-to-1 transition between v1 and v2causes more switching activity in the scan chain than the 1-to-0 transition between v2and v3 . The weighted transitions count metric [2] is also strongly correlated to the switching activity in the internal nodes of the core under test during the scan in operation. The scan vectors that have higher weighted transition metric dissipate more power in the core under test. The weighted transitions metric for tj ,denoted W T M , isgiven by

$$WTM_j = \sum_{i=1}^{l-1} (l-i)(t_{j,i} \oplus t_{j,i+1}) \quad (2)$$

T_D contains 'n' vectors t 1 ,t 2 , . . . , tn then the average scan in power, Pavg and the peak scan in power, Ppeak are estimated as follows, in Eq. (3) and Eq. (4).Here, 'l' is the scan chain length, 'i', bit position of each test vector and 'j' is the pattern number.

$$P_{avg} = \sum_{j=1}^{n} \sum_{i=1}^{l-1} (l-i)(t_{j,i} \oplus t_{j,i+1})/n \quad (3)$$

$$P_{peak} = \max_{j=\{1,2,\ldots n\}} \{ \sum_{i=1}^{l-1} (l-i)(t_{j,i} \oplus t_{j,i+1}) \} \quad (4)$$

4. RESULTS ANALYSIS

In order to validate the efficiency of the proposed technique, several experiments on the six large full scanned ISCAS'89 benchmark circuits have been performed. Table 9 shows the compression ratio attained by using the V-F and F-V coding on the test patterns of theses benchmark circuits. The compression ratios of the proposed techniques are then compared with that of the other existing methods [5],[7],[8],[9],[15],[16], as given in Table 10,and are found to be higher, with an average compression ratio of 86.15% and 89.95%, for V-F and F-V codes, respectively. Table 11 displays the average and peak power of both these techniques, on the benchmark circuits, while the average power consumed by V-F and F-V coding on original test patterns, are being compared with two earlier techniques [7], [17], using the ISCAS'89 benchmark circuits, in Table 12 and Table 13, to show their efficiency in reduced power consumption, also. A comparison between the Proposed Technique with other existing techniques, is illustrated in Fig. 2. , using the ISCAS'89 circuits.

Table 9. Comparison of Compression Ratios of V-F and F-V Codes

Circuit	Original DataVolume	Compression ratio(%) of V-F code over original data	Compression ratio(%) of F-V code over original data
S5378	23,754	80.40	85.90
S9234	39,273	77.90	85.40
S13207	1,65,200	93.85	94.81
S15850	76,986	92.43	93.68

Table 10. Experimental Result of Proposed Compression Method (V-F & F-V codes) with Other Existing Methods

Circuit	Golomb%	FDR%	9C%	RLHC%	SHC%	BM%	V-F%	F-V%
S5378	37.11	47.98	51.64	53.75	55.10	54.98	80.40	85.90
S9234	45.25	43.61	50.91	47.59	54.20	51.19	77.90	85.40
S13207	79.74	81.30	82.31	82.51	77.00	84.89	93.85	94.81
S15850	62.82	66.21	66.38	67.34	66.00	69.49	92.43	93.68
Average	**56.23**	**59.77**	**62.81**	**62.79**	**63.07**	**65.13**	**86.15**	**89.95**

Table 11. Experimental Results for Power Consumption of V-F and F-V Codes

Circuit	Total Power	Average Power(WTMA)	Peak Power(WTMP)
S5378 VF	32703	294.62	579
S5378 FV	27115	244.28	466
S9234 VF	69710	438.43	774
S9234 FV	67450	424.22	748
S13207 VF	44350	989.00	5235
S13207 FV	165830	702.67	2012
S15850 VF	239022	1117.22	5020
S15850 FV	132812	987.46	2764

Table 12. Comparison of average power of F-V codes with existing codes

ISCAS'89 Circuit	Average power of F-V codes	FDR		ALT-FDR	
		Average power	Average power reduction over FDR (%)	Average power	Average power reduction over ALT-FDR (%)
S5378	244.28	2146	88.60	1579	84.52
S9234	424.22	3683	88.48	877	51.62
S13207	702.67	8026	91.20	6815	89.68
S15850	987.46	13,362	92.60	9283	89.36
Average			90.22		78.79

Table 13. Comparison of scan-in average power of V-F codes with other codes

ISCAS'89 Circuit	Average power of V-F codes	FDR		ALT-FDR	
		Average power	Average power reduction over FDR(%)	Average power	Average power reduction over ALT-FDR(%)
S5378	294.62	2146	86.27	1579	81.34
S9234	438.43	3683	88.09	877	50.01
S13207	989.00	8026	87.68	6815	85.49
S15850	1117.22	13,362	89.64	9283	87.96
Average			87.92		76.20

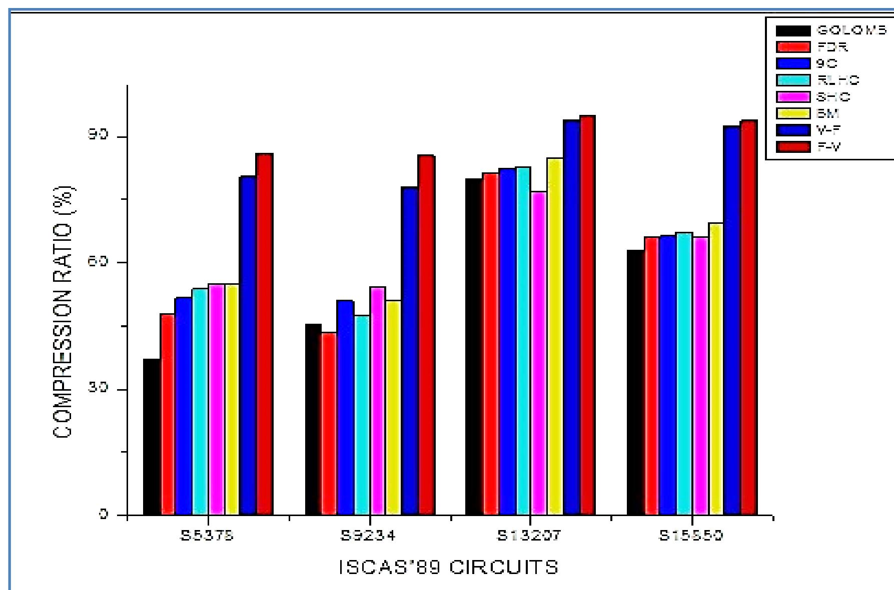

Fig. 2. Graph showing comparison between the Proposed Technique with other existing techniques using the ISCAS'89 circuits

5. CONCLUSION

Test data Compression is necessary due to the high cost of ATE memory, and the enormous amount of test volume. This work presents an efficient test data compression method, which simultaneously reduces the SoC test data volume, and test power consumption. Experimental results for the ISCAS'89 benchmark circuits shows that the proposed approach decreases test data volume to an average of 89.95%, using F-V codes and 86.15%, using V-F codes, over the original data. By reducing the number of transitions per second (switching activity is reduced), power consumption is reduced, using both these approaches. Selective compression of Unspecified test patterns form the basis of this technique, to effectively produce rapid reduction in test data volume and power consumption of test data.

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