Comparative Study of different Flip Flop Cells for WSN Applications

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ABSTRACT
Efficient power management in wireless sensor network is a critical issue as the sensor nodes are low powered devices. In a sensor node, flip flop consumes large amount of power as they make maximum number of internal transitions. Reduction in the power consumed by flip-flops shows a deep impact on the total power consumed. Hence, designing low power flip flop cells are highly important for enhancing the life time of network. This paper presents a comparative study of different flip flop cells for WSN applications based on simulation at 90nm and 45nm technology. The simulation results show that flip flop using multiplexers offers the best overall performance.

Keywords
D flip flops, microcontroller, wireless sensor network, network lifetime, power management.

1. INTRODUCTION TO WIRELESS SENSOR NETWORK
Wireless sensor network consists of large number of sensor nodes deployed in an area of interest and is gaining a considerable attention in today's world. It can be useful for large number of applications which includes habitat monitoring, structural health monitoring, transportation, precise agriculture and many more. Almost all these applications needs long lifetime of system. The system lifetime is measured as the time until all nodes have been drained out of their energy. So, the main aim is to enhance the life of the sensor network, so that it can last for the duration of the application. The lifetime of the sensor network depends on the lifetime of the constituent sensor nodes. Sensor nodes are battery powered and once deployed it is impossible to recharge or replace the batteries. So, in order to improve the lifetime of the network, the battery lifetime of the individual nodes has to be maximized.

Architecture of a wireless sensor node is shown in Fig 1 [1]. It is made of four basic components: sensing unit, processing unit, transceiver unit and power unit [2]. Sensing unit is used to trace the physical environment and tell the CPU to compute and store the data it sensed. Processing unit consists of microcontroller which reads sensor data and makes it ready for transfer. Transmission unit receive the information from CPU and transmit it to the outside world. Power unit regulate battery power to sensor node.

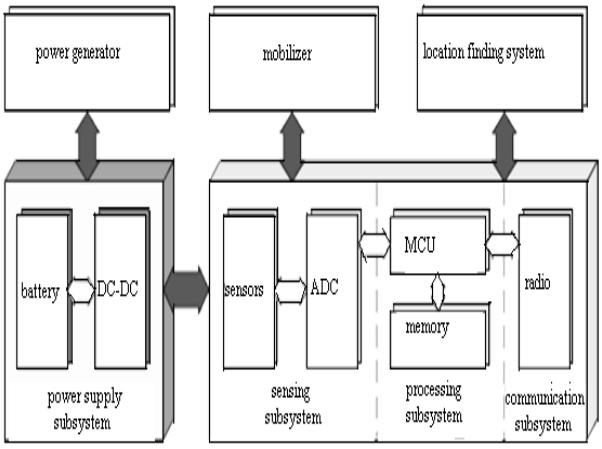


Fig 1: Architecture of wireless sensor node

Applications of wireless sensor network are discussed below:

- Security and Surveillance: Security and surveillance are important applications of wireless sensor networks. Sensors can be used to improve the safety of roads by providing warnings of approaching cars at intersections [3]. Image or video sensors can be very useful in identifying and tracking moving entities.

- Industrial Monitoring: Wireless sensors can be used to monitor manufacturing processes and conditions of industrial equipment to alert for imminent failures. This reduces cost of service and maintenance, improve customer satisfaction and even save lives.

- Health care monitoring: The medical applications are often of two types: wearable and implanted. In wearable health monitoring system devices are kept at close proximity of the user. It allows an individual to closely monitor changes in her or his vital signs and provide feedback to help maintain an optimal health status. In implantable medical applications devices are inserted inside human body.

- Sensing of wildfires: To detect drastic changes in temperature or heat, the sensor nodes can be randomly and densely placed across forest [4].

- Smart Home Monitoring: Wireless sensors embedded inside everyday object forming a wireless sensor network is used to observe the activities performed in a smart home.

- Drought prediction: Sensor nodes are deployed in an agricultural field or a plantation to detect the level of some chemical compounds. The information gathered will be useful in predicting droughts.

In a sensor node maximum power is consumed by microcontroller since most of functionalities are controlled or performed by it [5]. Flip flop occupies maximum areas of microcontroller. So, designing efficient flip flop cells are very important for WSN.

2. DESIGN OF FLIP FLOP CELLS

Flip-flop is an electronic circuit that is used to store a logical state of any data input signals with the response to a clock pulse. Flip-flops are widely used to receive and maintain data in selected sequences during recurring clock intervals for a limited time period sufficient for other circuits within a system. A huge portion of the on-chip power is consumed by clock systems, which consists of timing elements such as flip-flops, latches and clock distribution network. These clock systems have redundant transition and the transition probability of the clock is 100% while an ordinary logic has one-third on average. So, clock systems are one of the most power consuming components in a VLSI system. These components consume 30% to 60% of the total power dissipation in a system. Consequently, reduction in the power consumed by flip-flops show deep impact on the total power consumed. For this characterization of flip-flop cells performance, five widely used flip flop cells have been selected.

- Transmission-gate Master-Slave (TGMS) flip-flop: This flip-flop is realized by using two transmission gate based latches operating on complementary clocks [6]. This flip-flop may be sensitive to clock-skew of its two complementary clock-phases as shown in Fig 2.

- C^2MOS flip-flop: C^2MOS stands for clocked CMOS and is an inverter-based master-slave D flip-flop which uses clocked inverters to control the loading of a new value, and to break the feedback loop. It is based on using two clocked inverter-based D-latches. The schematic for the C^2MOS is shown in Fig 3.

- Power PC 603: This structure is a combination of TGMS flip-flop and C^2MOS flip-flop. The feedback transmission gate is changed with a clocked inverter as shown in Fig 4.

- Sense Amplifier based D flip-flop: The Sense-Amplifier based flip-flop (SAFF) consists of a sense-amplifier and a SR latch capturing the output of the sense-amplifier [7] as shown in Fig 5.

- Flip flop using multiplexers: The schematic for the flip-flop using multiplexers [8] is shown in Fig 6.

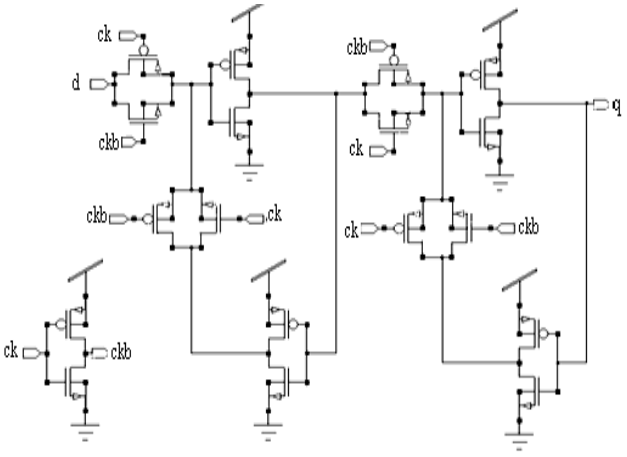


Fig 2 Transmission-gate Master-Slave flip-flop (TGMS)

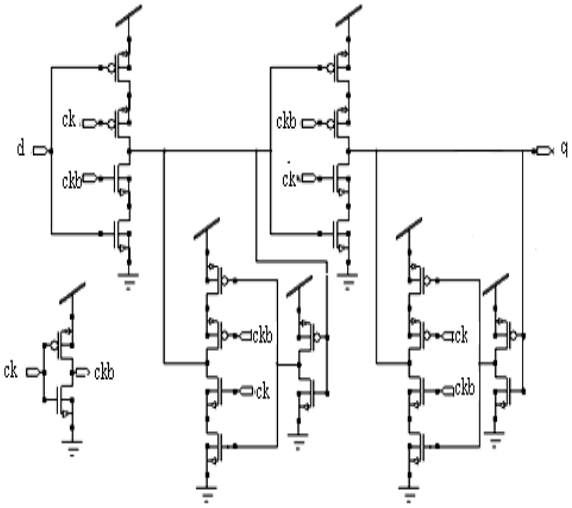


Fig 3: C^2MOS flip-flop

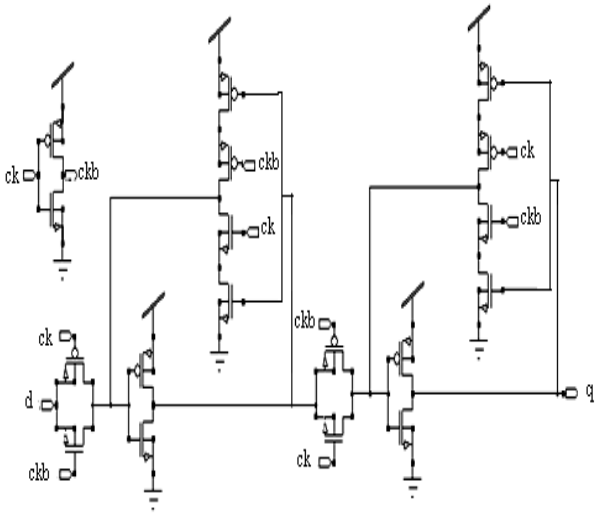


Fig 4: PowerPC 603

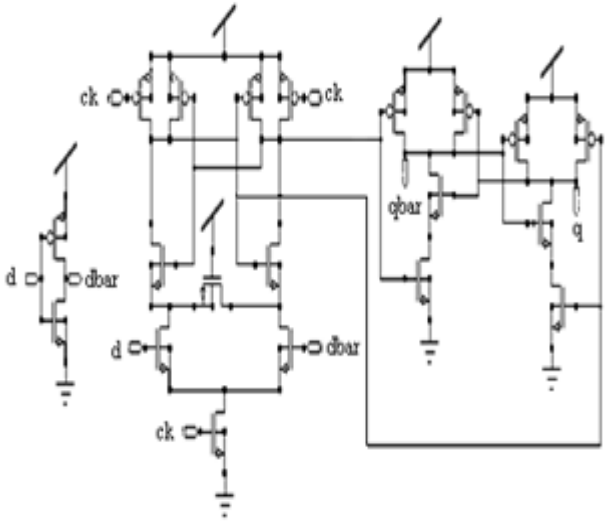


Fig 5: Sense Amplifier based D flip-flop (SAFF)

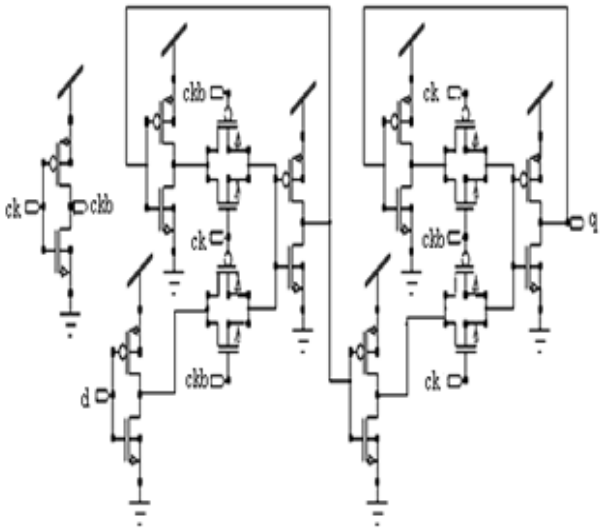
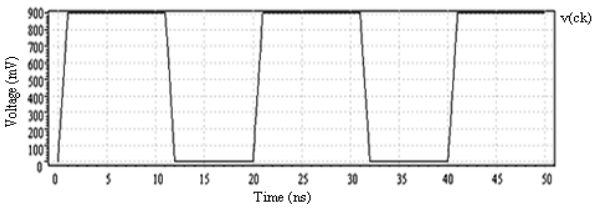
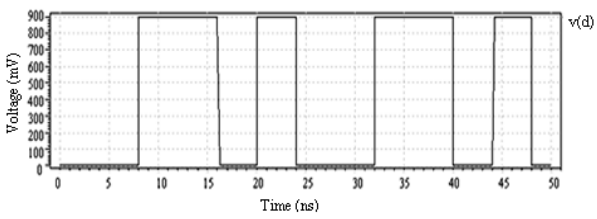


Fig 6: Flip-flop using multiplexers

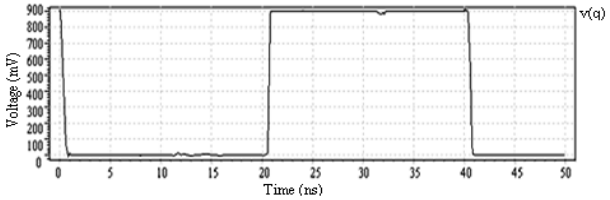
Now, the circuits are simulated and results are discussed in the next section.



(a)



(b)



(c)

Fig 7: Waveform of positive edge triggered D flip flop (a)clock signal b)data input (c)output

3. SIMULATION RESULTS

The simulation is carried out at 90nm and 45nm technology with a power supply voltage ranging from 0.5V to 1.2V at an operating frequency of 50MHz. The detailed results are discussed in following sections.

3.1 Simulation Results at 90nm

The characterization of the flip-flop cells have been achieved by simulation at 90nm technology. All flip-flops are simulated with a power supply voltage ranging from 0.5V to 1.2V at an operating frequency of 50MHz. For power dissipation analysis, a maximum power dissipation pattern (α) of 1 was considered and there was no external load. Fig 7 shows the simulation result for all five circuits. Table 1 presents the tabulated results for 90nm technology.

Table 1. Flip-Flop Metrics at 90nm Technology

Flip flop cell	Delay (ns)	Power (µW)	PDP (J)
TGMS	20.094	1.67	3.357×10^{-14}
C^2MOS	10.975	53.69	5.893×10^{-15}
PowerPC 603	20.039	1.72	3.452×10^{-14}
SAFF	0.20052	1.25	2.516×10^{-16}
Flip flop using multiplexers	9.9742	2.61	26.049×10^{-15}

The simulation result of TGMS and PowerPC 603 shows average delay and power dissipation of 20.094ns/1.67µW and 20.039ns/1.72µW respectively at 0.9V. These results are comparatively poorer.

The C^2MOS and flip-flop using multiplexers show medium performance on all figures regarding average delay and power dissipation, with C^2MOS slightly better than the flip flop using multiplexers. At 0.9V, the average delay and power dissipation of C^2MOS are 10.975ns and 53.69µW respectively. Whereas flip flops using multiplexers shows average delay and power dissipation of 9.9742ns and 2.61µW respectively at 0.9V.

The SAFF shows best performance on all figures regarding average delay and power dissipation. At 1.2V, average delay and power dissipation of SAFF are 0.20052ns and 1.25µW respectively.

3.2 Simulation Results at 45nm

The characterization of the flip-flop cells have been achieved by simulation on a 45nm technology. All flip-flops are simulated with a power supply voltage ranging from 0.5V to 1.2V at an operating frequency of 50MHz. Fig 7 shows the simulation result for all five circuits. Table 2 presents the simulation results for 45nm technology.

Table 2. Flip-Flop Metrics at 45nm Technology

Flip flop cells	Delay (ns)	Power (µW)	PDP (J)
TGMS	20.009	2.529	5.06×10^{-14}
C^2MOS	0.13841	62.544	8.656×10^{-17}
Power PC 603	20.009	2.529	5.06×10^{-14}
SAFF	0.096493	2.524	24.36×10^{-17}
Flip flop using multiplexers	0.0092282	3.359	31.002×10^{-18}

The simulation result of both TGMS and PowerPC 603 shows average delay of 20.009ns and a power dissipation of 2.529µW at 0.9V. These results are the worst overall results in this simulation.

The flip-flop using multiplexers show best performance regarding average delay and power dissipation. At 0.9V, the average delay and power dissipation of flip-flop using multiplexers are 0.0092282ns and 3.359µW respectively.

SAFF was unable to work successfully at 0.9V in 45nm. The simulation result of the SAFF shows average delay of 0.096ns and a power dissipation of 2.52µW at 1.2V. Increasing the power supply voltage to V_{DD} = 1.3V, the average delay decreases to 0.082ns while the power dissipation increases to 3.83 µW. So, SAFF provides medium power delay product than other flip flops but at the cost of high power supply. C^2MOS also shows medium performance but slightly better than SAFF. At 0.9V C^2MOS shows average delay of 0.13841ns and a power dissipation of 62.5µW.

4. CONCLUSION

Flip flops find wide applications in microcontrollers which again control most functionalities of WSN. In this paper, five different flip flop cells have been simulated at 90nm and 45nm technology. The simulation results show that at 90nm technology, SAFF shows best performance regarding average delay, power dissipation and power delay product, whereas at 45nm technology it is seen that, flip flop using multiplexers offers the best overall performance. The future study will include optimization of power and delay for the best design.

5. REFERENCES

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