A Variable Threshold Voltage CMOS Comparator for Flash Analog to Digital Converter

Gulrej Ahmed
Research Scholar
Electronics & Communication Engg. Department
Maulana Azad National Institute of Technology
Bhopal, India

Rajendra Kumar Baghel
Professor
Electronics & Communication Engg. Department
Maulana Azad National Institute of Technology
Bhopal, India

ABSTRACT
This paper presents a variable threshold voltage CMOS comparator for flash analog to digital converter. The proposed comparator has single-ended type of architecture. The comparator is designed and analyzed by Cadence Virtuoso Analog Design Environment using UMC 180nm technology. The proposed comparator consumes peak power of 34.97 µW from 1.8 V power supply. It achieves the power delay product (PDP) of 8 fJ and propagation delay of 230 ps. The designed comparator eliminates the requirement of resistive ladder network for reference voltage generation. This makes it highly suitable in the design of flash analog to digital converter.

General Terms
Comparator, analog to digital converter, propagation delay

Keywords
Variable threshold voltage, threshold inverter quantization, flash ADC, power delay product.

1. INTRODUCTION
In today's era, where the demand for portable battery operated devices is rising, the researchers are focusing towards low power methodologies for high speed applications. One of major application is analog to digital converters (ADC), where the low power dissipation and high speed is ultimate target. The main component, which limits the performance of ADC, is the comparator. There are many types of comparators available according to requirement and type of ADC. Typical comparators are of differential type of architecture. They can be further classified as pre-amplifier based comparator and dynamic comparator [1-3]. However these differential types of comparator are intrinsically complex in design and consume high power. However Power reduction may be achieved by number of ways in the CMOS circuits. One of the ways is to minimize the supply voltage overhead. But it may affect the circuit with large delay because as supply voltage reaches to the threshold voltage of the transistor, the delay of the circuit increases. On the other hand this can be overcome by proper scaling of the devices. The scaling not only improves the delay performance of the devices but also improves the low voltage operation characteristics. In this paper, the scaling of MOS transistors has been exploited for designing the comparator circuit, which fulfills both the requirements of high speed and low power consumption for flash ADC architecture.

2. COMPARATOR
Comparator constitutes the main component in analog to digital conversion (ADC). It is basically the first stage in ADC, which converts the signal from analog to digital domain. Among all types of ADCs, the flash ADC is the fastest ADC. The Flash ADC employs the 2^N-1 comparators for N-Bit resolution. However, these 2^N-1 comparators work simultaneously and therefore consume large amount of power. In addition to this, the flash ADC also requires resistor ladder circuit or capacitor array circuit for reference voltage generation, which is again power hungry and therefore Flash ADC consumes highest power. The most common structure of comparator is of differential type, which is extensively used in design of flash ADC. However a single ended type of comparator may be realized. An inverter may be deployed as an analog comparator instead of using a whole analog block of comparator [4]. The inverter requires lesser number of transistors as compared to traditional comparator. In fact, a traditional comparator requires two inputs, while inverter based comparator requires only one input. The threshold inverter quantization (TIQ) comparators have been used to design the flash ADC [5]. The variable logic threshold inverter can be scaled to generate a different reference voltages required for comparison. Hence there is no need of resistor array for the generation of reference voltages. Thereby, the static power consumption by resistor ladder is completely removed in Flash ADC.

2.1 Logical Threshold Voltage
An Inverter can be designed to switching voltages between V_{THN} and $V_{DD} - |V_{THP}|$, where V_{THN} and V_{THP} being the threshold voltages of the NMOS and PMOS transistors respectively. The switching voltage can be expressed as [6]

$$V_{sp} = \frac{(V_{DD} - |V_{THP}|) + V_{THN}\sqrt{\frac{\mu_n W_n}{\mu_p W_p}}}{1 + \sqrt{\frac{\mu_n W_n}{\mu_p W_p}}} \qquad (1)$$

Where, W_p= PMOS channel width, W_n= NMOS channel width, V_{DD} = supply voltage, μ_n = electron mobility, μ_p= hole mobility. It has been assumed that both transistors PMOS & NMOS have the same channel length. The switching voltage values of Inverters are determined by the relative sizing (W/L) of the transistors. The switching voltage may also be referred as logical threshold voltage of a CMOS inverter.

2.2 Physical Threshold Voltage
The threshold voltage of the device is given by the following mathematical expression [6]:

$$V_T = V_{TO} + \gamma\left(\sqrt{|(-2)\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \qquad (2)$$

Wherein, V_{TO} is threshold voltage under zero bias condition V_{SB} is source-to-substrate voltage, ϕ_F is Fermi potential, and

the parameter γ is called the body-effect coefficient & described by:

$$\gamma = (t_{ox}/\varepsilon_{ox})\sqrt{2q\varepsilon_{si}N_A} \quad (3)$$

Wherein, t_{ox} is the oxide thickness ε_{ox} is the permittivity of oxide layer; q is the carrier charge,ε_{si} is permittivity of Silicon and N_A is acceptor concentration.

Just by reducing the size of the device and scaling down the supply voltage, the threshold voltage of MOSFETs does not vary. It is clear from the Equation 2 & 3, that threshold voltage is not dependant on the aspects ration (W/L) rather it is a function of MOSFETs oxide thickness. On the other hand, the logical threshold voltage of the device can be change by varying the aspects ration of the device (W/L) from the equation 1.

3. VTV COMPARATOR

We have proposed the new modified structure. The architecture of Variable Threshold Voltage (VTV) comparator is similar to TIQ Comparator [5]. The comparator circuit consists of four cascaded stages as shown in figure 1.

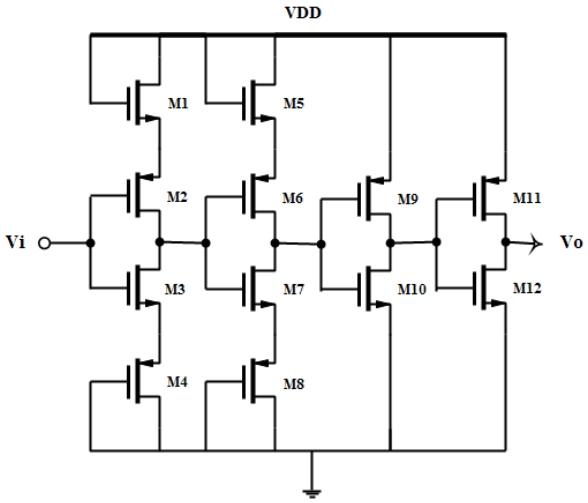

Fig 1: Proposed comparator schematics diagram

The first and second stages constitute VTV inverters and their logic threshold voltage is decided by equation 1, and third and fourth stages are two conventional inverters, their work is just to provide high gain and fast switching. Note that the devices M1, M4, M5 and M8 are always in saturation because the drain and gate are same potential i.e. V_G=V_D. For NMOS device source-drain current (I_D) is described by the following equations.

$$I_D = \frac{W}{L}\left(\frac{\mu_n C_{ox}}{2}\right)(V_{GS} - V_{THN})^2$$

$$I_D = \frac{W}{L}k_n\,(V_{GS} - V_{THN})^2$$

$$gm = \frac{\partial I_D}{\partial V_{gs}} = \sqrt{\frac{W}{L}k_n I_D}$$

Similarly for PMOS device,

$$I_D = \frac{W}{L}\left(\frac{\mu_p\, C_{ox}}{2}\right)(V_{SG} - V_{THP})^2$$

$$I_D = \frac{W}{L}k_p\,(V_{SG} - V_{THP})^2$$

$$gm = \frac{\partial I_D}{\partial V_{sg}} = \sqrt{\frac{W}{L}k_p I_D}$$

The resistance of saturated MOS device is given by inverse of its transconductance (*gm*). These resistances created by M1, M2, M3 and M4 are responsible for smaller short circuit currents in the first and second stages. This results in the lower power dissipation by the comparator. The first section of proposed comparator provides variable logical threshold voltages. For a 5-bit flash ADC, there is need of total 31 logical threshold voltages. This is accomplished by varying aspects ration of transistors M2 and M3. Using the proposed comparator, we have also simulated a low-power 5-bit flash ADC.

4. FLASH ADC

The block diagram of 5-bit Flash ADC is shown in the figure 2. An analog input voltage (Vin) goes through comparator bank. For 5-bit flash ADC, the comparator bank consists of total 31 comparators, each comparator has distinct logical threshold voltage. The comparators compare the input voltage with reference voltages, which are determined by the aspect ratio of CMOS transistors of comparator. The output of the comparator is either '1' or '0' depending on applied input voltage.

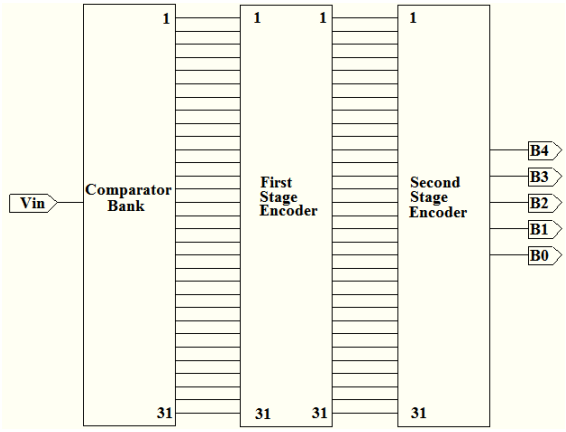

Fig 2: VTV comparator based 5-Bit Flash ADC

The comparator bank generates basically thermometer code. In order to convert these codes into binary, the encoder performs the encoding process in two steps. First the thermometer codes are converted into intermediate codes. These codes are generated by performing the logical Excusive-Or (XOR) operation of the two adjacent comparators output. Thereafter intermediate codes are converted into binary code by second stage encoder.

5. SIMULATION RESULTS

The proposed Comparator has been simulated at 180 nm CMOS process with 1.8V power supply voltage. The measurement of propagation delay T_{PLH} and T_{PHL} is shown in figure 3. The power consumed by the VTV and TIQ comparator is depicted in figure 4. Using the proposed comparator, the functional simulation of 5-bit flash ADC is also performed. The digital codes are obtained correctly for 5-bit ADC as shown in figure 5. The transient analysis of the ADC is made by giving a ramp input voltage signal ranging from 0.74 V to 1.6 V. The designed flash ADC can distinguish the minimum input voltage signal level of 27 mV.

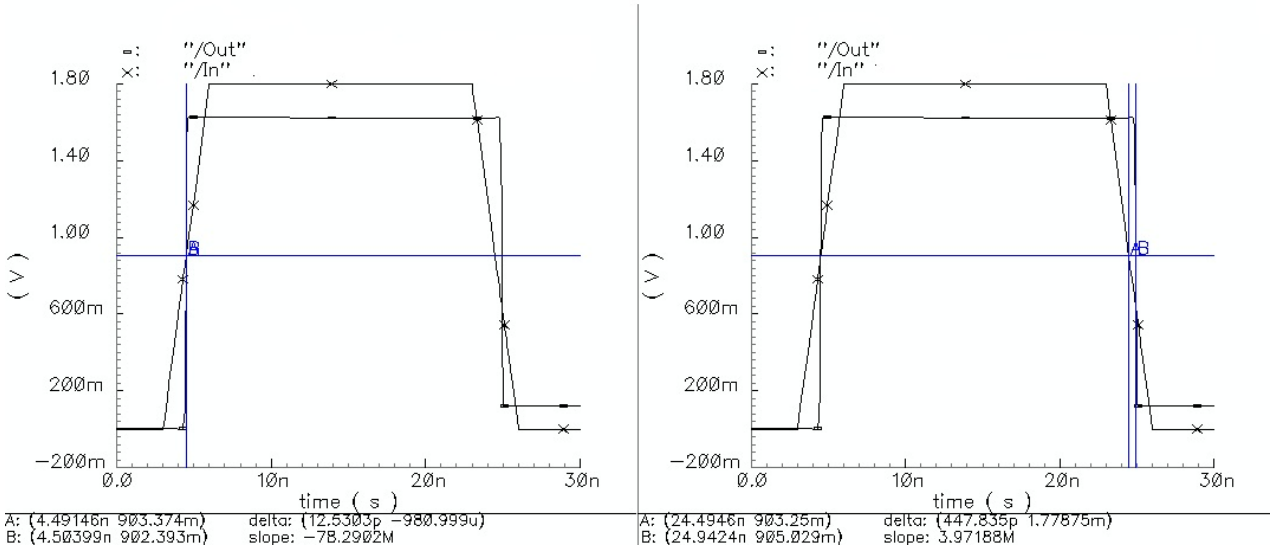

Fig 3: Measurement of Propagation Delay T_{PLH} and T_{PHL}.

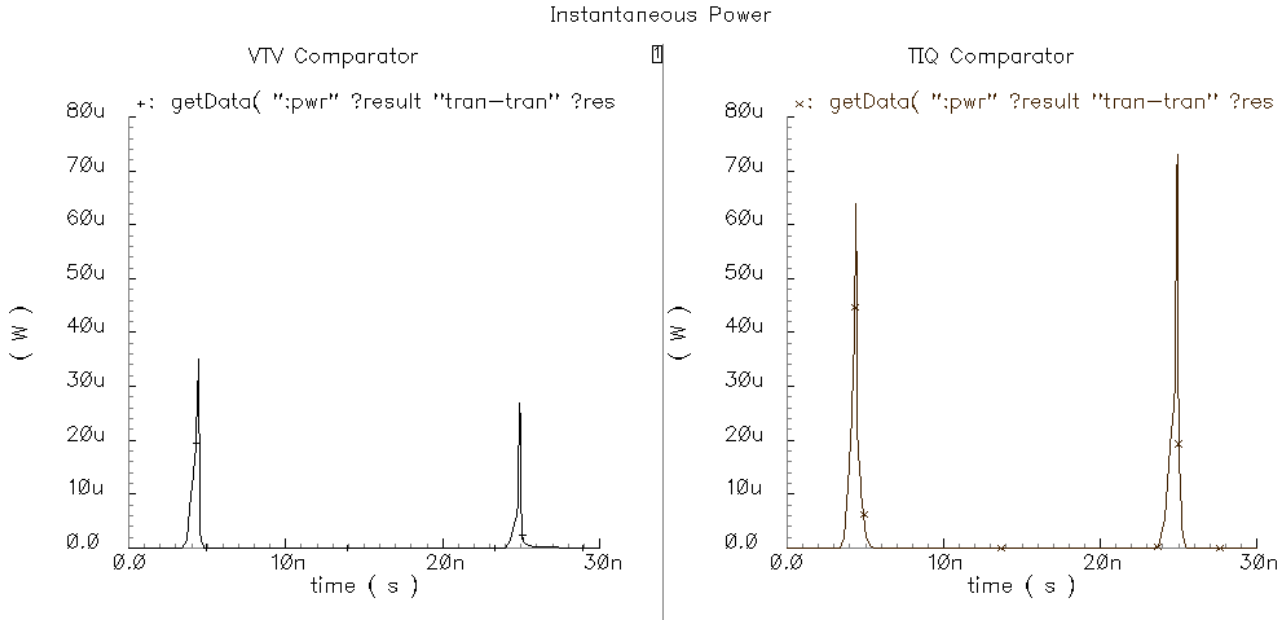

Fig 4: Power Measurement for Proposed & TIQ Comparator

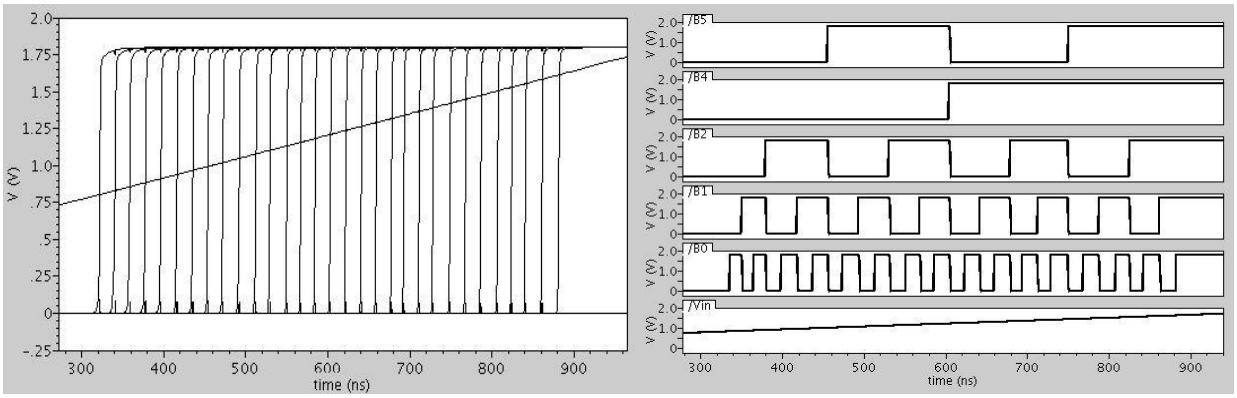

Fig 5: Variable Threshold Voltage Levels and Digital Codes for 5-Bit Flash ADC

6. DISCUSSION

The different parameters obtained for proposed comparator are compared with TIQ Comparator in table 1. It has been observed that the peak power for proposed VTV Comparator is 34.97μW & its average power is only 0.71 μW. While reported comparator [5] consumes peak power of 73.81 μW and its average power is 1.7 μW. There is an almost 47% reduction in the peak power.

Table 1: Results Summary

Parameter	TIQ Comparator	VTV Comparator
Peak Power	73.81μW	34.97 μW
Average Power	1.7 μW	0.71 μW
T_{PLH}	166 ps	17 ps
T_{PHL}	517 ps	447 ps
Delay	341.5 ps	230 ps
PDP	25 fJ	8 fJ

It is clear from the table 1 that the proposed comparator has improved result with the reported design. In table 2, the comparative analysis is also performed with other reported latch-type comparator and dynamic comparator.

Table 2: Comparative Results Analysis

Performance parameters	Proposed work	[1]	[3]
Technology	180nm	65nm	90nm
Supply Voltage	1.8 V	1.2 V	0.8 V
Delay	230 ps	104 ps	500 ps
Power	34.97 μW	2.88 mW	222 μW

7. CONCLUSION

The proposed new design of the comparator is based on variable threshold approach. The design has been carried out in UMC 180nm technology. The key parameters for the proposed comparator are delay and power dissipation. The proposed comparator dissipates peak power of 34.97 μW with maximum delay of 230 ps. The functional simulation shows its correctness in the logical operation with distinguished results in terms of power and speed. This makes it highly desirable for design of low power, high speed flash analog to digital converter.

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