A 1.5-V, 10-bit, 200-MS/s CMOS Pipeline Analog-to-Digital Converter

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ABSTRACT
Analog-to-digital converters (ADCs) are required in almost all communication and signal processing applications. This paper describes a 1.5-v, 10-bit, 200-Msample/s pipeline analog-to-digital converter in 0.18-µm CMOS technology. The entire circuit architecture is built with a modular approach consisting of identical units organized into an easily expandable pipeline chain. The converter uses ten stage pipelined architecture with fully differential analog circuits, with a full-scale sinusoidal input at 10 MHz's A special focus is made on pipelined ADC for its superior performance in terms of speed and resolution.

General Terms
Op-amp, Flip-flop, Adders,

Keywords
Analog-to-Digital converters (ADCs), Pipeline, High Speed

1. INTRODUCTION
The world around us is analog in nature i.e. all changes and physical phenomenon occurring are continuous. However due to the various advantages of having data in digital format like storage, processing, transmission etc., we prefer to convert these continuous varying quantities into discreet digital values [1]. This process in known as quantization and the device employed for quantization is known as an Analog to Digital Converter – ADC.

High-speed low-power Analog-to-Digital converters (ADCs) are the critical building blocks for modem communication and signal processing systems. They are the interface between the analog and digital signal processing. In recent years, pipelined switched - capacitor topologies have emerged as approach to implementing power-efficient Nyquist-rate ADC that have medium-to-high resolution at medium-to-high conversion rates [2], [3]. Recently, there has appeared a new class of ADC with an architecture known as pipeline, which offered an attractive combination of high speed, high resolution and low power dissipation. The pipeline ADC, therefore, became the optimum solution for present low power applications, such as a wireless Communication system [4], Such applications include wireless local area- network transceivers and digital set-top boxes.

MOS Transistors can be sized; that is, their W and L values can be selected, to fit a wide range of design requirement [5]. CMOS is currently the most widely used IC technology for analog and digital as well as combined analog and digital (or mixed –signal) applications [6].

2. DESIGN CONSTRAINTS
To further reduce the hardware cost at high resolution, pipeline architecture is employed. Figure1 shows typical pipeline A/D architecture. There is n number of identical stages, each quantizes k bits. So the overall resolution is M x K. Each stage samples the output from the previous stage and quantizes to k bits digital codes using flash ADC architecture. Stage 1 gives MSBs, stage n gives the LSBs. The later the stage is, the less significant the bits it outputs because of the gain factor in each stage.

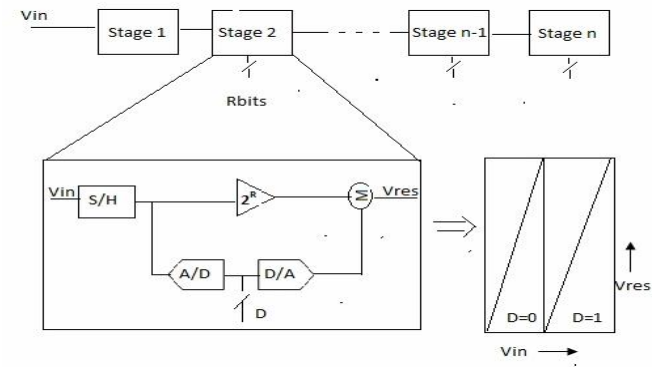

Fig.1 Pipeline Architecture

Pipeline architecture offers high degree of concurrence and approximately linear hardware cost with resolution [8]. The key advantage of pipeline architecture is that it allows digital error correction and digital gain calibration and power minimization through capacitor scaling [9]. Pipeline A/D is most popular in high speed (several MHz~50MHz) and high resolution (above 8-bit) application [10].

3. PROPOSED PIPELINE ADC
For the design of each stage pipeline ADC the required components are:

A. Operational Amplifier(Op-Amp):
Design of two stage opamp is shown in fig.2. Two stage Cmos opamp is designed to have many advantages like high open-loop voltage gain, rail to rail output swing, large common mode input range etc. The circuit comprises of an input differential stage with active load followed by a common source stage. The gain obtained from this design is 77.585dB.

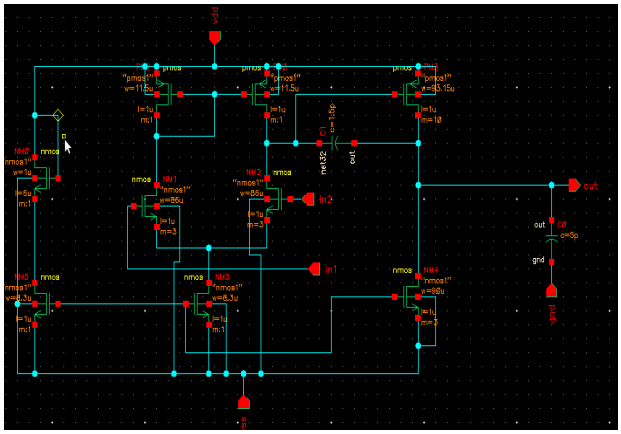

Fig.2 Two stage CMOS Op-Amp

B. **Sample and Hold Circuit:**
The design of sample and hold circuit is as shown in fig.3.

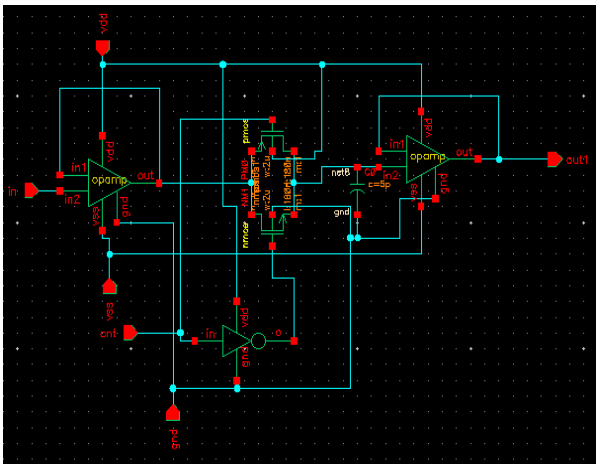

Fig.3 Sample and hold circuit

A storage element and a switch are the basic elements of sample and hold circuit. In this design as shown in fig.3, two buffers are used to avoid the loading on the source when sampling takes place and it is used to avoid the charge and discharge through the capacitor in the hold mode.

The sampling clock is given to the control of transmission gate. When the sampling clock is high the input is sampled through the first buffer and the capacitor to the input level. The path from the input is open circuited and the sampled voltage is maintained constant as soon as the clock goes low and then it is given to the preceding block for conversion.

C. **Comparator**
Two cascaded CMOS inverters are used as comparator for high speed conversion and for higher resolution. The design is as shown in fig. 4.

The proposed comparator saves the need of reference generator and operation mainly depends on the value of threshold voltage of NMOS (V_{tn}) AND PMOS (V_{tp}) device used. Vth can be obtained as

$$Vth = \frac{Vdd + Vtp + Vtn(Kn/Kp)^{\frac{1}{2}}}{1 + (Kn/Kp)^{\frac{1}{2}}}$$

$$Kn = Kp' \frac{Wn}{Ln}$$

$$Kp = Kn' \frac{Wp}{Lp}$$

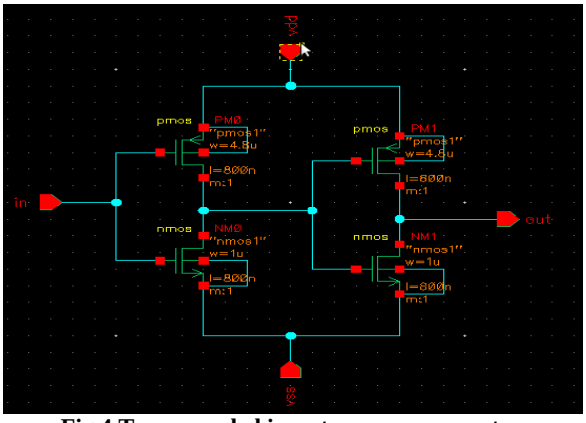

Fig.4 Two cascaded inverter as a comparator

D. D- Flip-flop
D- Flip-flops is used as a storage and delay element which will synchronize the bits of all stages, i.e. it will synchronize the output of pipeline ADC. For example 10 bit pipeline ADC has 10-bit shift register and decrementing to1 in the last stage.

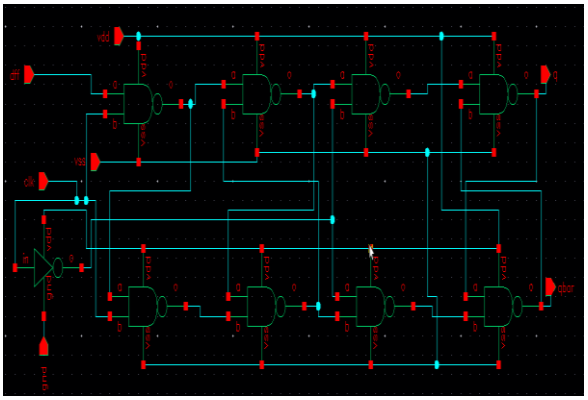

Fig. 5 D- Flip-flop

E. Analog Adder
The design of analog adder is as shown in fig.6. This configuration of analog adder has the advantage that it will not suffer the effect of loading even though both the input voltages are applied to the same terminal as shown in the circuit.

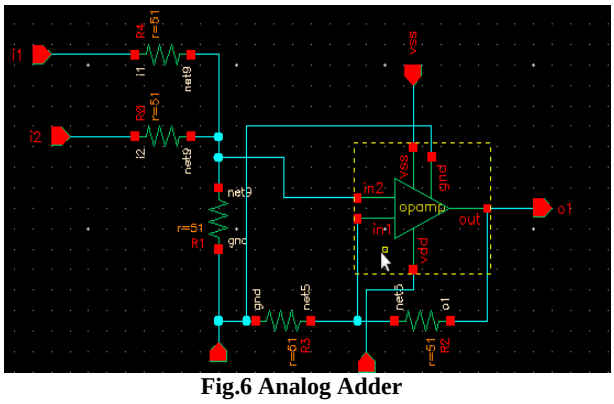

Fig.6 Analog Adder

F. One Bit DAC
The purpose of DAC is to provide an analog voltage corresponding to digital bits. The circuit shown below in fig.7

uses the multiplexer logic. The operation can be explained as, if 'CB' is zero then the upper part is on that means 'vref1' is passed else vref2.

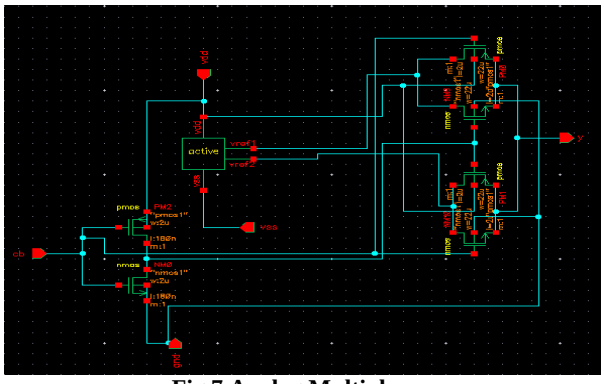

Fig.7 Analog Multiplexer

The reference voltages are generated with the help of a simple active divider network as shown in fig.8 with two supplies at either end of the ladder network.

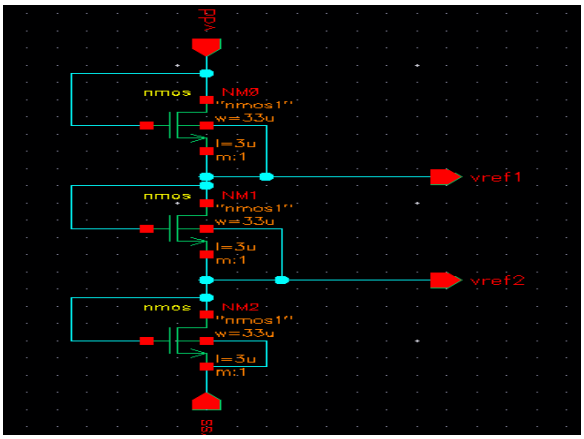

Fig. 8 Resistor Network

G. Inverting Amplifier

Each pipeline ADC stage have a gain block, whose gain depends on the number of output bits of each stage i.e Av=2n. Where Av is the gain of the amplifier and n is the number of bits of each stage. The inverting gain amplifier configured for gain of 2 is shown below in fig. 9.

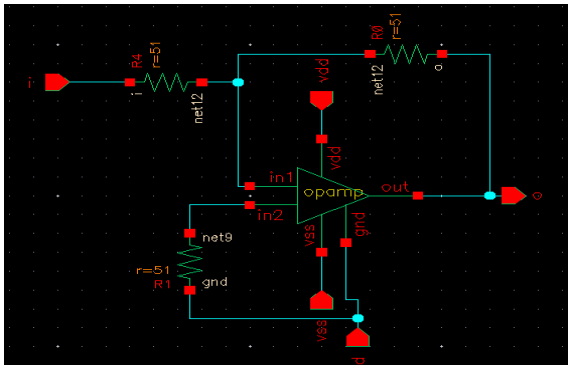

Fig. 9 Inverting Amplifier

H. One –bit single stage ADC

The proposed design architecture for one –bit single stage ADC is as shown in fig. 10 and consists of one sample and hold block, one comparator, inverting amplifier for gain of 2, one D flip-flop, one analog adder block.

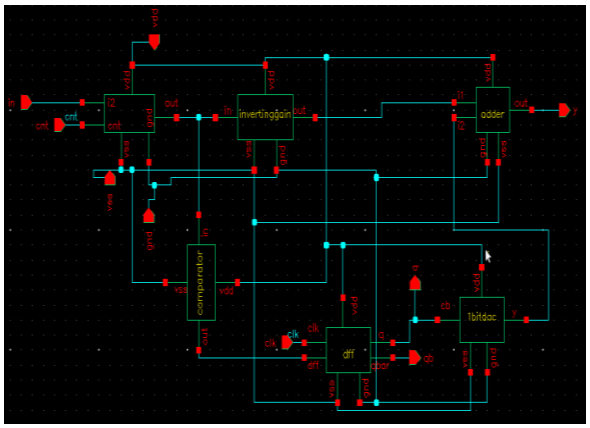

Fig.10 One –bit single stage ADC

I. 10 –bit Pipeline ADC

One –bit single stage ADC are cascaded to form 10 –bit Pipeline ADC as shown below in fig.11.

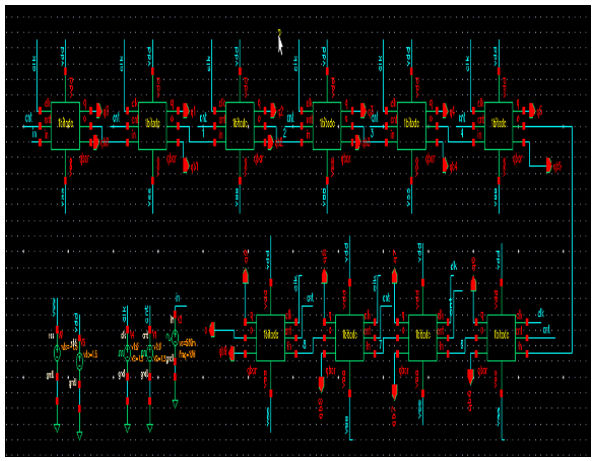

Fig.11 10 –bit Pipeline ADC

4. SIMULATION RESULTS:

The simulation results are as shown.

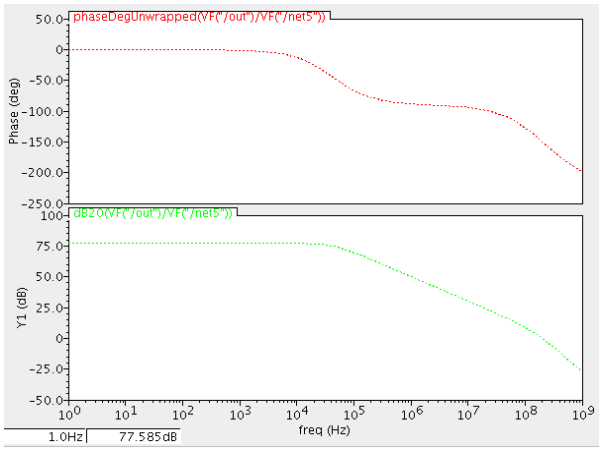

Fig.12 Gain and Phase Plot of Op-Amp

Gain = 77.585dB
Output swing = +1.4v to -1.4v
Gain Bandwidth = 200MHz

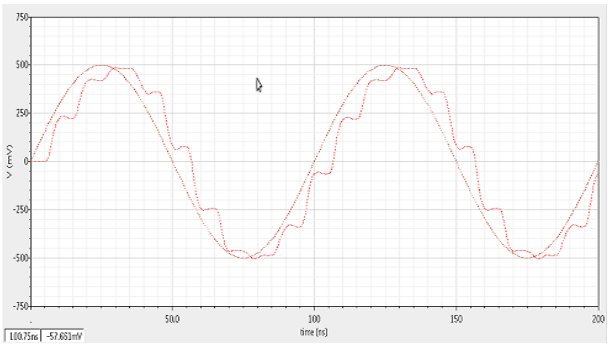

Fig.13 Plot of Sample And Hold

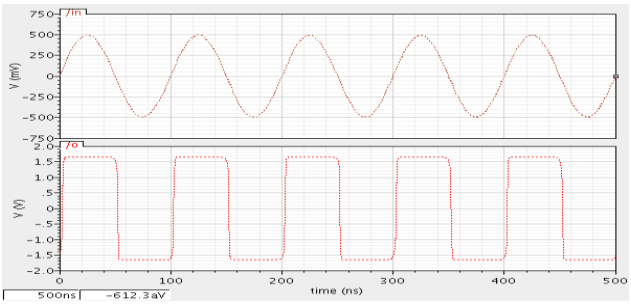

Fig.14 output Results of Comparator

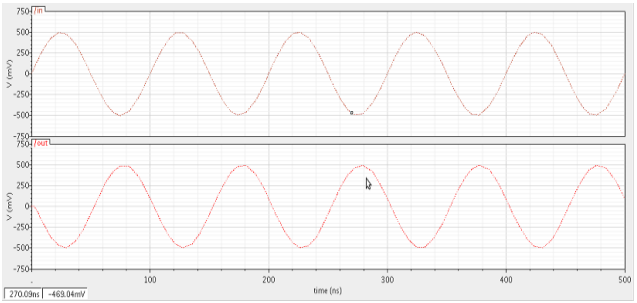

Fig.15 output plot of Inverting Gain Amplifier

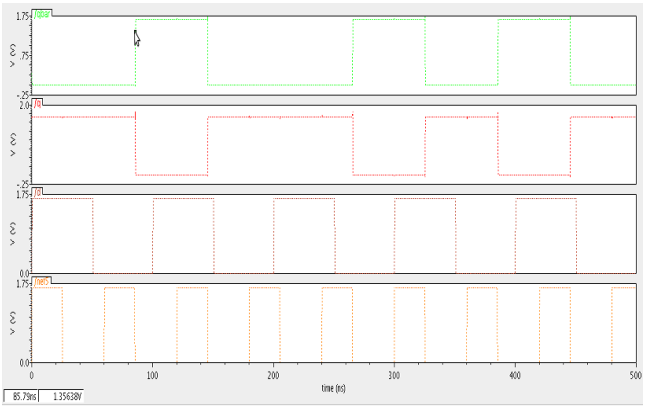

Fig.16 output Results of D Flip-flop

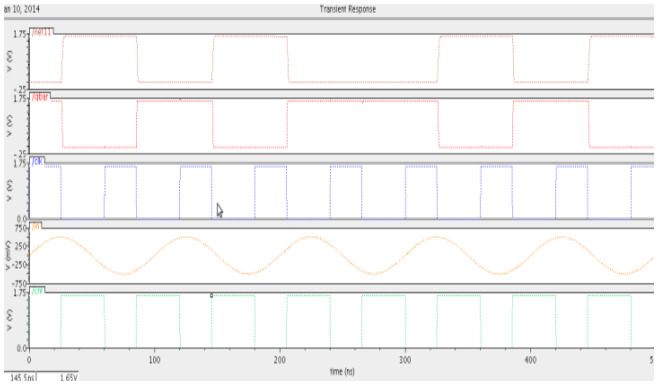

Fig.17 output of 1 bit pipeline ADC

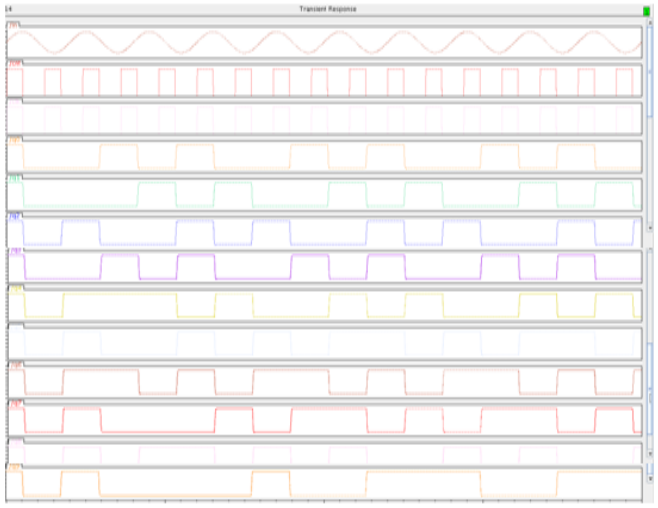

Fig.18 output of 10 bit pipeline ADC

5. CONCLUSION

The design of 1.5v, 10-bit pipeline ADC is implemented in Cadence Virtuoso Schematic editor using CMOS 180nm technology. The overall design is tested with various input signals and the results obtained are satisfactory. The designed 10-bit pipelined ADC is working for 10 MHz input frequencies and the maximum sampling rate archived from the design is 200Ms/s. The gain of the op-amp is 78.585dB with an output swing of +1.4V to -1.4V.

6. REFERENCES

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