Timing Optimization and Noise Tolerance Dynamic CMOS Logic Design

Priya Verma Sakshi Singh Jaikaran Singh

ABSTRACT
Dynamic CMOS logic circuits are used in high performance VLSI chips in order to achieve very high system performance. These circuits requireless number of transistors as compare to CMOS logic circuits. But they suffer from limitations such as noise tolerance, charge leakage, and power consumption. This noise induce in circuits will affect the performance of dynamic circuits. The our work base on noise of MOSFET in contrast to the conventional method which measures drain current noise of MOSFET and divides it by MOSFET transconductance. Therefore, the need for accurate measurement of I–V characteristics of the MOSFET is eliminated, leading to the better accuracy of the measured noise. To design a noise tolerable circuit using dynamic CMOS logic, a new noise tolerant technique is proposed here and then with the help of software we perform parametric analysis to improve the parameters such as noise margin, worst case delay, delayuncertainty, delay sensitivity from their initial performances. By studying those effects we try to put such parameters which help us to make a noise tolerable circuit.

Index terms
Dynamic Logic Structure, Charge sharing, Keeper logic

1. INTRODUCTION
In the Static CMOS logic style each logic stage contains pull up and pull down networks which are controlled by input signals. The pull up network contains p channel transistors, whereas the pull down network is made of n channel transistors. The networks are so designed that the pull up and pull down networks are never 'on' simultaneously. This ensures that there is no static power consumption.

Dynamic Vs. Static Logic
• Static Logicalways has a path from power or ground to the output
– Stable over long periods
– Simple clocking schemes
• Dynamic Logicrelies on capacitance of gates or other structures to hold state
– Can be faster than static logic
– Has minimum operating frequency
– More restrictions about how/when inputs can change

Noise sources in dynamic logic circuits can be due to gate internal noises which includes charge sharing noise, leakage noise, and so on, and due to external noises, which includes input noise, power and ground noise, and substrate noise. Charge sharing noise is caused by charge redistribution between the dynamic node and the internal nodes of the pull-down network. Charge sharing reduces the voltage level at the dynamic node causing potential false switching of a dynamic logic gate. Leakage noise refers to the possible charge loss in the evaluation phase due to sub-threshold leakage current. They are primarily caused by the coupling effect, also known as crosstalk, among adjacent signal wires. Power and ground noise is mainly caused due to the parasitic resistance and inductance at the power and ground networks and at the chip package. Substrate noise can affect the signal integrity of a logic gate through substrate coupling.

2. DYNAMIC LOGIC STRUCTURE
Dynamic CMOS logic circuits are used in high performance VLSI chips in order to achieve very high system performance. These circuits require less number of transistors as compare to CMOS logic circuits.But they suffer from limitations such as noise tolerance, charge leakage, and power consumption.Dynamic circuits also reduce input capacitance by implementing the pull-up circuits using a single PMOS transistor instead of a complete PMOS transistors network. Domino logic circuits consist of the pull-down network, a clocked pull-up pMOS transistor and clock NMOS pull down transistor. These two transistor can operates in precharge and evaluate phase. During precharge phase (when clk = 0) the output node of the dynamic CMOS stage is precharged to a high level, and the output of the CMOS inverter becomes low. During evaluation phase (when clk = 1) there are two possibilities: The output node either discharged to a low level through nMOS circuitry, or it remains high.

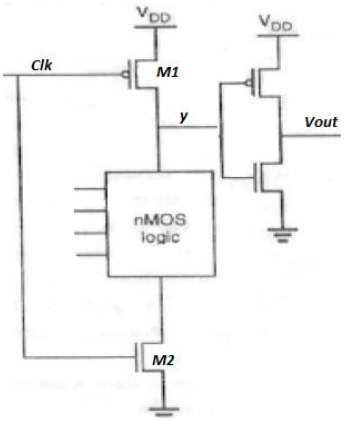

Fig.1: Dynamic CMOS logic structure

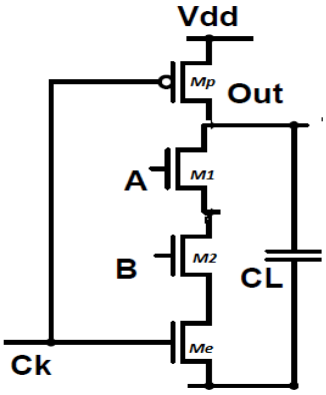

Fig.2: Dynamic CMOS NAND gate logic structure

A typical n-type dynamic NAND CMOS logic gate, as shown in Fig. 2, consists of clock controlled transistors Mp and Me, a pull-down n-type transistor network, and an output driver. The operation of a dynamic CMOS logic gate can be divided into two phases. In the precharge phase when the clock CLK is low, the dynamic node 'out' is charged to logic high through Mp and the output of the gate Q is high. The evaluation phase starts when the clock goes high. In this phase, Mp is OFF and Me is ON. The dynamic node S discharges or retains its charge depending on the inputs A and B to the pull-down network.

3. CHARGE SHARING

Charge sharing problems occur when two capacitive nodes charged to different voltages are connected through a pass transistor. When pass transistor is turned on, it connects the two nodes, resulting in a redistribution of the charge on both nodes. Charge sharing is a serious problem in precharge circuits and must be carefully guarded against. One solution is to make any charge holding capacitor much larger than any capacitors it shares charge with. Charge sharing between the dynamic stage output node and the intermediate nodes of the nMOS logic block during evaluation phase may cause erroneous outputs. Charge sharing between the output capacitance C1 and an intermediate node capacitance C2 during the evaluation cycle may reduce the output voltage level. During precharge phase, the output node capacitance C1 is charged up to its logic high level of VDD through pMOS transistor. In next phase, the clock signal goes high and the evaluation begins. If the input signal of the uppermost nMOS transistor switches from low to high during this evaluation phase. The charge initially stored in the output capacitance C1 will now be shared by C2, leading to the charge sharing phenomenon. The output node voltage becomes VDD/2, if C1 = C2 in the evaluation phase. Thus it is important to have C2 much smaller than C1.

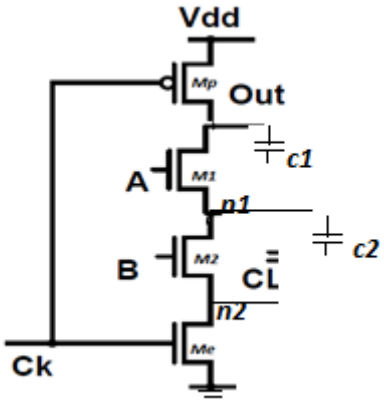

Fig.3: Chargesharing noise in dynamic CMOS

The charge sharing noise can be eliminated by using keeper logics.To enhance the noise tolerance of dynamic CMOS logic gates is to employ weak transistor, known as keeper, at the dynamic node as shown in Fig.3. The keeper transistor supplies a small amount of current from the power-supply network to the dynamic node of a gate so that the charge stored in the dynamic node is maintained. In the original domino dynamic logic work, the gate of the PMOS keeper is tied to the ground. Therefore, the keeper is always on. Later, feedback keepers, became more widely used because they eliminate the potential DC power consumption problem using the always-on keeper in the evaluation phase of domino gates.

Keeper logic with a small W/L ratio is added for the dynamic CMOS stage output, compensates for charge loss due to charge sharing and leakage at low frequency clock operation. Since keeper device is always on, the static power dissipation increases. Other way to realize this is to have a weak pMOS pull-up device in a feedback loop can be used to prevent the loss of output voltage level due to charge sharing. The keeper device conducts only when the output of static gate goes low. i.e. when precharge node voltage is kept high.

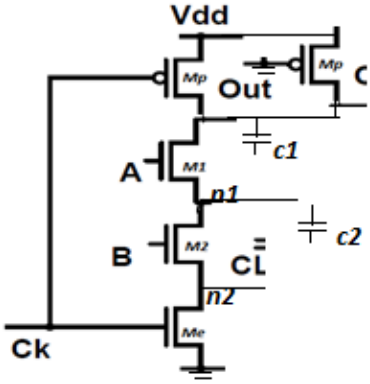

Fig.4: Charge sharing noise susceptible keeper logic in dynamic CMOS

4. DYNAMIC CMOS DESIGNS

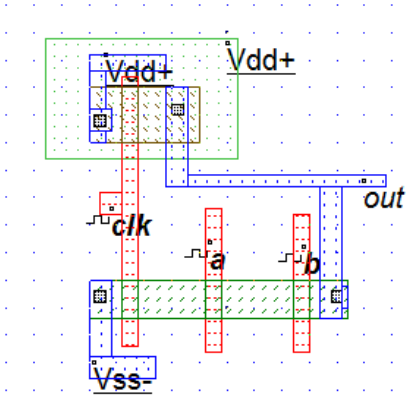

Fig.5: Dynamic CMOS NAND logic gate

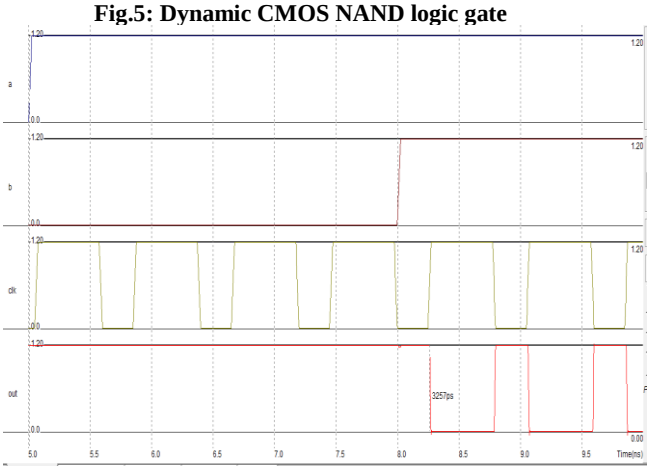

Fig.6: Timing simulation of dynamic CMOS NAND logic gate

A dynamic CMOS NAND logic, as shown in Fig. , consists of clock controlled transistors Mp and Me, a pull-down n-type transistor network, and an output driver. In the precharge phase when the clock CLK is low, the dynamic node 'out' is charged to logic high through Mp and the output of the gate Q is high. The evaluation phase starts when the clock goes high. In this phase, Mp is OFF and Me is ON. The dynamic node S discharges or retains its charge depending on the inputs A and B to the pull-down network.

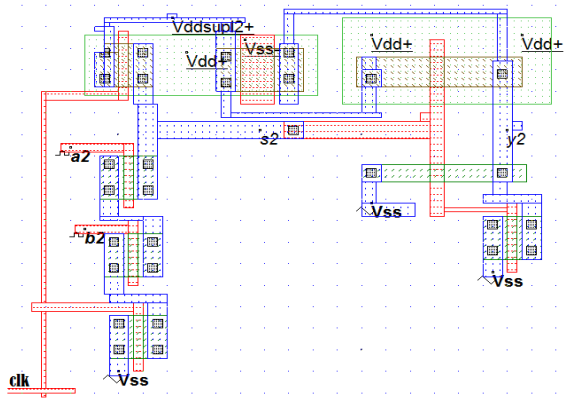

Fig.7:Charge sharing noise susceptible keeper NAND logic

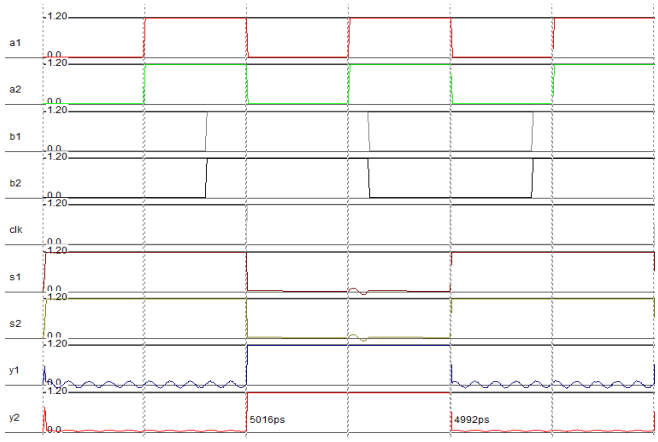

Fig.8:Timing simulation for noise susceptible keeper NAND logic

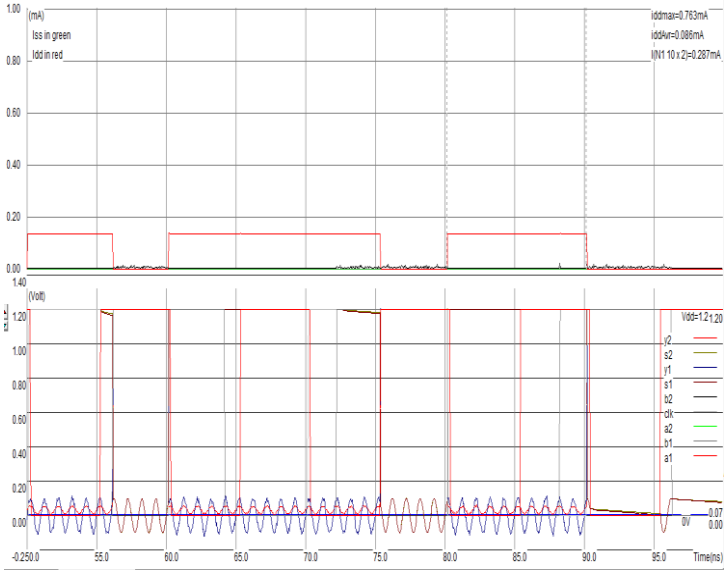

Fig.9: Current Voltage simulation for noise susceptible keeper NAND logic

The keeper transistor supplies a small amount of current from the power-supply network to the dynamic node of a gate so that the charge stored in the dynamic node is maintained. In the original domino dynamic logic work, the gate of the PMOS keeper is tied to the ground, Therefore, the keeper is always on. Later, feedback keepers, illustrated in above Fig. , became more widely used because they eliminate the potential DC power consumption problem using the always-on keeper in the evaluation phase of domino gates. The dynamic power dissipation with noisy signal calculated is 97uW with the average current though design is 0.763mA.The noisy signal of 49MHz frequency of amplitude 0.164V can be reduce to 67MHz frequency of amplitude of 0.07V.

5. CONCLUSION

To design a noise tolerable circuit using dynamic CMOS logic, a new noise tolerant technique is proposed here and then with the help of software we perform parametric analysis to improve the parameters such as noise margin, worst case delay, delayuncertainty, delay sensitivity from their initial performances. By studying those effects we try to put such parameters which help us to make a noise tolerable circuit. The dynamic power dissipation with noisy signal calculated is 97uW with the average current though design is 0.763mA. The noisy signal of 49MHz frequency of amplitude 0.164V can be reduce to 67MHz frequency of amplitude of 0.07V.

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7. REFERENCES

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8. AUTHOR'S PROFILE

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