Design 2.4 GHz 130nm CMOS Low Noise Amplifier Design for Wireless Network

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ABSTRACT
A low noise amplifier is one of the most commonly used components in analog and digital circuit designs. Low voltage, low power and low noise amplifier design has become an increasingly interesting subject as many applications switch to portable battery powered operations. An amplifier is linear electronic circuits that may used amplify an input signal and provide an output signal that is a magnified replica of the input signal. The need for design techniques to allow amplifiers to maintain an acceptable level of performance when the supply voltages are decreased is immense for maintain high gain and as low as possible noise. Popular LNA topologies are the inductive source degeneration common-source low noise amplifier. The common source low noise amplifier is commonly used for narrow-band applications due to its ease of input matching, high gain and low noise. Using this method, overall gain can be increased and the noise figure of the low noise amplifier can be decreased.. This work we presents a design of a low noise CMOS amplifier realized in a standard 130 nm CMOS technology with 1.3V supply voltage and consumes power less than 200uW with <1.5mA current. A two stage cascode LNA has to achieved noise figure is less than 2.5dB and achieves a gain >18dB on given frequency range also have good input and output matching.

Keywords
Two stage, low noise amplifier cascode, CMOS, gain , noise and power.

1. INTRODUCTION
A low noise amplifier is the first block of receiver also it is key building block in analog circuit design. Now a days CMOS become a very fast growing technology for a radio transreceiver implementation of various wireless communication system due to technology scaling. In RF front end is easy to integration with digital blocks by using CMOS whole system on single chip. LNA design very much used for telemetry wireless systems. It has large number of various sensors and attenuators. Typically first block of a receiver is LNA. There are several topologies for narrow band single ended LNA design, an appropriate Topology should be selected for low power and low voltage optimized LNA design. For Common gate topology, the gain is less than 10.0 dB with very low power consumption. For shunt series feedback common source topology, it is difficult to trade off among gain, small noise figure and better input/output matching with very low power consumption. Resistor termination common source topology adds noise to the LNA because of the resistor thermal noise. Inductive degeneration common source topology satisfies the specification in very low power consumption, but the isolation is not good enough compared to the cascade inductor source degeneration topology, which can get the similar low noise amplifier performance with very low power consumption. Above all, the cascode inductor source degeneration topology provides higher gain with a low noise figure. For all designs, the circuit's input matching, noise factor and gain have been derived to verify the design methodology. The whole performance of any receiver directly depend upon LNA gain and noise figure. It used such a design has low noise with a high linearity IIP3 and stable 50Ω impedance to terminates. The transmission line length is provide signal from antenna to amplifier. Input matching increases the overall performance of LNA and each stage of blocks. The LNA is designed as ISM band 2.4GHz frequency using 130nm CMOS technology.

2. LNA DESIGN OBJECTIVES
One of the most important features in low noise amplifier designs is ensuring that the amplifier maintains constant gain as well as noise at given narrowband frequency. 2.4 GHz CMOS 130nm Low Noise Amplifier is optimize for low noise at low current with very low power consumption .Here, we use inductive source degeneration common source topology, it helps to give very low noise figure and high gain. The inter-stage matching between two stages are off-chip, which reduce chip size. Another objective of this design is that, it is widely applicable for Bluetooth, WI-FI, ISM band, Mobile phones and handset. The low noise amplifier is the most important block at the receiver side which amplifies the week signal, for Bluetooth there is transmitting and receiving section for communication and transfer of data.

3. TECHNIUES FOR LOW NOISE AMPLIFIER DESIGN
There have been a number of works that have explored how to achieve high gain with minimum noise figure. Inductive source degeneration common source topology used to maintain the minimum noise so we used this topology. There are several topology to design the LNA some for the high gain and some for minimum noise but mostly depends upon the current and voltage parameter. To achieved high gain as well as low noise by using inductive source degeneration topology with two stage to improve gain but it also have its some disadvantages.

3.1 Design Differential Amplifier for Low Power and Low Noise
In this LNA[1 In this paper, a low power low noise amplifier for wireless sensor networks applications was presented. To reduce the LNA's power consumption and chip area, a two-stage cascade common-gate topology and an internal new designed inductor were used to achieve the input and the output matching. The LNA contained gain control circuit and frequency control

circuit to adapt the deviations of process and the environments.

It is provides a low power low noise differential amplifier designed for Wireless Sensor Network (WSN) in TSMC 0.18

µm RF CMOS process. It should work well centered at 2.44 GHz frequency and the forward gain is variable with highest gain at 12 dB to lowest gain at -2 dB by 2dB steps. It also has a two-stage cascade common-gate (CG)topology and two external inductor choke coils are used to achieve input matching of LNA under low power consumption, and a differential inductor has been designed as the load to achieve reasonable gain and reduce chip area simultaneously. The NF (Noise Figure) at high gain (12.5 dB) is 3.9 dB, the input referenced 1dB compression point (IP1dB) is about -1 dBm at lowest gain mode. The LNA consumes about 1.5 mA current from 1.8 V power supply.

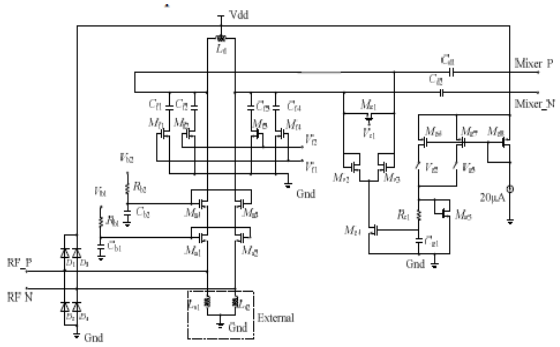

Fig.1 (a)

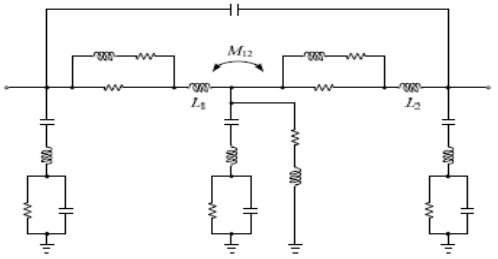

Fig.1 (b)

Figure 1 (a) Schematic of the LNA and (b) Double-π circuit model for inductor

3.2 Low Noise Amplifier Based on Inductor less Shunt-Shunt Topology

This CMOS LNA[2] A common-source topology with resistive feedback in a shunt-shunt configuration as represented in Fig. 2 compromise. For frequencies at which sCgs is negligible in comparison with gm, the input impedance is almost real and equal to 1/gm and if gm is high enough it is possible to have the voltage gain and the input impedance dimensioned almost independently. The proposed circuit is low cost and power efficient. To be low cost the circuit is inductor less and implemented in a standard nanoscale digital CMOS technology, with a state-of-the-art figure for area. To be power efficient all the circuits were chosen based on their power efficiency.

The result shows that a NF (Noise Figure) at high gain (16.5 dB) is 2.66 dB, the input referenced 1dB compression point (IP1dB) is about -21.8 dBm. This LNA consumes about 2.68 mA current from 1.2 V power supply.

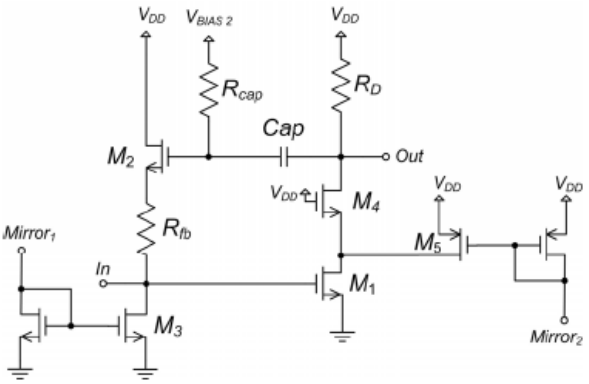

Figure 2 Resistive feedback LNA

3.3 Low Noise Amplifier with utilizing π-match and capacitive feedback input network

This LNA [3] employs an improved gain by using capacitive feedback. An ultra low-power CMOS low noise amplifier (LNA) with a new input matching topology will be proposed and analyzed. The LNA design is based on the capacitive feedback in conjunction with a π-match network. The proposed LNA saves on chip area by using only one inductor for the input matching. The π-match network introduces an additional degree of design freedom and allows the LNA to achieve higher gain. The LNA is designed for 2.4 GHz ISM band in a 130 nm RF-CMOS process. It achieves a gain of 25.2 dB with an Sll of -14 dB while consuming only 0.6 mW. The noise figure (NF) is 3.8 dB. The design makes use of the capacitive feedback and the π-match network to realize the input matching. The design method was explained and the LNA was designed. Number of inductors used was reduced and higher gain was achieved when compared to the L-CSLNA. The proposed LNA consumes only 0.6 mW while providing very high gain, good input matching and moderate NF and linearity. This LNA consumes about 0.6 mA current from 1V power supply

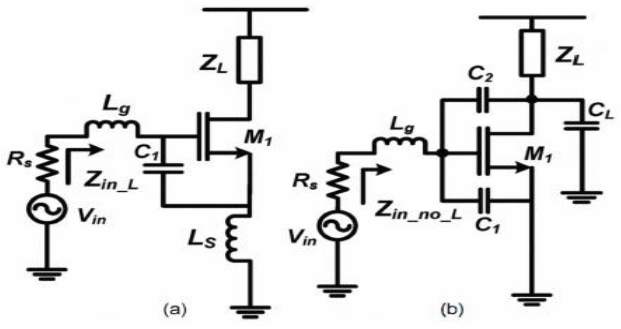

Figure 3 (a) Inductive source-degeneration CSLNA (b) Capacitive feedback LNA

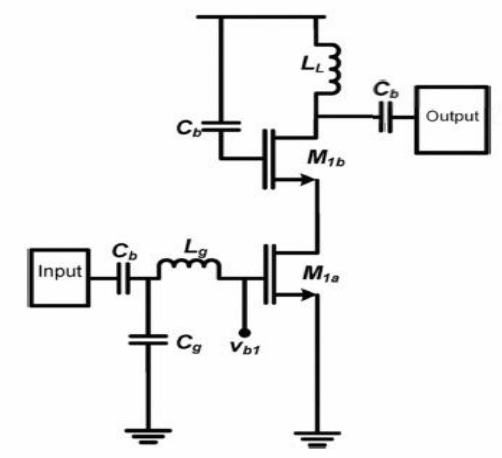

Figure 3 (c) Schematic of LNA

3.4 Proposed LNA with cascade inductive source degeneration topology

For the designing of a low noise amplifier (LNA) it seems appropriate to establish what the target specifications are. This is done in terms of a number of various parameters like S-parameter calculation in which we calculate the Gain (S21), Input return loss (S11), Output return loss (S22), and Isolation. S-parameter is mostly used for high frequency circuit design. The cascaded architecture provides a good input output impedance matching. By using cascaded transistor its minimize the Miller's capacitance. For gain boosting the inter stage inductor is used between two transistors. By using this the parasitic capacitance form impedance match network between input stage and cascoded stage which boost gain and lower the noise figure. Also used the high-quality factor inductor is difficult to implement on chip with CMOS technology. If It is implemented then it will consumes a large area. So to ensure the normal operation of the on-chip inductor, the distance between the inductor and any other components (which include the interconnection metal wire) it should be a

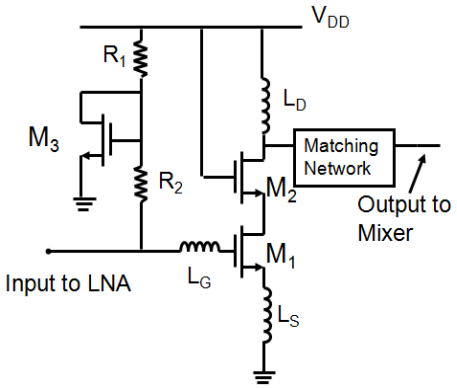

Figure 4 (a)

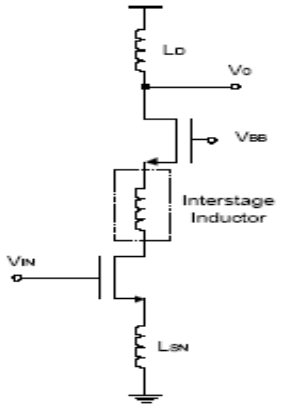

Figure 4 (b)

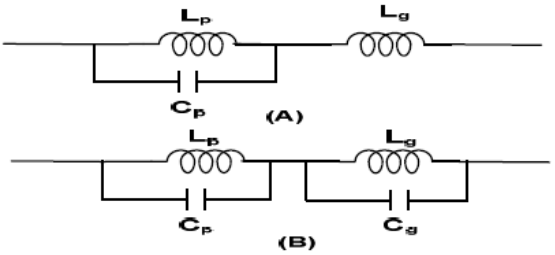

Figure 4 (c)

Figure 4 (a) LNA architecture (b) Inter stage inductor for gain boosting (c) Matching circuit

minimum length while designing the layout. The parasitic resistance of a large inductor contributes large thermal noise. So that use of large-value inductors should be avoided. The proposed Low Noise CMOS amplifier realized in a standard 130 nm CMOS technology with 1.3V supply voltage and consumes power less than 200uW with <1.5mA current. A two stage cascode LNA has to achieved noise figure is less than 2.5dB and achieves a gain >18dB on given frequency range also have good input and output matching.

4. COMPARISON AND DISCUSSION

Table 1

parameters	**Ref . Paper 1.**	**Ref. Paper 2.**	**Ref. Paper 3.**
technology	0.13 um	0.13 um	0.13 um
Supply Voltage	1.8 V	1.2V	1.7V
Gain	12.5dB	16.5 dB	25.2dB
Noise	3.9dB	2.66dB	3.8dB
S11	-16	-11.8	-14
S12	-17	-15	-18
Power consumption and current	2.7mW/ 1.5mA	8.61mW/ 2.68mA	0.6mW/ 0.36mA

As we can see from the above comparison table the proposed Low Noise Amplifier provides high gain and low noise as compared to [1],[2],[3] LNA. Proposed LNA has relatively simple circuitry for gain boosting as compared to the rest of the configuration.

5. CONCLUSION

Different methodologies for Low Noise Amplifier design has been seen above. It shows that 'Low Noise Amplifier has a differential pair' [1] and 'Low Noise Amplifier with Capacitive Feedback with π-matching Technique' [3] has better gain and noise. Proposed Low Noise Amplifier Circuit less power consumption than rest of the techniques. The proposed Low Noise Amplifier can provides high gain > 18dB and less Noise figure < 2.5dB at the expense of low power consumption.

6. REFERENCES

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