Design and Analysis of Area and Power Efficient 1-Bit Full Subtractor using 120nm Technology

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ABSTRACT
In this paper an area and power efficient 14T 1-bit Full Subtractor design has been presented by using GDI techniques. The proposed 1-bit Subtractor design consist of 7 NMOS and 7 PMOS. For difference output of 1-bit full Subtractor GDI XOR-XNOR module outputs has been used with GDI 2x1 MUX. A GDI XOR- XNOR module has been used which consume less area at 120 nm as compared with the previous XOR-XNOR modules. The proposed GDI 1- bit Full Subtractor design is based on this area efficient 6T XOR-XNOR module. To improve area and power efficiency a cascade implementation of XOR module has been avoided in the used 1-bit GDI Full Subtractor module. Difference block of this 1-Bit Full Subtractor module has been implemented by 8 transistors only. The proposed 1-bit Full Subtractor has been designed and simulated using DSCH 3.1 and Microwind 3.1 on 120nm. Also the simulation of layout and parametric analysis has been done for the proposed 1-bit GDI Full Subtractor design. Power variation with respect to the supply voltage has been performed on BSIM-4 and LEVEL-3 on 120nm. Results show that area consumed by the proposed 1-Bit GDI Full Subtractor is 263.1μm^2 on 120nm technology. At 1.2V input supply voltage the proposed 1-bit GDI Full Subtractor consume 7.697μW power at BSIM-4 and 7.708μW power at LEVEL-3. Also the proposed 1-bit GDI Full Subtractor has been compared with other Subtractor designs by CMOS, TG and PTL logic and the proposed design has been proved both area and power efficient as compared to design by other logics.

Keywords
BSIM, CMOS, Gate Diffusion Input, NMOS, PMOS, Pass transistor logic, Very Large Scale Integrated circuit

1. INTRODUCTION
In today's world of technology use of portable devices such as laptops, cell phones and computer has been increased. Power and area consumption has become major concern in schematic design of these portable devices before their actual implementation in the layout. Batteries used in these portable devices have ability to supply limited power. So the no of transistors used in these portable devices must be less as possible to consume less power and area. Also the cost and complexity of any VLSI circuit also depends on the large power dissipation in that circuit. Increased rate of transistors on a single chip can cause increase in both static and dynamic power consumption. Subtractor is one of the most critical components used in the processor of these portable devices. So the area and power efficient design of 1-bit Subtractor is necessary for design of small size portable devices [1]-[2]. There is various possible logic styles that can give better performance as compared to the basic CMOS logic style. The performance estimation of 1- Bit full Subtractor is based on area and power consumption, power delay and Power –Delay Product. Area, speed and power consumption are the main issues in VLSI design which often conflict with each other and the design methodology and act as constrain on the design of VLSI circuits. These performance criteria's should be individually investigated, analyzed for the various designs of the 1-Bit Subtractor by using different logic styles [3]. Power dissipation in any 1-Bit Subtractor circuit depends on both static and dynamic power dissipation. The static power dissipation is the product of the leakage current and supply voltage. The leakage current is described by the equation [4]:

$$i_o = i_s(e^{qV/kT} - 1) \quad (1)$$

Where i_s = reverse saturation current
V= diode voltage
q= electronic charge
k= Boltzmann's constant
T= temperature

The static power dissipation is the product of the leakage current and supply voltage. The total static power dissipation P_s is given by

$$P_s = \sum_{1}^{n} \text{Leakage current} \times \text{Supply voltage} \quad (2)$$

Where n= no of devices

The majority of the power dissipated in CMOS VLSI circuits is due to dynamic power. Thus for performance estimation of 1-bit Subtractor only dynamic power is of interest. During a transition from either '0' to '1' and vice versa both NMOS and PMOS transistors are ON for a short period of time. This results in short current pulse from V_{dd} to V_{SS}. Current is also required to charge and discharge the output capacitive load. With no load capacitance, the "short circuit" current is noticeable. As the capacitive load is increased, the discharge or charge current starts to dominate the current drawn from the power supplies. The dynamic dissipation can be modeled with the assumption that the rise and fall time of the step input is much less than the repetition period. The average dynamic power (Pd), dissipated during switching for a square-wave input (V_{in}), having a repetition frequency of $f_p = \frac{1}{t_p}$, is given by

$$P_d = \frac{1}{t_p}\int_0^{t_p/2} i_n(t)V_{out}dt + \int_{t_p/2}^{t_p} i_p(t)(V_{dd} - V_{out})dt \quad (3)$$

Where i_n = Transient current of n-devices and i_p = transient current of p- devices. For a step input and with $i_n(t) = \frac{C_L d_{Vout}}{dt}$ where C_L =load capacitance we obtain the following expression for the P_d :

$$P_d = \frac{C_L}{t_p}\int_0^{V_{DD}} V_{out} dV_{out} + \frac{C_L}{t_p}\int_{V_{dd}}^{0} (V_{DD} - V_{out}) d(V_{dd} - V_{out}) \quad (4)$$

$$= \frac{C_L V_{DD}^2}{t_p} \quad (5)$$

Substituting $f_p = \frac{1}{t_p}$ in equation (1.9) we get

$$P_d = \frac{C_L V_{DD}^2}{t_p} \quad (6)$$

Hence equation (6) shows that for repetitive step input the average dissipated power is proportional to energy required to charge and discharge the circuit capacitance and switching frequency.

Short circuit power occurs due to signal rise and fall time. During these periods PMOS and NMOS are ON for short period, so there will be a path from V_{dd} to Vss .Short circuit power is part of dynamic power consumption due to its dependency on signal transition and it may presents differently in static and dynamic logic digital logic structure. Basically, CMOS cells have a minimal period of short circuit current flow, but this period increases due to the slower operation in low voltage circuits. Thereby, the short circuit power is a factor of the supply voltage and as voltage decreases shot circuit power consumption will be less due to its direct relation with V_{dd} . Note that t_r and t_f parameters will increase because of V_{dd} reduction.

$$P_{SC} = V_{dd} \cdot \left[\frac{I_{pr} t_r}{2} + \frac{I_{pf} t_f}{2} \right] f \quad (7)$$

Where

I_{pr} : Pick current during the rise-time.

I_{pf} : Pick current during the fall-time.

t_r : Rise-time period.

t_f : Fall-time period.

f : Circuit switching frequency.

Total power dissipation is given by the sum of these three power dissipation i.e. static power dissipation, dynamic power dissipation and short circuit dissipation.

$$P_{total} = P_S + P_d + P_{sc} \quad (8)$$

2. 1-BIT FULL SUBTRACTOR

A 1- Bit full Subtractor is a combinational circuit that performs a subtraction between two binary bits and 1 may have been borrowed by a lower significant stage. This circuit has three inputs and two outputs. Let the three inputs are A, B and C and Borrow and Difference are two outputs of the 1-bit Subtractor and denoted by B_{OUT} and D_{OUT} respectively. Logic diagram of 1-bit full Subtractor has been shown in fig.1.

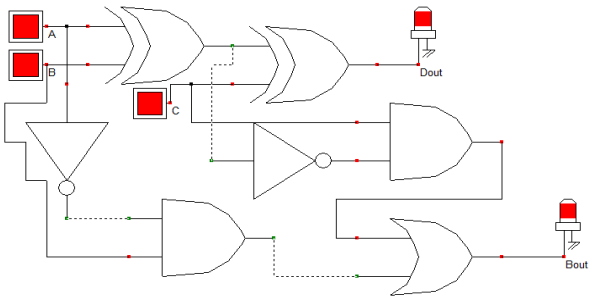


Fig. 1 Logic Diagram Of Full Subtractor [5]

The Boolean Expression for two output variables are given by

$$D_{OUT} = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC \quad (9)$$

$$B_{OUT} = \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + ABC \quad (10)$$

And truth table of Full Subtractor has been shown in Table.1

Table 1. Truth Table of Full Subtractor

A	B	C	D_{OUT}	B_{OUT}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

3. 1- BIT FULL SUBTRACTOR DESIGN

In the recent past various approaches of CMOS 1- Bit full Subtractor design by using various different logic styles has presented and unified into an integrated design methodology. Circuit area, speed and power consumption are the main criteria of concern in CMOS 1- Bit full Subtractor design which often conflict with the design methodology and act as a constrain on the design of comparator circuits. These performance criteria's are individually investigated, analyzed and their interaction to develop both quantitative and qualitative understanding of the various designs have been presented in literature**.**

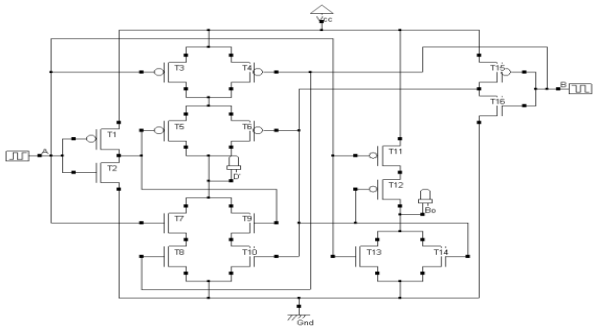


Fig. 2 Transistor level Half-Subtractor Circuit [6]

In Fig.2 a 16T transistor level half Subtractor has been shown which consists 8T PMOS and 8T NMOS transistors. The Subtractor take two inputs called minuend bit (A) and subtrahend bit (B) and two outputs called the Difference bit

(D) and the Borrow bit (B_0). In order to achieve reduction in power consumption two schemes have been used, one is Adaptive Voltage level at supply (AVLS) in which the supply voltage is reduced and the other is Adaptive Voltage Level at Ground (AVLG) in which the ground potential is increased.

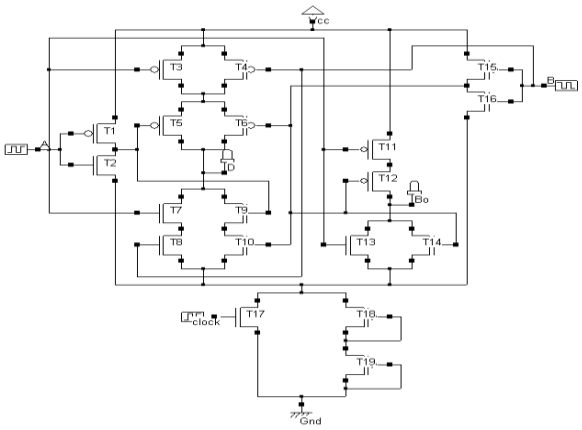


Fig. 3 Half Subtractor using AVLS Technique [6]

Half Subtractor using AVLG scheme is shown in Fig.3 [6]. This scheme is used at the upper end of the cell to bring down the supply voltage level. Use of AVLS scheme is more successful in lowering the value of total power usage of half Subtractor than the AVLG scheme. At transistors T3, T4 there is a decrease in gate-source and gate-drain voltage, which is the major source of reduction of power consumption of the whole circuit. In this scheme it is also observed that an additional loss in power consumption occurs due to the reduction of drain voltages in transistors T2, T3, T6.

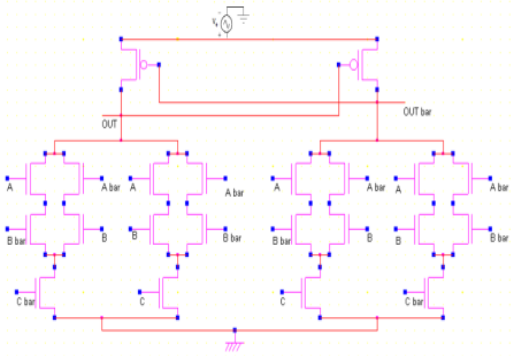


Fig. 4 ECRL Difference Block [7]

A commonly used logic called the adiabatic logic is used to reduce the energy loss during the charging and discharging process of circuit operation. It is also known as "energy recovery" or "charge recovery" logic. The Adiabatic logic instead of dissipating the stored energy during charging process at the output node towards ground, recycles the energy back to the power supply thereby reducing the overall power dissipation and hence the power consumption also decreases. It makes use of AC power supply instead of constant DC supply; this is one of the main reasons in the reduction of power dissipation.

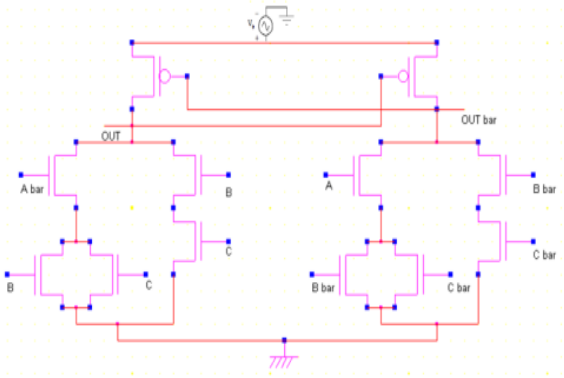


Fig. 5 ECRL Borrow Block [7]

Adiabatic logic has different logic styles which can be used to reduce the power. One is ECRL and difference and borrow block using ECRL logic have been shown in Fig. 4 and 5. Efficient charge recovery logic in the pull up section consists of two cross couple PMOS transistors where as a tree of NMOS transistors is used in the pull down section. Its structure is similar to Cascode Voltage Switch Logic (CVSL) with differential signaling.

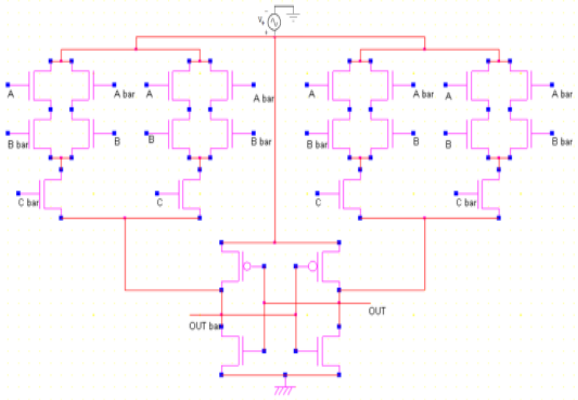


Fig. 6 PFAL Difference Block [7]

Second logic is PFAL logic and difference and borrow block using ECRL logic have been shown in Fig. 6 and 7. The Positive Feedback Adiabatic Logic is also known as PAL-2N (Pass transistor Adiabatic Logic). It is a partial energy recovery circuit. To avoid the logic level degradation on the output nodes, the core of PFAL logic is a latch made up of two PMOS and two NMOS transistors.

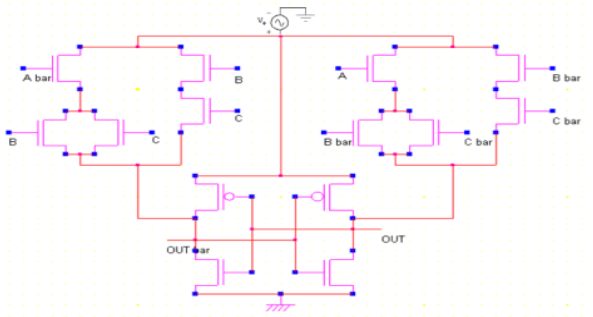


Fig. 7 PFAL Borrow Block [7]

Here NMOS transistors connected in parallel to the PMOS transistors are used to implement the functional block of the

logic function. The main advantage of PFAL over ECRL is that the functional blocks are in parallel with the PMOSFETs forming transmission gate. Also it has the advantage of implementing both the true function and its complimentary function.

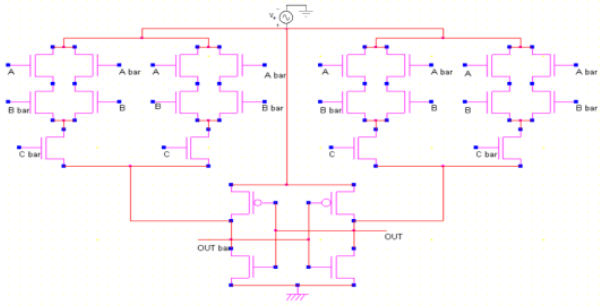


Fig. 8 2PASCL Difference Block [7]

Third logic is 2PASCL logic and difference and borrow block using ECRL logic have been shown in Fig. 8 and 9. The Two Phase Adiabatic Static Clocked Logic (2PASCL) uses two phase clocking split level sinusoidal power supply's which has symmetrical and unsymmetrical power clocks where one clock is in phase while the other is out of phase. The circuit has two diodes in its construction where one diode is placed between the output node and power clock, and another diode connected between one of the terminals of NMOS and power source. Both the MOSFET diodes are used to recycle charges from the output node and to improve the discharging speed of internal signal nodes. The circuit operation is divided into two phases "hold phase" and "evaluation phase". During the evaluation phase, the power clock swings up and power source swings down. During the hold phase, the power source swings up and power clock swings down.

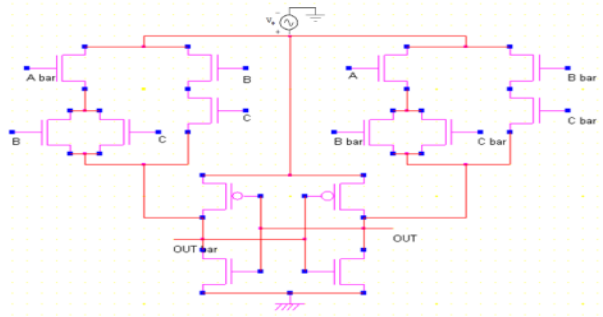


Fig. 9 2PASCL Borrow Block [7]

4. PROPOSED 1- BIT FULL SUBTRACTOR SCHEMATIC

The design of proposed 1-Bit Full Subtractor consists 6T XOR- XNOR module which produce two intermediate signals which are passed to the 2x1 MUX. Two intermediate signals are XOR and XNOR which acts as two inputs to the 2x1 MUX. Third input acts as select line for 2x1 MUX. Output of 2x1 MUX is difference of three inputs A, B and C. borrow is implemented by two AND gates and one OR gate. Proposed 1-bit GDI Full Subtractor has been implemented by using only 14 transistors i.e. difference output has been obtained by 6T XOR-XNOR module and 2T 2x1 MUX and Borrow is obtained by cascading the output of 6T XOR-XNOR module with 6 more transistors.

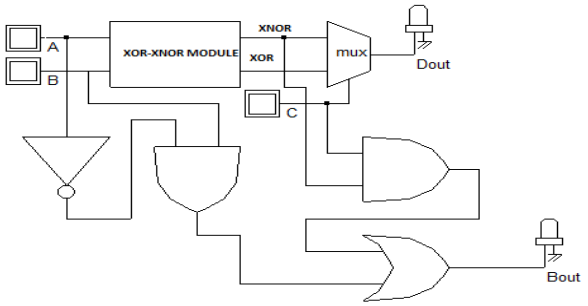


Fig. 10 Logic Diagram of Proposed 1-Bit GDI Subtractor

Difference is realized by as per equation 11 and Borrow is realized as per equation 12.

$$D_{OUT} = C(A\Theta B) + \bar{C}(A \oplus B) \quad (11)$$

$$B_{OUT} = \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + ABC \quad (12)$$

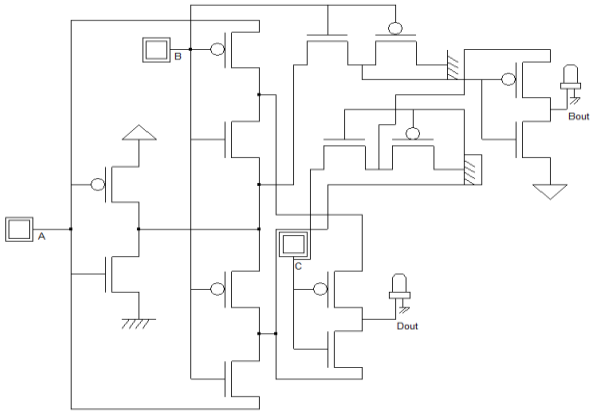


Fig. 11 Proposed GDI 1-Bit GDI Subtractor Design

As shown in Fig.11 the proposed 1-bit GDI Subtractor comparator consist XOR-XNOR modules designed by GDI logic which is area and power efficient as compared to CMOS, TG and PTL XOR-XNOR module. AND gate and OR gate have been implemented by using two transistors each which is lest as compared to designed by CMOS, TG and PTL logic.

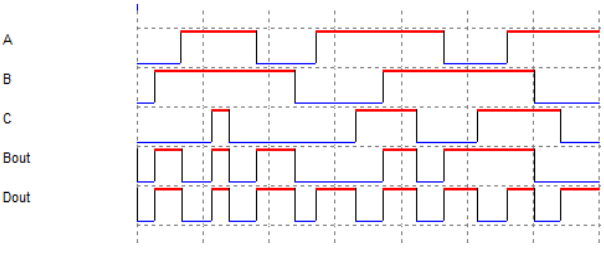


Fig.12 Timing Simulation of GDI 1- Bit Subtractor

Before the actual layout design of 1-bit GDI Subtractor it is necessary to validate the schematic of logic circuit. To overcome this problem DSCH and MICROWIND designing tools works parallel. Firstly the design is simulated in DSCH designing tools to know the exact functionality of the circuit and then implemented on the layout in MICROWIND [8].

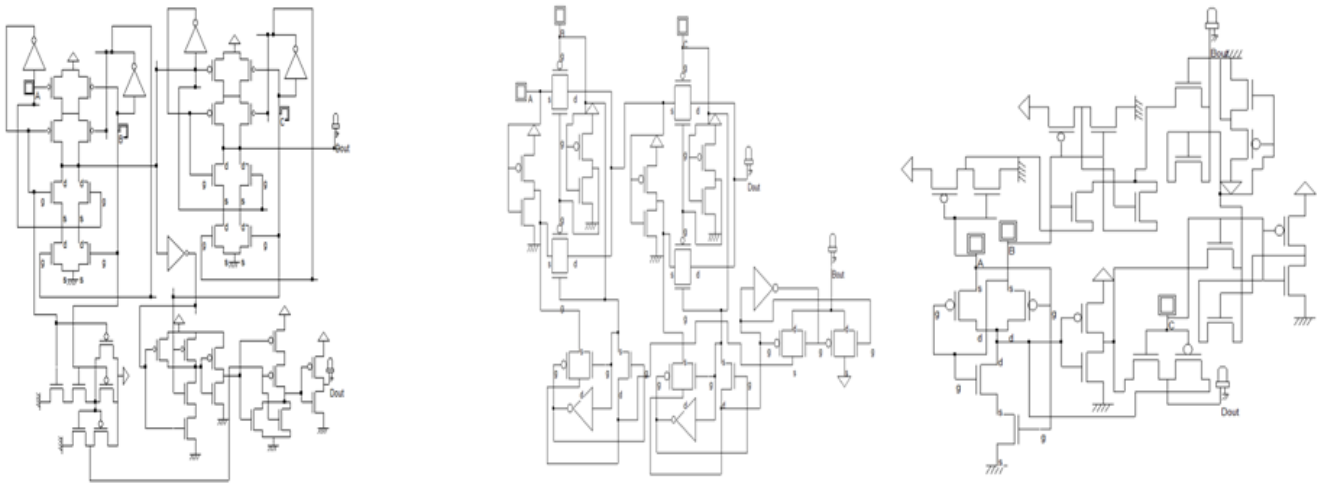


Fig 13.a: CMOS 1- Bit Subtractor Design **Fig 13.b: TG 1- Bit Subtractor Design** **Fig 13.c: PTL 1- Bit Subtractor Design**

Fig 13: 1- Bit Subtractor Design by using different logic

Timing simulation of proposed 1-bit GDI Subtractor has been shown in Fig.12. In order to simulate the 1-bit GDI Subtractor design at logic level the design has been made in the DSCH tool and after launching the simulation the timing waveform can be obtained by chronogram icon. As shown in Fig. 12 the waveform the 1-bit GDI Subtractor is according to required 1-bit GDI Subtractor operation. Timing simulation shows the exact functionality of 1-bit GDI Subtractor for two outputs. The proposed 1- bit GDI Subtractor has been compared with other 1-bit Subtractor designs by the CMOS, TG and PTL logic in terms of area and power in MICROWIND 3.1 designing tool on 120nm technology.

Table 2. Comparative Analysis of 1-bit GDI Subtractor in terms of area with other 1-bit GDI Subtractor design by different logics on 120nm technology

GDI 1-bit Subtractor design	CMOS	TG	PTL	Proposed GDI
NMOS	22	17	14	7
PMOS	22	15	8	7
Width (µm)	79.3µm	58.7µm	44.3µm	31.3µm
Height (µm)	10.8µm	10.8µm	9.4µm	8.4µm
Area (μm^2)	856.7μm^2	633.7μm^2	414.5μm^2	263.1μm^2

Different 1-bit GDI Subtractor designs have been shown in Fig. 13 by using conventional CMOS, TG and PTL. 1-bit GDI Subtractor design by conventional CMOS consist 44 transistors, TG Subtractor consists 32 transistors, GDI Subtractor consists 16 transistors and PTL comparator consists 22 transistors respectively.

5. LAYOUT ANALYSIS

In complex VLSI design manual layout designing for a very complex circuit will become very difficult. So as compared to manual layout designing an automatic layout generation approach is preferred. Layout and post layout simulation of GDI 1- Bit Subtractor has been shown in Fig.14 and 15 respectively

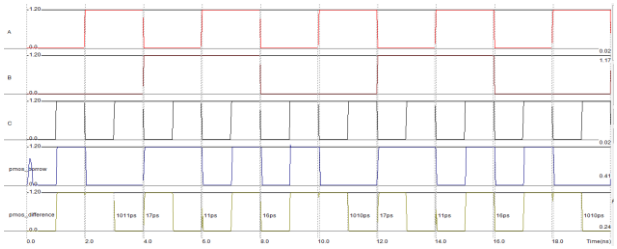


Fig.14 Post Layout Simulation of GDI 1- Bit Subtractor

In DSCH designing tool the schematic diagram has been firstly designed and validated at logic level on DSCH designing tool. Although DSCH 3.1 have feature to analyze timing simulation as well as power consumption at logic level but accurate layout information is still missing. VERILOG file is generated by the DSCH 3.1 tool which is compiled by the MICROWIND to construct the corresponding layout with exact desired design rules. Another way to create the design is by NMOS and PMOS devices using cell generator provided by the MICROWIND 3.1. The advantage of this approach is to avoid any design rule error. Length and width can be adjusted by the MOS generator option on MICROWIND tool.

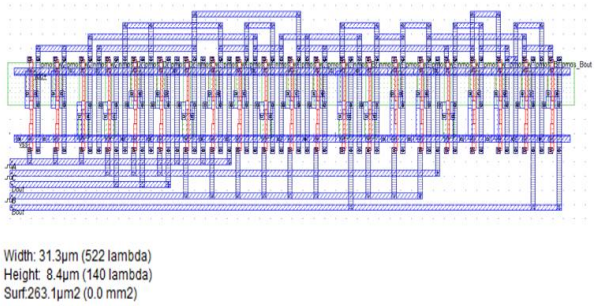


Fig.15 Layout of GDI 1- Bit Subtractor

6. SIMULATION RESULTS

The performance of proposed 1-bit GDI Subtractor design has been evaluated in terms of area and power on 120nm technology. Simulation has been performed using MICROWIND 3.1. Results are measured in terms of variation in power with respect to the variation in voltage on BSIM-4 and LEVEL-3.

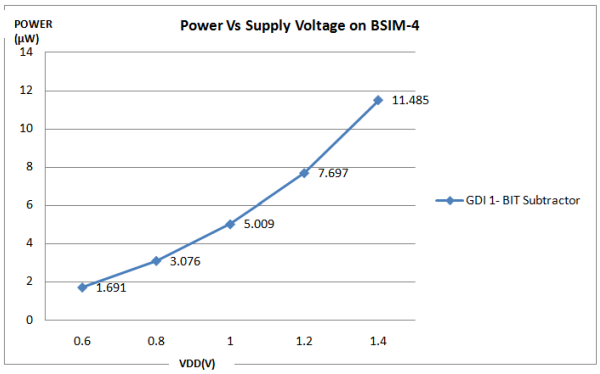


Fig 15: Power vs. Supply Voltage on BSIM-4

Simulation have been performed using the MOS Empherical model Level-3 and BSIM Model-4 at different power Vdd. Threshold voltage has been taken as 0.4V for both levels.

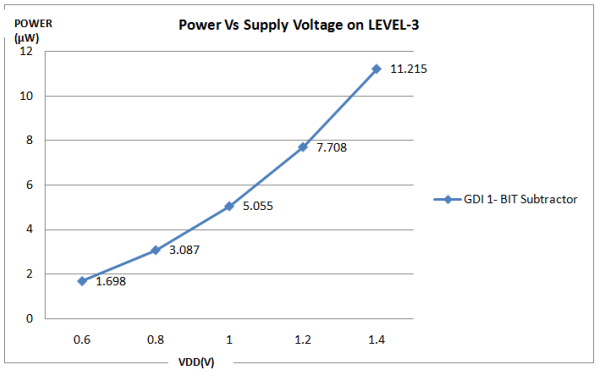
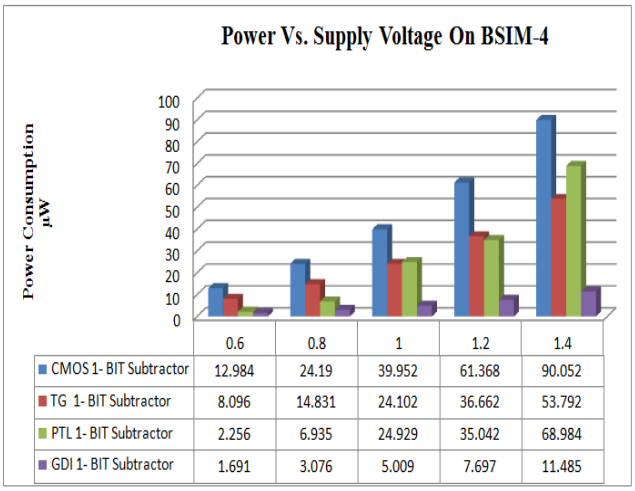


Fig 16: Power vs. Supply Voltage on LEVEL-3

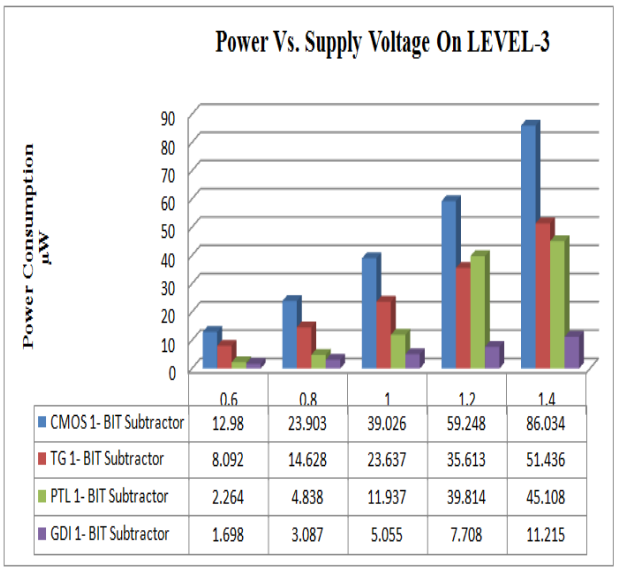
All results have been performed using MOS Empherical model Level-3 and BSIM Model-4 in terms of power and current on voltage levels 0.6, 0.8, 1, 1.2 and 1.4V and operating temperature has been taken 27^0C. 10 different curve fitting parameters has been used in MOS Empherical model Level-3 whereas BSIM Model-4 work with 19 different parameters Results plotted for change in power have been shown in Fig.15 for BSIM-4 and in Fig.16 for LEVEL-3 w.r.t supply voltage and results shows non linear dependence of the power with VDD. Layout result will change on different technology i.e. if we use 120nm or 90nm for same circuit area consumption will be different. Finally the analog simulation has been obtained to know the power consumption at different voltage and temperature by using Microwind 3.1. Analog simulation is carried out for proposed 1-bit comparator on 120nm technology. For 120nm VDD is fixed to 1.2V and VSS to 0V. Simulation can be done by four ways in Microwind 3.1.-Voltage vs. Time, Voltage and current vs. time, Voltage vs. Voltage and Frequency vs. Time. Voltage vs. Time simulation for proposed 1- bit comparator has been done on 120 nm.



	0.6	0.8	1	1.2	1.4
CMOS 1- BIT Subtractor	12.984	24.19	39.952	61.368	90.052
TG 1- BIT Subtractor	8.096	14.831	24.102	36.662	53.792
PTL 1- BIT Subtractor	2.256	6.935	24.929	35.042	68.984
GDI 1- BIT Subtractor	1.691	3.076	5.009	7.697	11.485

Fig.17 Comparison of Power Consumption on BSIM-4

Simulation results have been shown in Fig.17 and 18. From Fig.17 it is clear that power dissipation increases with the power supply. Fig. 17 and 18 also shows that the power dissipation is less at BSIM-4 as compared to LEVEL-3 at 1.2V input supply.



	0.6	0.8	1	1.2	1.4
CMOS 1- BIT Subtractor	12.98	23.903	39.026	59.248	86.034
TG 1- BIT Subtractor	8.092	14.628	23.637	35.613	51.436
PTL 1- BIT Subtractor	2.264	4.838	11.937	39.814	45.108
GDI 1- BIT Subtractor	1.698	3.087	5.055	7.708	11.215

Fig.18 Comparison of Power Consumption on LEVEL-3

7. CONCLUSION

An alternative 1- bit Subtractor design by GDI approach has been introduced which consists only 14 transistors. Proposed 1- bit GDI Subtractor design has been implemented by using 7 NMOS and 7 PMOS transistors. Proposed 1- bit Subtractor design has been designed using an area and power efficient XOR-XNOR module which has been implemented by using only 6 transistors. This area efficient GDI XOR-XNOR module has been used in proposed 1- bit GDI Subtractor design. Area and simulation of proposed 1- bit GDI Subtractor design has been shown on 120nm. The simulation results have been shown on LEVEL-3 and BSIM-4 models. Proposed 1-bit GDI Subtractor design has shown improvement in terms of area as compared to other 1- bit design designs. Results show that area consumed by the proposed 1-bit GDI Subtractor design is 263.1µm^2 on 120nm technology. At 1.2V input

supply voltage the proposed 1-bit GDI Subtractor design consume 7.708 µW power at LEVEL-3 and 7.697 µW power at BSIM-4 model. The proposed 1- bit GDI Subtractor design can work efficiently with minimum voltage supply of 0.4V and can work on wide range of frequency range between 2MHz to 400MHz. simulation results of 1- bit GDI Subtractor design shows that the power consumption is less at BSIM-4 as compared to LEVEL-3 model.

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