Power Efficient Design of Polar Code

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ABSTRACT
Polar codes are the family of the codes which are first ones to achieve channel capacity of any binary discrete memory less channel (B-DMC) with an explicit construction. The method relates with polar codes, channel polarization and encoding & decoding of polar code is considered that in the live structure of polar code when BER gets increase, channel capacity is satisfied but overall power of data transmition in channel gets increase. So here in this analysis the main issue is related with the power consumption. Encoding & decoding construction of polar codes is based on XOR-XNOR gates. The XOR-XNOR circuits' design which uses 6 transistors instead of conventional structure is designed and it is suitable for low-voltage and low-power application by achieving lower delay, power consumption and power-delay product (PDP).So by using this design phenomenon of XOR-XNOR gate it is possible to construct power efficient encoding and decoding of polar codes.

General Terms
Polar codes, Channel Polarization, Encoding, Decoding, Comparition of Conventional & new design of XOR-XNOR gate, Power consumption

Keywords
Polar Code, XOR-XNOR Gate, Power Consumption, Power Delay Product (PDP), Delay, Power Dissipation.

1. INTRODUCTION
Due to the increasing use of portable systems e.g. notebook computers, personal digital assistants, and cellular phones, power is rapidly becoming as important a parameter as area and speed in the design of such systems [9]. The limited power supply ability of present battery equipment has made power consumption an important figure in portable devices So, It is necessary to achieve the power consumption and delay in real time applications for improved use in day to day life and get better generosity. There is clearly need for new technology and design phenomenon that would achieve ultra low power dissipation below performance & cost constrains. The two central topics of information theory are the compression and the transmission of data. Shannon, in his decisive work, dignified both these problem and determined their fundamental limits. Since then the main goal of coding theory has been to find practical schemes that approach these limits. Polar codes, invented by Arıkan, are the first "practical" codes that are known to achieve the capacity for a large class of channels [1]. The encoding as well as the decoding operation of polar codes can be implemented with O (N log N) complexity, where N is the block length of the code [5]. For decoding, he considers applying a simple linear transform to the channel inputs before transmission and a successive cancellation decoder at the output [2]. So by using polar code the complexity and bandwidth is reduced and data rate and channel capacity is increased. But at the otherside overall power of data transmition gets increased. Now when the information bits are encoded and decoded in the channel they are XORed with each other. In encoding structure of polar codes, there is XOR operation is performed at channel combining stage of channel polarization. So here the point of attention is the design criteria of XOR gates. The increasing speed and complexity of today's designs implies a considerable increase in the power consumption problem. To meet this challenge, researchers have developed many different design techniques to reduce power. In brief, by concentrating and take XOR gates as one parameter of the issue of power consumption; it has gone through substantial improvement in power consumption, delay, power delay product, speed and size with its different circuit designs [3]. By adding this approach in polar codes' encoding structure with XOR gate's new circuit design, it might be possible to achieve power consumption at transmission of information of polar code within the channel.

Further the rest of paper is organized as follows: section II deals with a brief technical description of Polar codes with its encoding and decoding part. Section III provides analysis of concept of power consumption and requirement of it. Section IV, Power consumption with XOR circuit gives brief introduction of XOR-XNOR gate. Section V provides technical comparison of other circuit designs of XOR gate with proposed circuit design and finally section VI delivers the conclusions.

2. POLAR CODE
Polar codes are recently invented in 2008 [7]. This code can achieve the symmetric capacity which is the highest capacity of the channel with same probabilities for any given Binary Discrete Memoryless Channel (B-DMC) [5]. The encoding and decoding capacity of polar code is O (N log N). Here N is Block Length of code and the complexity is n log N. so this is a big achievement and this can solve the big open problem of Coding Theory.

2.1 Encoding of Polar code
Basically, polar codes were constructed using a generator matrix created using the Kronecker power of the base matrix $G_2 = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}$ to the block of N= 2^n bits. This construction method yields polar codes whose lengths are powers of two. For example, the generator matrix of an n=8 polar codes are:

$$G_8 = G_2^{\otimes 3}$$
$$= \begin{bmatrix} G_2 & 0_2 & 0_2 & 0_2 \\ G_2 & G_2 & 0_2 & 0_2 \\ G_2 & 0_2 & G_2 & 0_2 \\ G_2 & G_2 & G_2 & G_2 \end{bmatrix}$$
$$= \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}$$

Fig 1: Generator Matrix of n=8

Generally what is done here, that the information bits of Polar codes work by encoding an information vector u into a codeword X by multiplying it with a generator matrix G, using X= u.G. This resulting vector is then transmitted over a communication channel. A decoder receives a noisy version of X called Y from the output of the channel. This decoder then estimates the original information vector u as showen in Figure 2.

2.2 Channel Polarization

A method is proposed to constrict code sequences that achieve the symmetric capacity of any given B-DMC is called *channel polarization*, [7]. It works with two operations, one is channel combining and other is channel splitting [1]. Channel Polarization synthesize N channel of B-DMC then it split into noiseless channel (called good bit channel) approaching the capacity of $I(W)$ or into a pure noise channel (called bad bit channel) approaching 1- $I(W)$ [1].So by using this sort of polarization method the construction of Polar codes is done in which data is send through those channel with high capacity and fix the inputs through those channels with low capacity.

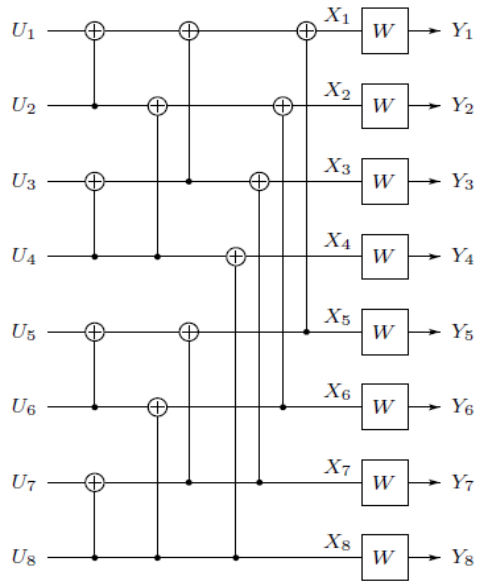

Fig 2: Combining of Channels

2.3 Decoding of Polar code

The decoding of polar code is done by using successive cancellation algorithm and belief propagation algorithm

2.3.1 Successive Cancellation Decoding Algorithm

In [4] Tal and Vardy have proposed SC decoder and its different architectures like,

2.3.1.1 Butterfly-based architecture:

In [4] it is showed that SC decoding can be efficiently implemented by the factor graph of the code similar to Fast Fourier transform. The Butterfly-based SC decoder based on this fact. The successive cancellation decoding algorithm is based on the sum-product algorithm. It makes use of the *equality* and *parity* constraints introduced by the encoding graph to carry out a soft estimation of the information vector. Figure 3 illustrates the graph of SC decoder for n=8.

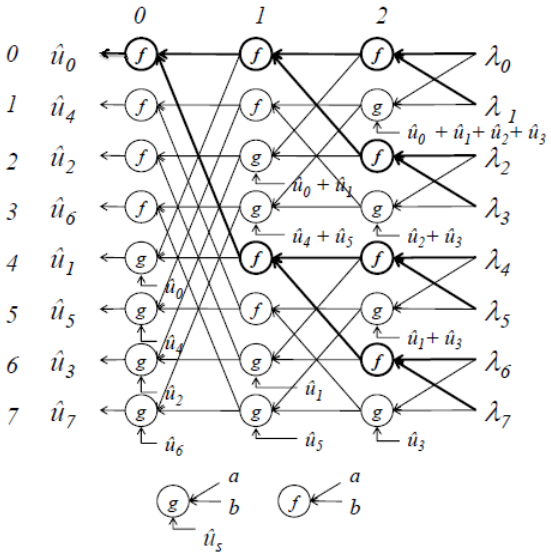

Fig 3: The Butterfly-based SC decoder Architecture for n=8 [4]

In this architecture, λ_0 to λ_7 input bits are given which are basically the outputs of channel. By doing fast Fourier transformation on this bits we get the original transformed data bits u_0 to u_7.

Despite this well defined structure and scheduling of the butterfly-based decoder, drawback of this architecture is that it does not address the problem of resource sharing, memory management or control generation that would be required for hardware implementation [4]

2.3.1.2 Pipelined Tree Architecture:

Further study is about pipelined tree architecture in which the scheduling reveals that whenever stage l is activated, only 2^l nodes are actually updated. For example, in Figure 3, when stage 0 is enabled, only one node is updated. Then the n nodes of stage 0 can be implemented using a single processing element (PE). As such, for stage l, 2^l processing elements are sufficient to update all the nodes. However, this resource sharing does not necessarily guarantee that the memories assigned to the merged nodes can also be merged. Table I shows the stage activation during the decoding of one vector y.

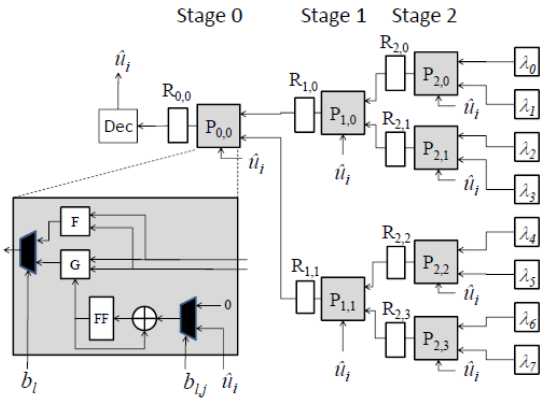

Fig 4: Pipelined tree Architecture for n=8 [4]

TABLE 1: Schedule for the butterfly based and pipelined tree SC architectures (n=8)

cc	1	2	3	4	5	6	7	8	9	10	11	12	13	14
S_2	f							g						
S_1		f			g				f			g		
S_0			f	g		f	g		f	g		f	g	
u_1			u_0	u_1		u_2	u_3		u_4	u_5		u_6	u_7	

Here a decision unit generates the estimated bit ˆui which is then broadcast back to every PE. A PE is a configurable element that can perform either the f or the g function. It also includes the ˆus computation block that updates the ˆus value with the last decoded bit ˆui only if the control bit bl,j = 1. Another control bit is used to select the f or g function. Compared to the butterfly-based structure, the pipelined tree architecture performs the same amount of computation with the same scheduling (see Table 1) but with a smaller number of PEs and registers. The throughput is same and the decoder has lower hardware complexity,

$$C_{tree} = (n-1)(C_{PE} + C_r) + nC_{r,} \qquad (1)$$

Where, C_{PE} represent the complexity of single PE. Also with lower complexity tree architecture is much simpler compare to butterfly-based architecture. In tree architecture the PE's connections are local which lowers the congestion ratio and increase clock frequency and the throughput.

2.3.1.3 Processing Elements:

The processing element is the main arithmetic component of the pipeline decoder. It embodies the arithmetic logic needed to perform both f and g functions within a single logic component. This grouping, motivated by the fact that all stages of the decoding graph either perform function f or g at any given time, allowed a greater level of resource sharing.

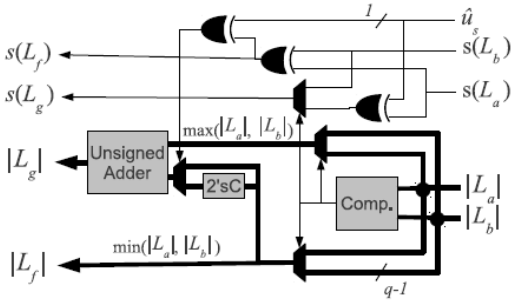

Fig 5: Processing element architecture [4]

Figure 5 illustrates the overall architecture of our SM-based PE. In this figure, La and Lb are the two q-bit input LLRs of functions f and g; a partial sum signal ˆus controls the behaviour of g; the sign s(.) and the magnitude |.| of input LLRs are directly extracted; and the comparator is shared for the computation of |Lf |, |Lg| and s(Lg). Thick lines and thin lines represent magnitude and sign data paths, respectively.

2.3.2 Belief Propagation Decoding Algorithm

Thought A Successive cancelation decoding is the capacity-achieving property of the polar code, Belief Propagation decoding obtain better BER performance while keeping the decoding complexity at O (N log N). The BP is an algorithm that helps to solve inference in graphical models. More accurately, it provides estimates of the subsequent marginal distributions of the variables, called beliefs. To obtain the beliefs, the BP passes messages iteratively between the variable nodes and the check nodes, according to their neighborhood dependence. Belief propagation decoding is easily obtained by adding check nodes to the polar code as it is shown in figure 3 for length n=8.it is also called "Tanner Graph" of the code. The graph is formed of columns of variable nodes and check nodes. In the tanner graph, each variable node v has a set of check nodes as its neighbors, denoted by Cv. The check nodes in Cv also have a set of variable nodes Vv as their neighbors from which we exclude v. We refer to Vv as"depth-2 neighborhood" of v and we call the members of Vv"depth-2 neighbors" of v.

In [10] they are particularly interested in the analysis of"stopping sets" in the tanner graph of the polar code, as an important cause of the decoding failure and error floor. A stopping set is a set of variable nodes such that every neighboring check node of the set is connected to at least two variable nodes in the set. Fig. 6 shows an example of the stopping set in the polar codes' graph.

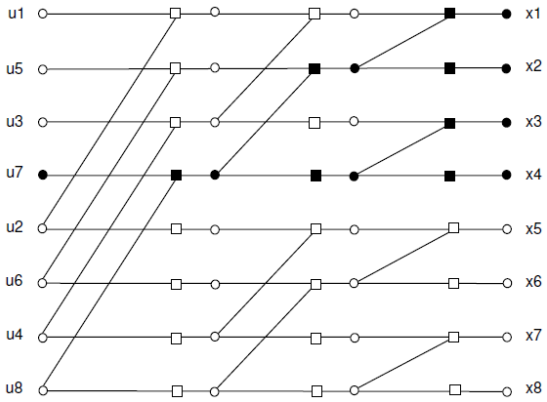

Fig 6: Normal realization of the encoding graph for N = 8. An example of the stopping set is shown with white variable and check nodes [10]

It is easy to see that if all the variable nodes in a stopping set are erased, then none of them can be decoded in belief propagation. Further, if any of the variable nodes in a stopping set is decoded then all of them can be decoded [10]. As a result, the probability of decoding error is closely related to the probability of having a stopping set with erased variable nodes. Since the stopping set with the minimum number of variable nodes, called "minimal stopping set", is more probable to be erased than larger stopping sets, it plays the dominant role in the error probability. Therefore, in code design, codes with large minimal stopping sets are desired for making its decoding

So, by using both this algorithm we can decode the code bits which are output of the transmition channel. But here it is noticed that BP performs better than SC in terms of BER.

3. CONCEPT OF POWER CONSUMPTION

The growing speediness and complexity of today's designs implies a considerable increase on the power consumption issue. To meet this challenge, researchers have developed many different design techniques and try to reduce power. In today's market scenario, battery lifetime is a important factor for the commercial success of the product. A high absolute level of power is not only undesirable for economic and environmental reasons, but it also creates the problem of heat dissipation. In order to keep the device working at acceptable temperature levels, excessive heat may require expensive heat removal systems.

The low-power design has become a major design consideration the limited power supply ability of present battery tools has made power consumption an important figure in portable devices. The speed of the design is limited by size of the transistors, parasitic capacitance and delay in the critical path. The driving capability of a full adder which is designed by using XOR gates is very significant, because, full adders are principally used in cascade construction, where the output of one provides the input for other. In the last decade, the design criteria of XOR gates has gone through significant expansion in power consumption, speed and size, but at the cost of weak driving capability and reduced voltage swing. However, reduced voltage swing has the benefit of lesser power consumption.

4. POWER CONSUMPTION WITH XOR CIRCUIT

The XOR and XNOR gate functions are shown in Table 1 and denoted by ⊕ and ⊙ respectively [3]. The logic expression for XOR and XNOR are:

$$A \oplus B = A'B + AB' \qquad (2)$$

$$A \odot B = A'B' + AB \qquad (3)$$

TABLE 2: XOR-XNOR gate Function

INPUT A	INPUT B	OUTPUT A XOR B	OUTPUT A XNOR B
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

XOR based circuits have good testability properties at least if they are limited to specific subclasses of AND/XOR forms and thus are well suited for design for testability. Now, constrains like size, performance and testability of XOR based circuits have been studied, approach of power consumption is also taken as most important factor into account. The primary concern to design XOR-XNOR gate is to obtain low power consumption and delay in the critical path and full output voltage swing with low number of transistors to implement it. Due to the important role played by XOR and XNOR gate in various circuits especially in arithmetic circuits, optimized design of XOR and XNOR circuit to achieve low power, small size &delay is needed [9].

5. TECHNICAL COMPARITION OF EXISTING CIRCUIT DESIGNS OF XOR GATE

Numerous designs were reported to realize the XOR-XNOR functions using different number of circuit techniques and approaches as in [6], [8] and many more. They are very in methodologies and transistor count to improve the circuit performance. The XOR-XNOR circuits design in static CMOS with complementary pull-up PMOS and pull-down NMOS networks is the most conventional one but it requires more numbers of CMOS transistors. The circuit can operate with full output voltage swing. In [6] The XOR and XNOR circuits are based on the modified version of a CMOS inverter and pass transistor logic (Figure 7 and 8) .This circuit designs claimed to have lower PDP, less power dissipation and faster with a low supply voltage. However both of the circuits give a poor signal output voltage in certain input combination.

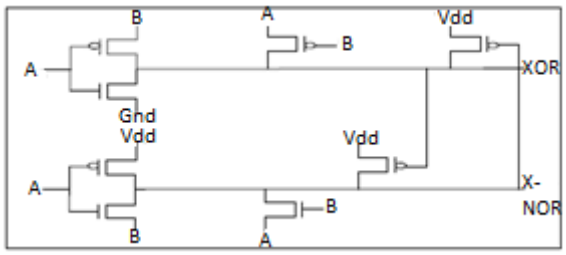

Fig 7: XOR-XNOR Gate Using 8 Transistors [6]

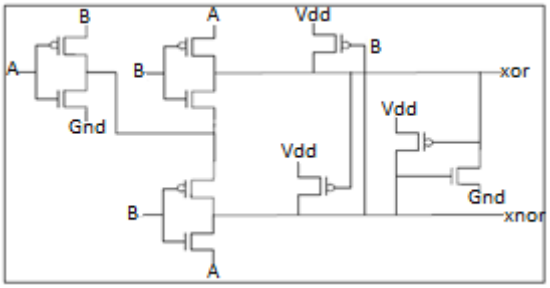

Fig 8: XOR-XNOR gate using 10 transistors [6]

Also it is described in [3] that Complementary pass transistor logic (CPL) is used in some usual Reported design of XOR-XNOR circuits based on transmission gates. It uses eight transistors and opposite inputs and has a drawback of loss of driving capability. Also in past, some designs of XOR-XNOR circuits are based on inverter gates. It does not require a complementary inputs but it has no driving capability because there is no direct connection to Vdd and Gnd. The improved version of this circuit has been designed by adding a standard inverter to the output. This modified circuit provides a good driving capability but uses twelve transistors for XOR-XNOR circuits.

Now in [4] Ahmad and hasan proposes a new design of combination of XOR-XNOR gate using 6-transistors for low power applications. It offers the lowest power dissipation at a low supply voltage And Better performance especially in low supply voltage compared to the previous designs by reducing the no. of transistor in circuit design. Thus, the proposed circuit is suitable for low-voltage and low-power application. So, here we are going to use this new circuit design of XOR-XNOR gate in to the conventional structure of encoding and

decoding of polar code and the old design of XOR-XNOR gate with 8-transistor is replace by this new one. By merging this both approach we are going to achieve overall power consumption with polar codes at transmission of information within the channel.

6. CONCLUSIONS

Thought Polar codes provably achieve capacity for any symmetric binary-input discrete memory less channels (B-DMC). In practice, channel properties may change with time, therefore it is important to analyze the performance of the constructed code for channel model e.g. BEC or BSE with different noise level. Also the main point of attention is Problems with previous reported XOR design which are Delay, Power Dissipation & PDP are solved by new proposed circuit design. It fulfils the clear need to obtain low power consumption and delay constrains in broadcasting data in Channel. So, this phenomenon is used instead of the conventional design of XOR gate and it is replaced by new proposed XOR-XNOR circuit in the encoding & decoding structure of polar code to achieve overall power consumption of data transmition in channel.

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