

Design and Comparative Analysis of SRAM Cell Structures using 0.5 μm Technology

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ABSTRACT

In rapid development of digital designs, memory is the most important building block, as half of the silicon area is used to store data value and program instructions. The power consumption and speed of SRAMs are important issue that has lead to multiple designs with the purpose of minimizing the power consumption. Speed and power consumption is the key parameter in ADC resolution. In this paper, we design and analyze 4-bit flash ADC by using 0.5 μm CMOS technology in Tanner Tool. In the proposed design, we are using TIQ comparator and mux based encoder for converting analog signal in to digital signal, and analog input range is between 0 to 1.36V, with the supply voltage of 2.5V. Here we work on low power consumption of comparator which can be achieved by varying W/L ratio of PMOS and NMOS of TIQ comparator. The tool used for simulation purpose is S-Edit, T-Spice, W-Edit by Tanner Tool using hp0.5 μm CMOS technology at supply voltage of 2.5volts.

Keywords

SRAM cell, 6T SRAM cell, 8T SRAM Cell, 10 SRAM Cell and SNM

1. INTRODUCTION

From last 5 decades, CMOS devices are scaling down to achieve the better performance in terms of speed, power dissipation, size and reliability which can be done by making memories compact and faster or by decreasing size of memory i.e. SRAM (Static Random Access Memory). SRAM is a type of semi-conductor memory which uses bi-stable latching circuitry to store single bit. It is volatile in nature; it means that it holds the data as long as power supply is not cut off. SRAM plays an important role in modern mobile phones, microprocessors, microcontrollers, and computers etc. SRAM and DRAM (Dynamic RAM) both holds the data but in different manners. DRAM requires the data to be refreshed periodically in order to retain the data. SRAM does not need to be refreshed (therefore called static) as the transistors inside would continue to hold the data as long as the power supply is not cut off. The additional circuitry and timing are needed to refresh the DRAM periodically, which makes DRAM memory slower and less desirable than SRAM.

As device size is scaled, random process variations significantly degrade the noise margin. As the sizing of the SRAM is in nanometer scale the variations in electrical parameters (e.g., threshold voltage, sheet resistance) reduces its steadily due to the fluctuations in process parameters i.e., density of impurity concentration, oxide thickness and diffusion depths. Considering all these effects, the bit yield for SRAM is strongly influenced by V_{DD} , threshold voltage (V_{th}), and

transistor-sizing ratios. Therefore, it is complicated to determine the optimal cell design for SRAM. The transistor mismatch can be described as two closely placed identical transistors have important differences in their electrical parameters as threshold voltage (V_{th}), body factor and current factor and make the design with less predictable and controllable. The stability of the SRAM cell is seriously affected by the increase in variability and decrease in supply voltage V_{DD} [1].

Conceptually, an SRAM has the structure shown in Fig.1. It consists of a matrix of 2^m rows by 2^n columns of memory cells. Each memory cell in an SRAM contains a pair of cross coupled inverters which form a bi-stable element. These inverters are connected to a pair of bitlines through NMOS pass transistors which provide differential read and write access. An SRAM also contains some column and row circuitry to access these cells. The $m+n$ bits of address input, which identifies the cell which is to be accessed, is split into m row address bits and n column address bits. The row decoder activates one of the 2^m word lines which connect the memory cells of that row to their respective bitlines. The column decoder sets a pair of column switches which connects one of 2^n bitlines columns to the peripheral circuits.

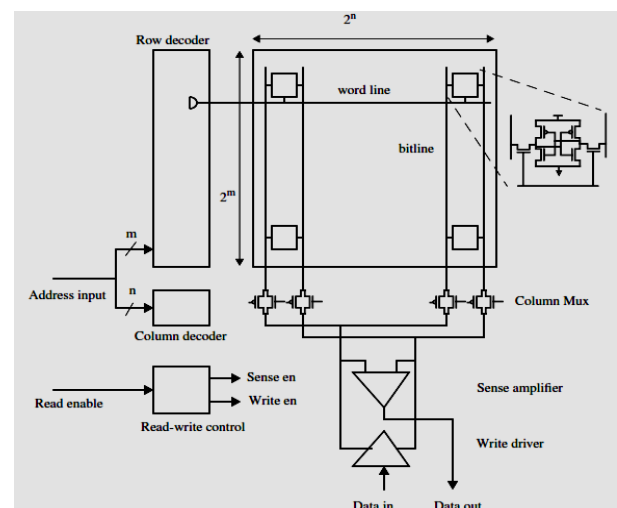


Fig. 1: Elementary SRAM structure with the cell design in its inset

1.1 Conventional 6T SRAM Cell Structure

1.1.1 Architecture and working

The 6T SRAM cell can be designed by using two PMOS transistors and four NMOS transistors as shown in fig.2. It consists of two crossed coupled inverters and two access

NMOS transistor M5 and M6. These two cross-coupled inverters, which are connected back to back, are used for storing one bit of information at a time (either 0 or 1). The two additional access transistors serve to control access to a storage cell during read and write operations. This access to the cell is enabled by the word line (WL) which controls these two access transistors M5 and M6 which, in turn, control whether the cell should be connected to the bit lines, bit and bitbar [7]. They are used to transfer data for both read and write operations. The value of bit and bitbar is inverted. When bit is high then bitbar will be zero and vice-versa.

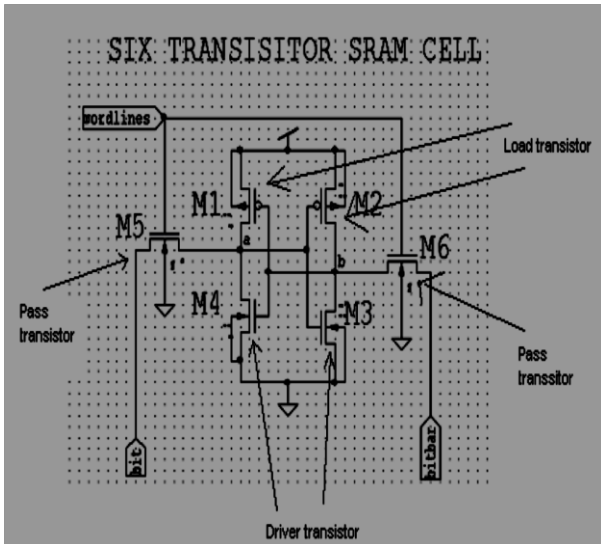


Fig.2 : Cell structure of 6T SRAM Cell.

In the SRAM cell of fig.2., upper PMOS transistor in both the cross coupled inverter is termed as the load transistor and lower NMOS transistor in cross coupled inverter is termed as the driver transistor and the NMOS which connect the cell to the outside word will be termed as the pass transistor.

An SRAM cell has three different states or operation: standby (where the circuit is idle), reading (when the data has been requested) and writing (when updating the contents)[8].

(a) Standby Mode

When word line is not asserted (word line=0), the access transistors M5 and M6 disconnect the cell from bit lines. The two cross coupled inverters formed by M1-M4 will continue to reinforce each other as long as they are connected to the supply. So when WL=0, access transistors M5 and M6 are off and data held in the latch.

(b) Read Mode

Assume that 1 is stored at node a. The read cycle is initiated by pre-charging bit-lines to high voltage pulse, and then asserts word line high. Word line enables both the access transistor which will connect cell from the bit lines. The second step occurs when the values stored in a and b are transferred to the bit lines. One of the bit line will discharge through the driver transistor and the other bit lines will be pull up through the Load transistors toward V_{DD} , a logical 1[2].

If the content of the memory were a 0, the opposite would happen and bitbar line would be pulled toward 1 and bit line toward 0. Then these bit and bitbar will have a small difference of delta between them and then these lines reach a sense amplifier, which will sense which line has higher voltage and thus will tell whether there was 1 stored or 0. The higher the sensitivity of sense amplifier is faster is the speed of read operation of SRAM. Design of SRAM cell requires

read stability (do not disturb data when reading). For read stability node 'a' must not flip and $M4 \gg M5$.

(c) Write Mode

Assume that the cell is originally storing a 1 and we wish to write a 0. To do this, the bit line is lowered to 0V and bit bar is raised to V_{DD} , and cell is selected by raising the word line to V_{DD} . Each of the inverters is designed so that PMOS and NMOS are matched, thus inverter threshold is kept at $V_{DD}/2$. To write 0 at node a, M5 operates in saturation. Initially, its source voltage is 1. Drain terminal of M4 is initially at 1 which is pulled down by M5 because access transistor M5 is stronger than M1. Now M2 turns on and M3 turns off, thus new value has been written which forces bit line lowered to 0V and bit bar to V_{DD} . SRAM to operate in write mode must have write-ability which is minimum bit line voltage required to flip the state of the cell.

1.2 Conventional 8T SRAM Cell Structure

1.2.1 Architecture and working

The 8T SRAM cell consists of 8 transistors, N1-N5 and P1-P3, as shown Fig. 3. Four transistors N1, N2, P1, P2 form a cross-couple structure to store data. Four transistors P3 and N3- N5 are access to the internal nodes D and /D of the cell. N3 and N4 connect the cell internal nodes D and /D of the cell. N3 and N4 connect the cell internal nodes to the BLs while P3 and N5 form an inverter to control the voltage of node C1. The source terminal of P3 is connected to a column select (CS) line while gates of P3 and N5 are connected to WL. Unlike conventional design, the sources of P1 and P2 are connected to dynamic cell supply (cell_supply) line which is raised to the higher voltage during read operation to obtain a higher noise margin [10].

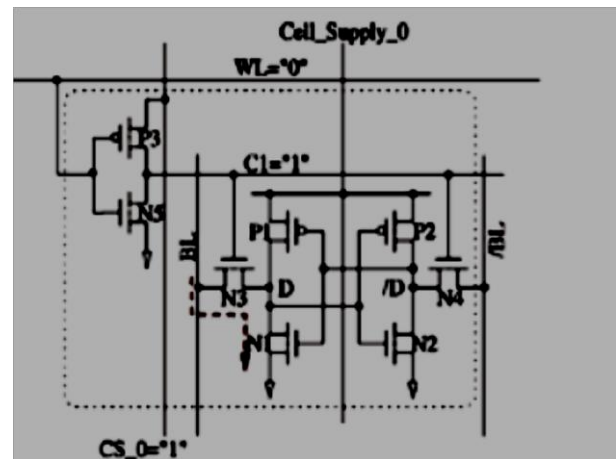


Fig.3 : Cell structure of 8T SRAM Cell

During Read operation in 6T SRAM cell, the fundamental stability problem occurs. In order to reduce leakage power consumption, pre-charge voltage for bit-lines is kept much lower than the cell supply voltage [13]. When the transistors are turned on, the '0' logic node is pulled up to a poor '0' level and the '1' logic node is pulled down to a poor '1' level; this may lead to flip the cell data. In the 8T SRAM cell, three MOSFETs are introduced to separate the read and write current paths and to avoid the accidental flipping of cell during read operation as shown in fig.4.

It can also be seen from the fig 4 that M5 and M6 transistor are connected to write line and M7 and M8 transistor are connected to read line and also these transistors are high

voltage transistor that means threshold voltage is higher for these transistors as compared to normal transistor[14]

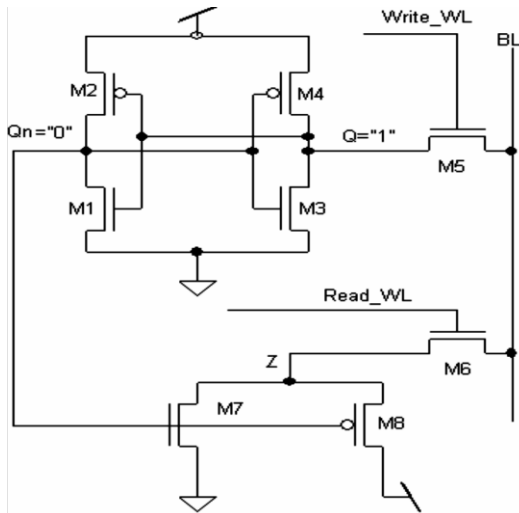


Fig.4: Cell structure of 8T SRAM Cell.

(a) Read Operation

Read operation in 8T cell is performed by using MOSFETs M6, M7 and M8 as shown in Fig.4. Bit-line is pre-charged to logic '1' for successful read operation. Node 'Qbar' is connected to the gates of M7 and M8 transistors. When transistor M6 is turned 'ON' using Read_Word_Line, current starts flowing in and out of the read circuit. Sense amplifier is used to read the cell data by sensing the Bit-Line voltage fluctuation. The amplifier detects the voltage difference of its inputs. For read '1' operation, the initial states of Q and Qbar are assumed to be '1' and '0' respectively. As 'Qbar' node stores '0' logic, on turning 'ON' M6 transistor, it enables the M8 (PMOS) transistor which in turn charges the Bit Line through M8 and M6. The sense amplifier detects the bit swing and output '1' is obtained.[9] During read '0' operation Read Word Line enables the M6 and as 'Qbar' node stores logic '1', it turns on M7 (NMOS) which discharges the Bit-Line through M7 and M6 and logic '0' is obtained at the output.

(b) Write Operation

In this cell structure of 8T SRAM cell only single bit-line is used for read and write operation as compared to conventional 6T SRAM cell as shown in Fig.4. During write '1' operation, enabling the Write Word Line will turn on M5 transistor. As the Bit Line is charged to logic '1' for write '1' operation, the 'Q' node starts charging and turns on M1 which leads to flip 'Qbar' node to logic '0'. Now 'Qbar' node helps enabling the M4 which facilitates writing logic '1' at 'Q' node.

On the other hand, during write '0' operation, the Bit Line is charged to logic '0' and M5 turns on, by enabling Write Word Line signal. The 'Q' node starts discharging and turns on M2 which in turn flips 'Qbar' node to logic '1'. Now 'Qbar' helps turning M3 on, which facilitates discharging 'Q' node properly, and consequently logic '0' is obtained at 'Q' node [16].

1.3 Conventional 10T SRAM Cell Structures

1.3.1 Architecture and working

10T SRAM cell of fig.5, consist of two pair of CMOS inverters, in which one pair is directly connected to *bit* and

bit_ line which avoids the leakage power through *bit* lines (*bit* and *bit_*) and V_{DD} [10] and reduces drain to source subthreshold current. As compared to 6T cell, 10T cell shows less read and write time delay on different scale. Extra transistors is the only drawback of this architecture.[12]

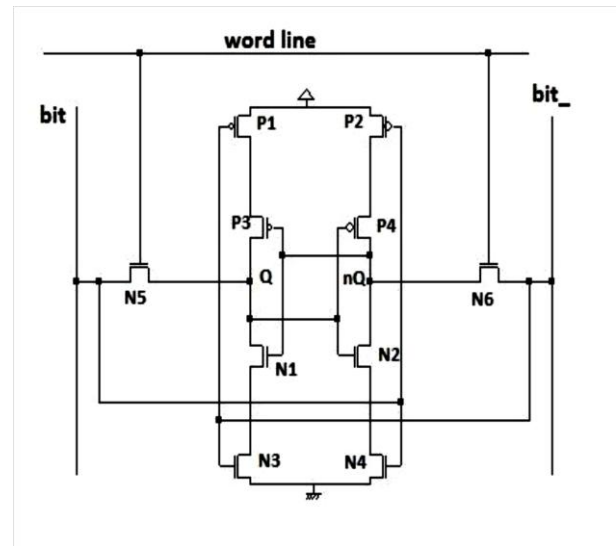


Fig.5: Cell structure of 10T SRAM Cell.

(a)Read Operation

For read operation bit and bit_ line are kept in floating condition in that case if Q is high then it will transfer bit "1" on bit line. and if nQ is high then it will transfer bit "0". In this read operation P1 and P2 are responsible for reducing the delay because of their initial high resistance. And for reading bit "0" on bit line series P3 and P4 are responsible for reducing delay [15].

(b)Write Operation

For storing bit "1" on SRAM cell, *bit* and address line goes high. Transistor N5 passes bit "1" on cross-coupled CMOS inverter. For storing bit "1" transistor P1 and P2 are on and for storing bit "0" on cell bit line goes low and N5 passes bit "0". When address line goes low its makes pass transistors N5 and N6 off. At this instant N3 and N4 limits the sub threshold current and bit line discharging which enhances the performance of 10T SRAM cell.

2. DESIGNED STRUCTURE

This work is carried out under the environment of Tanner software. In this design, Schematic-Editor (S-Edit) is used for schematic diagram. T-Spice is used for generating Netlist and Waveform editor (W-Edit) is used for generating waveform. Spice simulator is used for simulation, by using hp0.5μm technology. The supply voltage is 2.5V.

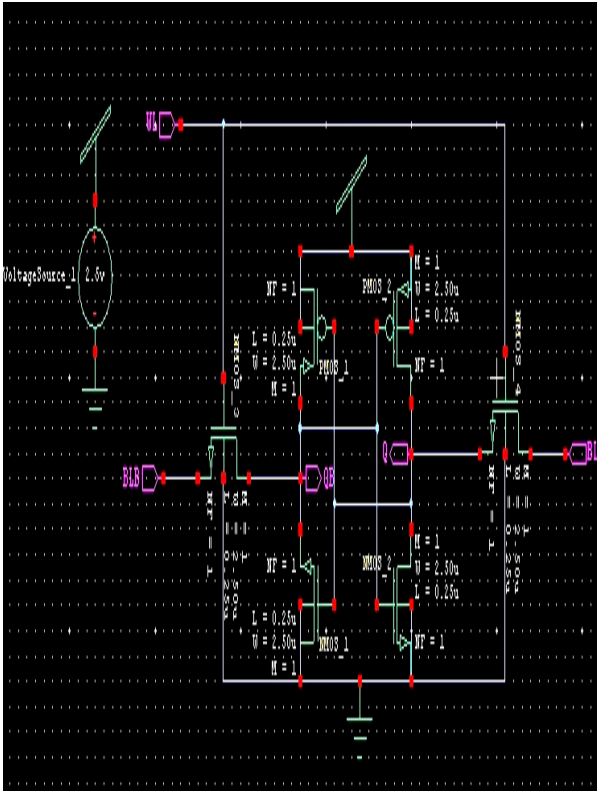


Fig.6 Designed structure of 6T SRAM cell

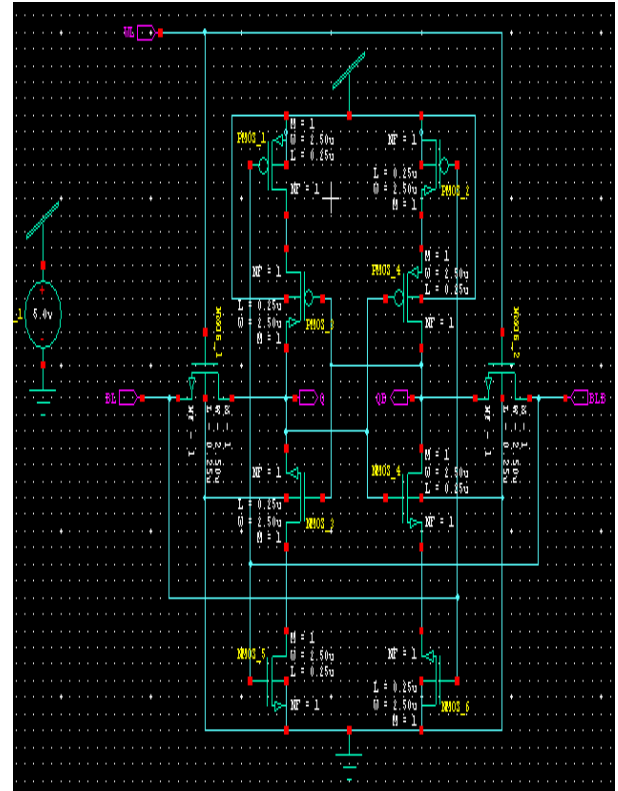


Fig.8 Designed structure of 10T SRAM cell

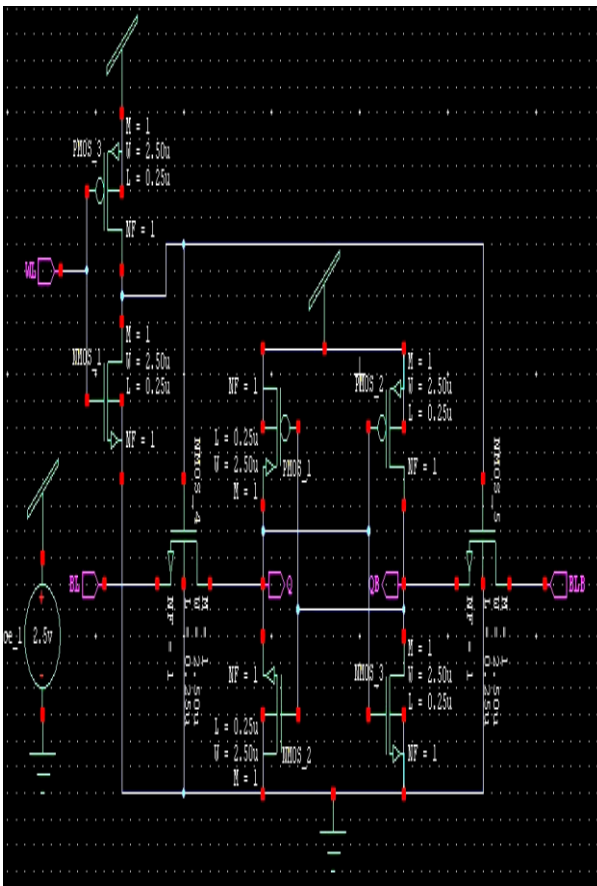


Fig.7 Designed structure of 8T SRAM cell

3. RESULT AND ANALYSIS

Waveform is generated by using W-Edit. The transient response of various cells is given below

3.1 Simulation Results of 6T SRAM Cell

The transient response of designed 6T SRAM cell of fig.6. is presented in fig.9

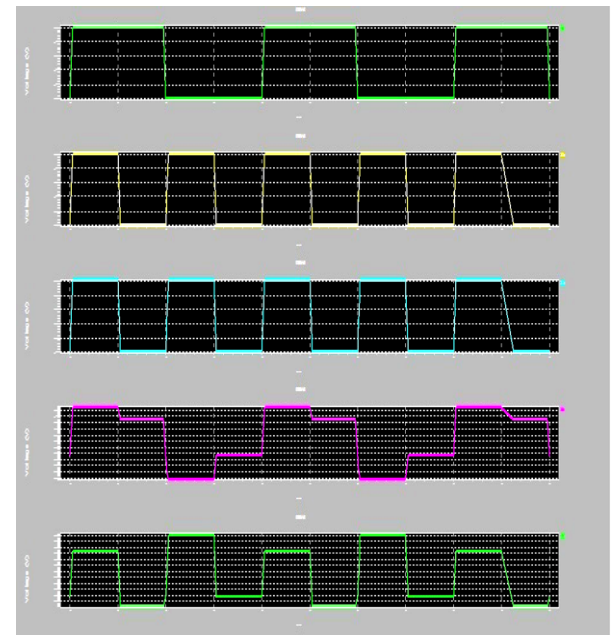


Fig. 9: Transient Response of 6T SRAM Cell

3.2 Simulation Results of 8T SRAM Cell

The transient response of designed 8T SRAM Cell of this fig.7. is presented in fig.10.

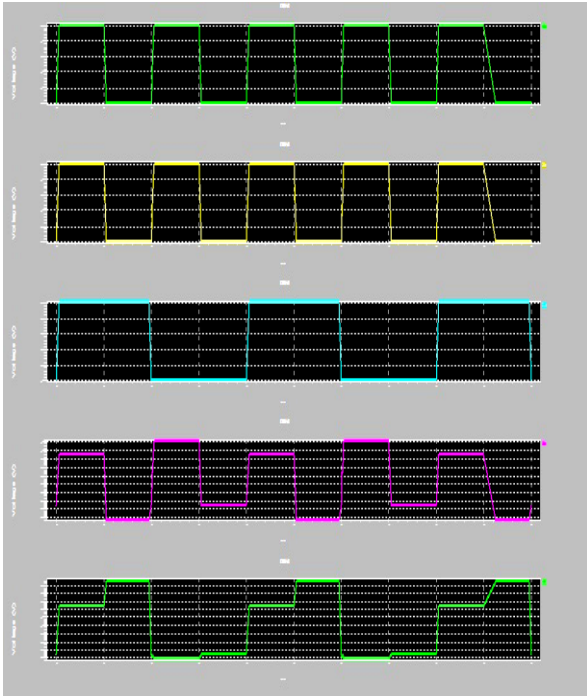


Fig. 10: Transient Response of 8T SRAM Cell

3.3 Simulation Results of 10T SRAM Cell

The transient response of designed 10T SRAM cell of fig.8. is presented in fig.11.

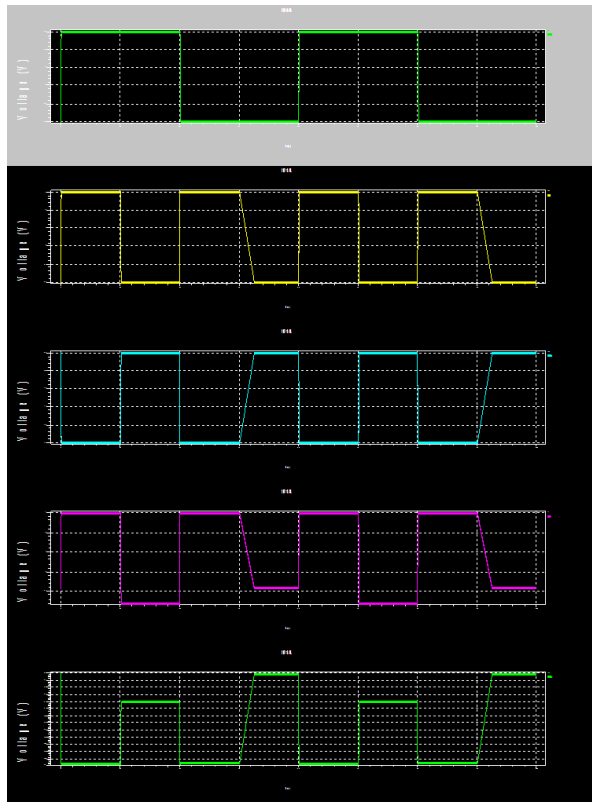


Fig.11: Transient Response of 10T SRAM Cell

3.4 Comparative Analysis Using Various Parameters

From the above design and implementations, RAM has been compared on the basis of following parameters and its

performance has been analyzed. The final results for the delay, power dissipation and SNM are shown in table 1

Table.1 Performance Parameter of the Various SRAM Cell Structure

S. No	Performance Parameter	6T SRAM Cell	8T SRAM Cell	10T SRAM Cell
1	Technology	hp 0.5 μ m CMOS	hp 0.5 μ m CMOS	hp 0.5 μ m CMOS
2	Supply Voltage	2.5V	2.5V	2.5V
3	No. Of NMOS transistor	4	5	6
4	No. Of PMOS transistor	2	3	4
5	Frequency(Hz)	5MHz	8MHz	10MHz
6	Power consumption (Watt)	1.25 μ W	1.37 μ W	1.487 μ W
7	Delay(Sec)	3n	0.8n	0.5n
8	Static Noise Margin	Highest	Medium	Lowest
9	Stability	Highest	Medium	Lowest

For comparative analysis of 6T SRAM cell, 8T SRAM cell and 10T SRAM cell, hp0.5 μ m technology has been used . On the basis of NMOS transistor whose number is varying from 4,5,6 and PMOS transistor whose number is varying from 2,3,4 for 6T SRAM cell, 8T SRAM cell and

10T SRAM cell respectively, with the same supply voltage of 2.5V,it had been analyzed that-

- (c) For 6T SRAM cell-Keeping frequency 5MHz, it is found that power consumption is 1.25 μ W and delay is 3nsec.
- (d) For 8T SRAM cell- Keeping frequency 8MHz, it is found that power consumption is 1.37 μ W and delay is 0.8nsec.
- (e) For 10T SRAM cell- Keeping frequency 10MHz, it is found that power consumption is 1.487 μ W and delay is 0.5nsec.

From the above values, it can be concluded that the power consumption of 6T SRAM cell is lesser in comparison to 8T SRAM cell and 10T SRAM cell whereas Static Noise Margin is highest for 6T SRAM cell and lowest for 10T SRAM cell. Also it can be seen that the stability will be highest in 6T SRAM cell than in comparison with 8T SRAM cell which is having medium and 10T SRAM cell which is having lowest stability. Thus 10T SRAM cell has lowest delay and SNM and thus achieves better performance as compared to 6T and 8T SRAM cell.

4. CONCLUSION

It has been concluded that if the number of transistor is increased in the SRAM cell the power dissipation will be increased due to increase in area, but other parameter like noise, delay can be reduced during read and write operation. So the optimum case is taken between speed, power and area.

Our aim is to reduce delay and SNM for increased area or for increased number of transistor. Both delay and SNM is reduced but at the penalty of area and power, as extra number of transistors are used. Present trend is likely towards lower delay and noise margin and this work results is beneficial to observe the impact of aging of all three SRAM designs. Thus it can be concluded that at 2.5 supply voltage, 10T SRAM cell has lowest delay and SNM and thus achieves better performance as compared to 6T and 8T SRAM cell at hp0.5µm technology.

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