A Novel High Performance Low Power Universal Gate Implementation in Subthreshold Region

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ABSTRACT
In any integrated circuit power consumption plays a paramount role and is considered as one of the top challenges in International technology roadmap for semiconductors. In this paper, a low power circuit designed to operate in subthreshold region is proposed. Voltage scaling technique is incorporated to reduce dynamic power consumption while static or leakage power is greatly reduced with forced stack technique. The present technique (VS-STACK) features very low power dissipation as compared to its standard CMOS counterparts in subthreshold region. The power consumption is curtailed by 20% to 90% together with a better power delay product (PDP) over a supply voltage range. The technique is tested on a 2-input NOR gate in the 45nm process. Tanner Tool EDA 13.0v is used for simulation.

General Terms
Power Consumption, Power Delay Product.

Keywords
Subthreshold, Voltage Scaling, Forced Stacking.

1. INTRODUCTION
With increase in the use of VLSI design in mobile applications, power consumption has become a primary concern. Recently, subthreshold logic circuit has emerged as a promising technique for ultra-low power applications [1] [2]. In these circuits, the supply voltage is less than the threshold voltages of transistors which helps in reducing both static and dynamic power.

CMOS logic design family is extensively used today for subthreshold circuits. The power consumption in these circuits is composed of static and dynamic parts. Dynamic power is given by the equation $P=CV^2f$ [3], where C is circuit loading, V is supplied voltage and f is clock frequency. Dynamic power dissipation consumes most of the power as V_{DD} supplies the circuit's parasitic capacitance during CMOS switching, so this voltage must be controlled to keep dynamic power within tolerable levels. However static power dissipation is due to junction leakage, subthreshold leakage and gate oxide leakage. But as technology scales down, leakage power becomes comparable to dynamic power dissipation because of reduced threshold voltage and device geometry.

Many techniques have been deployed to reduce both static and dynamic power dissipation. Dual threshold voltage-voltage scaling (DTVS) is a hybrid technique which incorporates Dual threshold voltage (DTV) and voltage scaling technique to suppress leakage and dynamic power dissipation and hence reduces total power consumption. Stacking of transistors [4] is a method to reduce leakage power. The forced stacking introduces an additional transistor for every input of gate in both PMOS and NMOS circuit network. In this brief, a novel low power circuit is proposed which incorporates the conventional dynamic voltage scaling (DVS) along with stacked NMOS transistors (VS-STACK). The proposed technique suppresses both dynamic and leakage power dissipation which reduces the overall power consumption. The circuit is operated in subthreshold region which further reduces the overall power consumption. The total power is reduced by 20% to 90% as compared to the existing techniques.

The paper is organized as follows: Section II gives an overview of existing methods for power reduction. Section III analyzes Voltage Scaling technique (VS). Section IV analyzes forced stack technique. Section V presents the proposed technique for low power and better performance. Section VI comprises of simulation results and section VII concludes the paper.

2. EXISTING METHODS FOR POWER REDUCTION
Numerous methods have been proposed to reduce both leakage and dynamic power dissipation. Dynamic power dissipation is generally reduced by lowering supply voltage, voltage swing or switching activity. Low Power V_{DD}-Management technique [5] reduces power consumption by exploiting a rising and charge sharing technique. This technique considerably reduces dynamic power consumption without deteriorating the circuit performance. The LPVS technique is very efficient even if the technology scales down say for 60nm or 45nm. Dual Threshold Voltage (DTV) and Voltage Scaling (VS) are merged to form a new hybrid technique called Dual Threshold Voltage-Voltage Scaling technique (DTVS) [6].

A technique for leakage power control is Power Gating [7] which introduces additional transistors (sleep transistors) in between either supply or ground and circuit. The sleep transistors are turned on while circuit is in active mode and turned off when the circuit is standby mode. In the standby mode, a virtual power and ground rail is created by the sleep transistor to reduce leakage power. The Multi-Threshold Voltage CMOS (MTCMOS) [8] technique has emerged as a very popular technique for reducing standby mode leakage power. It is similar to power gating technique which incorporates high threshold transistors as sleep transistors and

low threshold transistors for implementing logic. Dual Threshold Voltage (DTV) [9] is a variation of MTCMOS technique, which uses transistors having two different threshold voltages. Low threshold transistors are used for gates in critical paths while non-critical paths employ high threshold transistors.

3. VOLTAGE SCALING TECHNIQUE

Voltage Scaling Technique has been widely embraced technique for the abatement of power consumption through leakage. Now, as per the equation $P=CV^2f$, we can see that the average power dissipation is in proportion to V^2, where V is the supply voltage. In the Figure 1, when S=1 then N5 is in active state and P5 is in cut-off state which discharges the capacitor C1 and due to low V_p level transistor P5 is turned on. This makes the externally applied V_{DD} to fully charge the

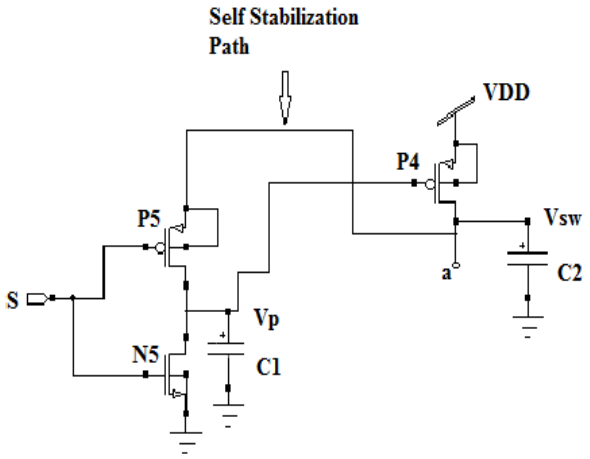

Fig 1: Voltage Scaling and Charge Sharing Circuit

capacitor C2. When N5 and P5 transistors are low then the current in P4 is determined by the voltage difference in PMOS transistors. The Self Stabilization path helps in charge sharing between C1 and C2 capacitors. Vsw, Vtp and V_{DD} shares a relation which is: $Vsw \leq V_{DD} - V_{TP4}$. When clock makes a transition from high to low P5 becomes active and thus Vsw is dropped to a value very lower than V_{DD}. Hence, the sole purpose of Voltage Scaling technique is to reduce the dynamic power consumption.

4. FORCED STACK TECHNIQUE

Another approach by which we can reduce the power due to leakage is by employing forced stack [10] technique, in which an existing transistor is broken down into two transistors half the size of the actual one and this effect is known as the stack effect. Now when implemented in a circuit, these two half size transistors when goes into a cut-off state a reverse bias is induced between the two which culminate in reducing the subthreshold leakage current. This technique generally reduces power dissipation when the circuit is in standby mode, i.e. when it is not working.

In Figure 2, the pull up network and pull down network transistors with W/L = 3 is divided into two set of transistors with W/L = 1.5 each. The only pitfall in the stack approach is that the delay increases significantly due to the divided transistors and hence, can border the effectiveness of the approach.

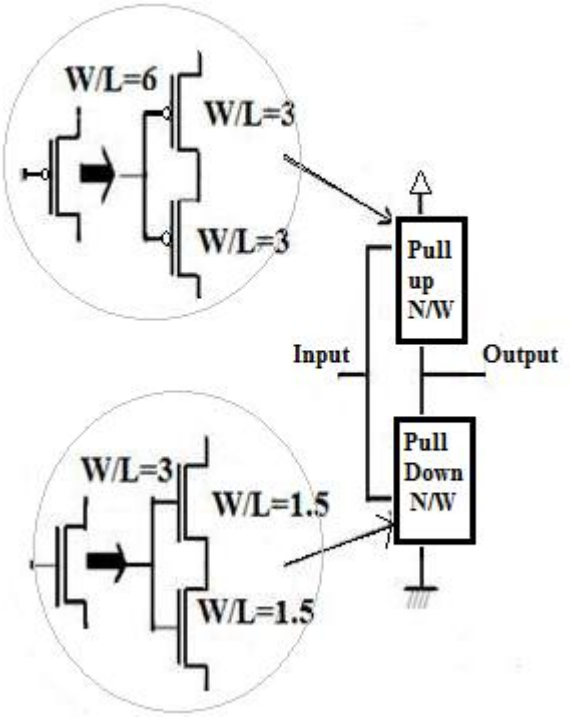

Fig. 2: Forced Stack Approach

5. PROPOSED VOLTAGE SCALING STACKED TRANSISTOR TECHNIQUE

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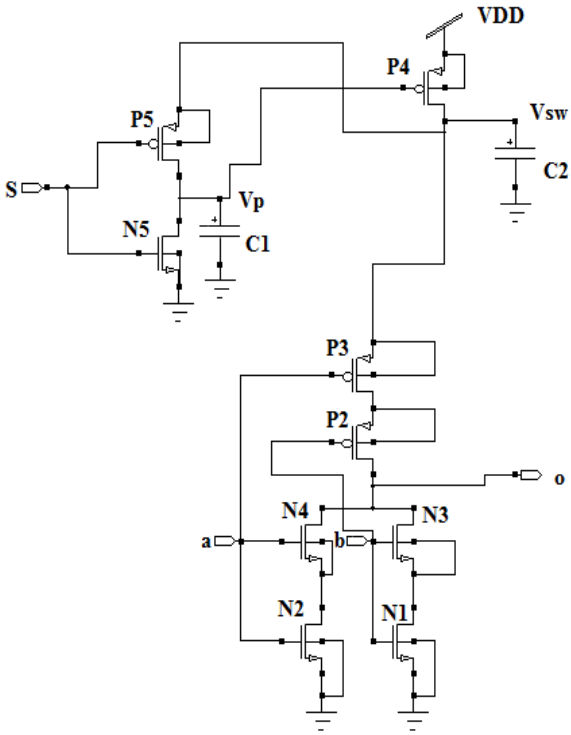

Fig 3: Proposed VS-STACK Technique

The proposed Voltage Scaling and Stacked transistor technique is shown in Figure 3. The proposed technique is

implemented on a NOR gate which is a universal gate. This technique employs Voltage Scaling and charge sharing technique which reduces the dynamic power dissipation without degrading the speed of the circuit. When S goes high then N5 turns on, which in turn enables the transistor P4 and hence voltage is fully supplied to the circuit. Now, when S goes from high to low, transistor P4 turns off. In this situation value of Vsw declines from V_{DD} level to a lower voltage level given by $V_{DD} - V_{TP4}$. During this period capacitor C2 shares charge with capacitor C1 through the Self Stabilization path. If the Vp level becomes too low then the transistor P4 might get turned on. This will raise the level of Vsw and at the same time helps to maintain a low level of variation in Vsw when signal S transits. Hence, the primary function of Voltage Scaling and Charge Sharing technique is to reduce the dynamic power consumption.

This technique also deploys forced stacking technique which helps us to abate the leakage power by splitting an existing transistor into two transistors where the W/L of each of the dissevered transistor is half as compared to the original transistors. In our circuit given in fig. 3 transistors N2 and N1 are stacked transistors such that (N1, N3) and (N2, N4) represents the two half sized transistors. When signal S is high and the two half sized transistors, i.e. (N1, N3) and (N2, N4) are turned off simultaneously, then the induced reverse bias between these transistors helps in abatement of leakage current. Similarly, when S goes from high to low, then the stacked transistors help in reducing leakage current by increasing the resistance of the path from power supply to ground.

The proposed technique helps to abate both dynamic and static (leakage) power consumption which in turn reduces the overall power consumption. This technique also features better Power Delay Product (PDP) as compared to its standard CMOS, Voltage Scaling and Stacked transistor approach.

6. SIMULATION RESULTS

The present technique is implemented on a 2-input CMOS NOR gate as shown in Fig. 3. Simulation results are obtained using Tanner EDA Tool 13.0v at 45nm CMOS process.

Table 1. Power consumption of 2-input NOR gate

Power Consumption(W)				
V_{DD} (V)	**Standard CMOS (W)**	**Voltage Scaling (W)**	**Stacked Transistor (W)**	**VS-STACK (W)**
0.6	7.731E-08	6.934E-08	6.351E-08	3.193E-08
0.5	4.712E-08	1.596E-08	3.953E-08	9.612E-09
0.4	2.824E-08	3.693E-09	2.329E-08	3.119E-09
0.3	1.463E-08	1.022E-09	1.180E-08	7.968E-10

The circuit is operated in subthreshold region, where the supply voltage V_{DD} is varied from 0.3V to 0.6V, which is less than the threshold voltages of the transistors used in our circuit.

Table 1 shows the power consumption (W) when operated in subthreshold region. The VS-STACK technique consumes up to 58.69% less power than the standard CMOS and 49.72% less power as compared to stacked transistor technique at 0.6V.

Similarly, at 0.5V the proposed technique consumes 79.60% and 75.68% less power as compared to standard CMOS and Stacked transistor technique. The same circuit at 0.4V and 0.3V shows a great reduction in power consumption as compared to standard CMOS and Stacked transistor technique. The power consumption is reduced by 88.95% and 86.60% at 0.4V while at 0.3V the decrease in power is more than 90%.

Figures 4 and 5 shows how VS-STACK technique outshined the existing standard CMOS and Stacked transistor technique in terms of power consumption when operated in subthreshold region.

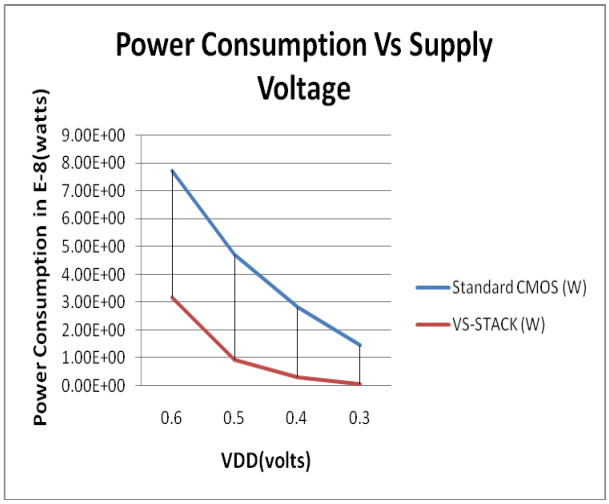

Fig. 4: Power Consumption Vs Supply Voltage

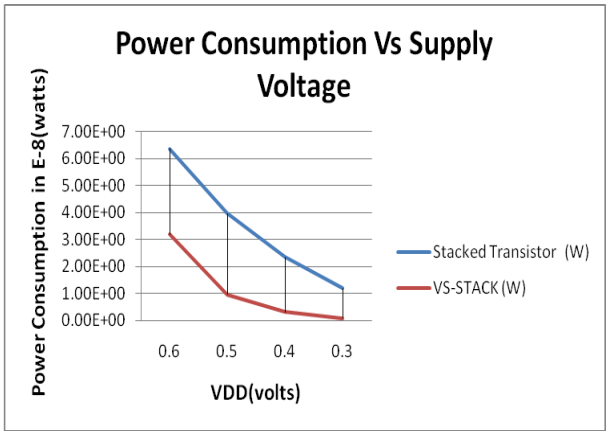

Fig. 5: Power Consumption Vs Supply Voltage

The VS-STACK technique consumes 53.95% less power than the Voltage Scaling technique at 0.6V. At 0.5V it consumes 37.77% less power than Voltage Scaling technique. A 15.15% and 22.03% reduction in power consumption is seen when the

circuit is operating at 0.4v and 0.3V. Figure 6 shows the comparison between VS-STACK and Voltage Scaling in terms of power consumption.

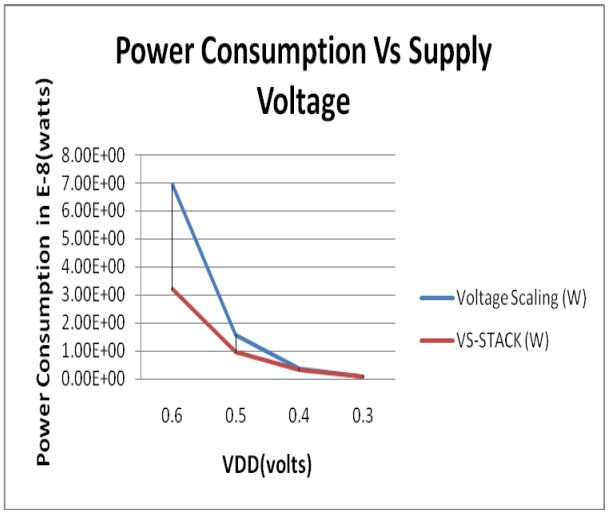

Fig. 6: Power consumption Vs Supply Voltage

From Table 1 VS-STACK approach shows uniform results at different operating voltages resulting in significant reduction of power consumption. The reduction is power is due to the combined effect of both Voltage Scaling and Stacked transistor approach. Dynamic power dissipation is reduced by Voltage Scaling technique while Stacked transistors technique curtails leakage power when the circuit is in standby mode, i.e. when signal S is low.

Figure 7 displays the graph of power consumption Vs supply voltage V_{DD} for 2-input NOR gate.

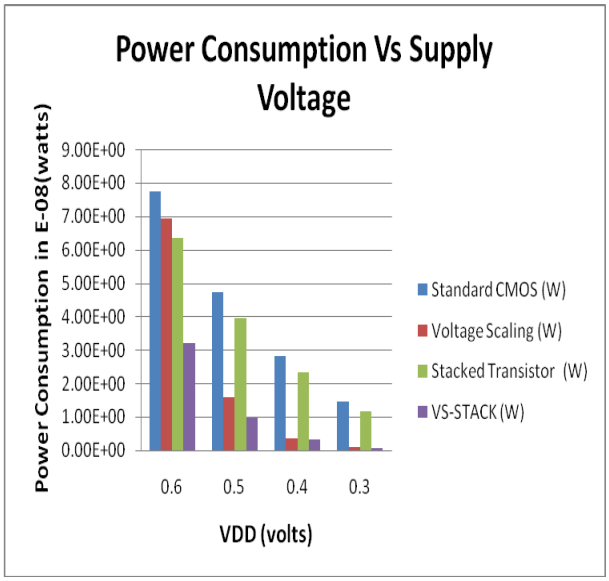

Fig. 7: Power Consumption Vs Supply Voltage for 2-input NOR gate

Table 2 shows Power Delay Product (PDP) at various operating voltages. The PDP of VS-STACK, as compared to the other existing techniques, is very less. The circuit shows consistent results at different supply voltages. Hence the proposed technique prevents the degradation of the speed of the circuit. The reduction in PDP of VS-STACK as compared to standard CMOS is 55.41% at 0.6V and it further reduces by 68.08% at 0.3V. When compared to the Voltage Scaling technique, the PDP of VT-STACK is 52.65% less at supply voltage 0.6V. The reduction in PDP of the proposed technique lies between 13.64% and 72.98% when compared with the stacked transistor technique. Figure 8 shows the Power Delay Product of 2-input NOR gate operating in subthreshold region.

Table 2. PDP for 2-input NOR gate

Power Delay Product(fWsec)				
V_{DD} (V)	**Standard CMOS (fWsec)**	**Voltage Scaling (fWsec)**	**Stacked Transistor (fWsec)**	**VS-STACK (fWsec)**
0.6	0.240	0.226	0.191	0.107
0.5	0.998	0.553	0.381	0.329
0.4	1.628	0.777	0.814	0.493
0.3	2.118	0.914	2.502	0.676

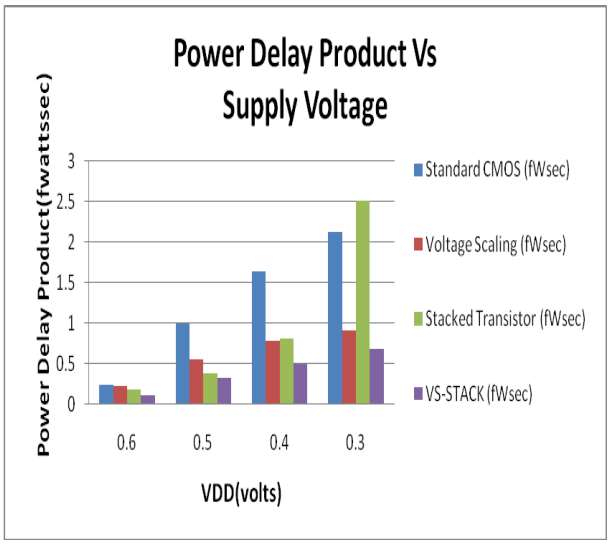

Fig. 8: Power Delay Product Vs Supply Voltage for 2-input NOR gate

Table 3. Area (Number of Transistors)

Design Technique	Standard CMOS	Voltage Scaling	Stacked Transistor	VS-STACK
Number of Transistors	4	7	6	9

Table 3 shows the Layout Area in terms of number of transistors required by each design technique. The proposed technique requires more number of transistors as compared to the existing techniques. But the tremendous reduction in

power consumption and an increase in the performance of circuit outweigh the area overhead.

7. CONCLUSION

In this paper, a new power reduction technique called Voltage Scaling Stacked Transistor (VS-STACK) has been presented. The proposed technique has been compared with some of the existing power reduction techniques. The result shows a colossal amount of reduction in power consumption for the 2-input NOR gate. The power consumption is curtailed by 20% to 90%. Furthermore there is a tremendous improvement in the power delay product. Hence this technique can be used for high speed circuits. The circuit operates in subthreshold region which is suitable for applications that require extremely low power consumptions.

Future work will include the employment of the proposed technique on domino circuits operating in the subthreshold region. Domino logic offers high speed but the average power consumption of the domino circuits is higher than the static circuit. Hence the proposed technique will be applied on the domino circuit and its performance and power consumption will be evaluated. Comparisons will be made with their standard CMOS counterparts.

8. REFERENCES

[1] Hendrawan Soeleman and Kaushik Roy,"Ultra-Low Power Digital Subthreshold Logic Circuits," in International Symposium on Low Power Electronics and Design, 1999, pp. 94-96.

[2] Hendrawan Soleleman, Kaushik Roy and Bipul Paul, "Sub-Domino Logic: Ultra-Low Power Dynamic Sub-Threshold Digital Logic," in 14th International Conference on VLSI Design, 2001, pp. 211-214.

[3] Manan Sethi, Karna Sharma, Paanshul Dobriyal, Navya Rajput, Geetanjali Sharma ,"A Novel High Performance Dual Threshold Voltage Domino Logic Employing Stacked Transistors," International Journal of Computer Applications(0975-8887), vol. 77- No. 5, September 2013.

[4] M. Johnson, D. Somasekhar, L-Y Chiou and K. Roy , "Leakage Control with Efficient Use of Transistor Stacks in Single Threshold CMOS," IEEE Trans. VLSI Systems, vol. 10, 2002, pp. 1-5.

[5] Yu-Tzu Tsai, Hsiang-Hui Huang, Shang-Wei Hsu Ching-Hwa Chang, *Jiun-In Guo ,"A Low-Power VDD-Management Technique For High-Speed Domino Circuits," in International Symposium on VLSI Design, Automation and Test (VLSI-DAT), 2011, pp. 1-4.

[6] Arun.P, Ramasamy.S ,"A Low-Power Dual Threshold Voltage-Voltage Scaling Technique for Domino Logic Circuits," in Proc. ICCNT, 2012, pp. 1-6.

[7] K. Agarwal, H. Deogun, D. Sylvester, and K. Nowka , "Power gating with multiple sleep modes," in Proc. 7th International Symposium on Quality Electronic Design, March 2006, pp. 633– 637.

[8] T. Douseki, S. Mutoh, Y. Matsuya, T. Aoki, S. Shigematsu and J. Yamada,"1-V power supply high-speed digital circuit technology with multithreshold-voltage CMOS," IEEE Journal of Solid-State Circuits, pp. 847-854, 1995.

[9] Q. Wang, and S. Vrudhula,"Static power optimization of deep submicron CMOS circuits for dual Vt technology," Proceedings of ICCAD, pp. 490–496, April 1998.

[10] Karna Sharma, Manan Sethi, Paanshul Dobriyal, Geetanjali Sharma ,"Designing a Novel Power Efficient D-Flip Flop using Forced Stack Technique," International Journal of Computer Applications(0975-8887), vol. 68- No. 9, April 2013.