Strategies and Techniques for Optimizing Power in BIST: A Review

Amandeep Singh
Department of Electronics and Communication Engineering
Lovely Professional University
Punjab, India.

P. Mohan Kumar
Department of Electronics and Communication Engineering
Lovely Professional University
Punjab, India.

Mohinder Bassi
Department of Electronics and Communication Engineering
Lovely Professional University
Punjab, India.

ABSTRACT
Power dissipation is a challenging problem in current VLSI designs. In general the power consumption of device is more in the testing mode than in the normal system operation. Built in self test (BIST) and scan-based BIST are the techniques used for testing and detecting the faulty components in the VLSI circuit. Linear Feedback Shift Register (LFSR) in BIST generates pseudo-random patterns for detecting the faults, increasing the power consumption during testing, boosting the need to add power optimizations to BIST pattern generators. This paper identifies the different techniques to modify the BIST architecture thereby finding an optimal choice to reduce power consumption without compromising upon fault coverage.

General Terms
Power optimization, IP cores.

Keywords
BIST, scan based-BIST, LFSR, VLSI, fault coverage.

1. INTRODUCTION
Techniques used to reduce the power and energy problems during the testing activity have recently attracted research attention. System utilizes more power in test mode than in normal mode [4]. As in testing activity, Circuit under test (CUT) has more switching activities so a special care must be taken to ensure that the system is working between its rated limits. Increase in average power and peak power consumption subsequently increase the heat dissipation and reliability problem respectively.

The power dissipation can be classified as:

i) The static power dissipation, that is due to leakage current in transistors during steady state.

ii) The dynamic power dissipation, that is due to the switching activity.

Number of techniques have been proposed and used to reduce the dynamic power dissipation. These include test scheduling algorithms under power constraints; scan testing techniques, LFSR structure modifications, correlation driven advancements in BIST structure, low transition test pattern generator.

VLSI chips with low controllability and observability are tested by BIST. BIST techniques provides an ease of on-chip test pattern generations and response verifications, so they are used to test the VLSI designs that in turns eliminates the need of any external equipment to used for testing.

Using BIST for the testing has a few drawbacks as its architecture uses a linear feedback shift register (LFSR) for generating the pseudo random test patterns. One drawback is the introduction of more switching activities in the circuit under test (CUT) during the test mode than in the normal operation. This consumes more power while testing activity thereby resulting in delay penalty into the design. This switching activity is the main source of dynamic power dissipation in test mode given by equation:

$$P = 0.5V_{DD}^2E(sw)f_{clk}\,C_L$$

where V_{DD} is supply voltage, E(sw) is the average number of output transitions per $1/f_{clk}$, f_{clk} is the clock frequency and C_L is the physical capacitance at the output of the gate. From the above equation the dynamic power dissipation depends on: voltage supplied (V_{DD}), Clock frequency(f_{clk}) and Switching activity. Power optimization on the basis of first two parameters effects the circuit performance but power reduction using the switching activity keeps the fault coverage and performance same as in the original technique.

In this paper, the Section 2 includes the description of BIST architecture along with its constituent parts, in Section 3, some power optimization techniques will be discussed with the power reduction results, and then in Section 4 we will conclude the problem.

2. BIST ARCHITECTURE
A typical BIST architecture consists of a test pattern generator (TPG), usually implemented as a linear feedback shift register (LFSR), an output response analyzer (ORA), implemented as a multiple input signature register (MISR), and a BIST control unit (BCU) all implemented on single chip.

Different components of BIST architecture are:

i) Circuit under test (CUT): This part is the circuit that is to be tested in BIST mode. It can be a combinational circuit or a sequential circuit. Their primary output (PO) and primary input (PI) delimit it.

ii) Circuit under test (CUT): This part is the circuit that is to be tested in BIST mode. It can be a combinational circuit or a sequential circuit. Their primary output (PO) and primary input (PI) delimit it.

iii) Test Pattern Generator (TPG): It is a dedicated circuit for generating pseudo random test patterns or deterministic test patterns. The patterns generated by TPG are given to CUT for testing.

iv) Multiple input signature register (MISR): Signature register efficiently match different input streams with different signatures with a very less probability of alias. MISR is usually implemented in built in self test (BIST) designs, in which output responses are compressed by MISR.

v) BIST Controller unit (BCU): It manages TPG, ORA and reconfigures the CUT, thereby controlling the execution of test activity. It is activated by Normal/Test signal and generates a Go/ No go signal.

vi) Output response analyzer (ORA): It analyses the sequence on primary output (PO) and compares it with the expected value.

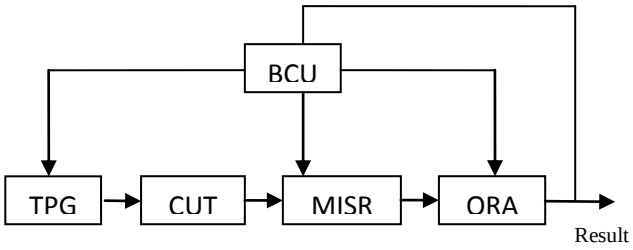

Figure 1: BIST Architecture

There are different architectural arrangements possible for the implementation of BIST using the above listed components. Different architectures consume different power even for same polynomial. It is very important to choose the proper test pattern generator for efficient fault coverage and performance.

3. POWER OPTIMIZATION TECHNIQUES

Various techniques and architectures have been proposed and presented in the literature to optimize the power consumption in BIST based architecture. These can broadly be classified into these categories:

a) System level scheduling and/or partitioning;
b) Correlation driven modifications of LFSR;
c) Power driven control of LFSR;
d) Switching activity control in LFSR.

Most of the techniques modify the structure of LFSR so as to reduce the switching transitions within the patterns and between the patterns generated by TPG. By controlling the number of transitions we are in turn controlling the switching activity which in turns helps in reducing the peak power and average power consumptions. In this section we will discuss different techniques adopted to reduce the power consumption in testing activity of BIST mode along with different Trade-offs.

required to test the two subcircuits is never greater than the test length for the original circuit [5].

3.3 Non-Uniform Cellular Automata for TPG

The technique proposed architecture for test pattern generator using Non Uniform Cellular Automata [7]. A polynomial time

3.1 Filtering Non-Detecting Vectors

A filtering technique is employed to filter out the vectors that are not detecting the faults. Filtering is performed by a combinational circuit named filter controlling the register located between LFSR and the CUT [12]. So filtering the unnecessary vectors reduces the power dissipation and circuit overhead. Simulation results in [12] shows that an average power has been reduced by 74.2% as tested on ISCAS'85 benchmark circuits.

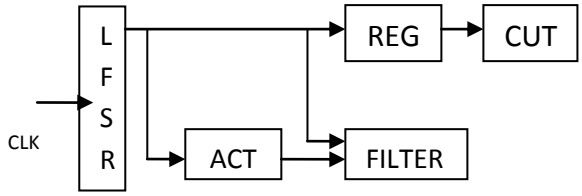

Figure 2: Filtering Non Detecting Vectors

The FILTER module is implemented with a combinational circuit. The ACT module includes a flip-flop to perform a self-disabling after the k vectors [12].

3.2 Circuit Partitioning

The technique proposed in [5] divides the main circuit into structural subcircuit so that each sub circuit can be tested by different BIST sessions [5]. Peak power dissipation and switching activity are reduced by partitioning the circuit into sub circuits. As the test length required to test sub circuit will be less than the test length for main circuit so the total power consumption for BIST reduces subsequently. ISCAS circuits showed average power reduction of up to 62 % and peak power reduction of 57 % [5].

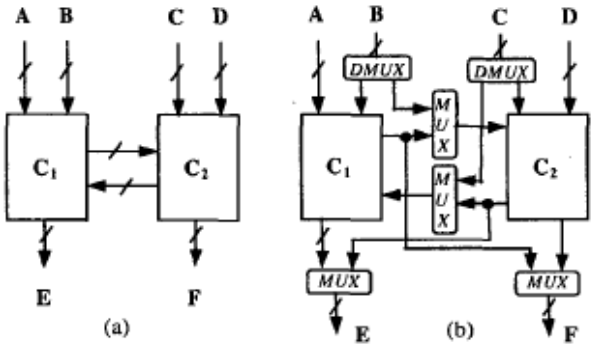

Figure 3: Circuit partitioning technique

In the proposed partitioning technique multiplexers and demultiplexers are inserted to get the embedded inputs and outputs of each subcircuit and connecting these embedded inputs and outputs to primary inputs and outputs that are not used by the subcircuits [5]. Instead of activating all nodes of the circuit as in the case of standard BIST, only one part of the circuit is activated for a given time interval. Moreover the total energy consumption is also reduced as the test length

algorithm has been designed in [7], that converts the test pattern generation problem into the combinational problem called Minimum Set Covering (MSC). The Solutions to this problem are nothing but the desired low power design topology for the test pattern sequence [7]. Non-Linear Hybrid Cellular Automata (NHCA) and Non Uniform Cellular Automata (NUCA) are efficient techniques for BIST-TPG design assuring 100% fault coverage in minimal test time [7].

Table below shows the comparative results for NHCA and NUCA designs. In the experiments, ISCAS benchmark data is used and the test vectors are obtained by using ATPG tool of cadence software [7]. Area Costs (AC) of the obtained designs are calculated by Synplify Pro FPGA logic synthesis tool, the target design being an Altera Stratix II FPGA [7]. Experimental results obtained in [7] are summarized in Table 1.

Table 1. Comparative results for NHCA nad NUCA

		Avg. PC per vector		TL		AC	
Circuit	n	NHCA	NUCA	NHCA	NUCA	NHCA	NUCA
C432	36	49.4	109.40	2000	83	36	865
C499	41	109.5	56.54	2000	68	41	340
C880	60	243.0	154.58	4000	67	60	876
C1908	33	466.6	145.70	8000	162	33	2035

3.4 Vector Inserted TPG

In the technique used in [3], n-stage LFSR is used as test pattern generator along with a control logic that makes the clock frequency of LFSR 1/m that of the original clock thereby lowering the transition density at the LFSR [3]. Thus (m-1) vectors are inserted between successive test patterns generated by the original LFSR, during the cycles when LFSR is unactuated. Genetic algorithm is used in [3] to locate the vectors to be inserted in LFSR.

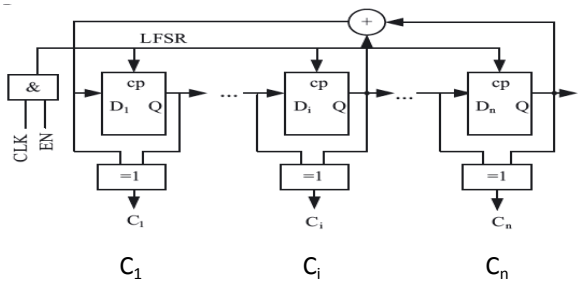

Figure 4: Logic for generating compare vector *C*

Compare vector is been made between the pseudo random vectors generated by original LFSR by adding some logic to the design then the vectors are been inserted between successive pseudo random patterns according to the specified bits of compare vector [3].

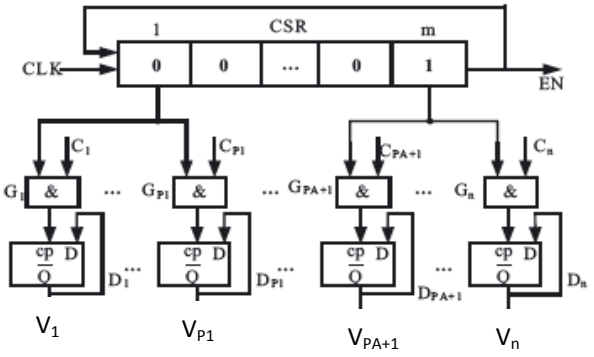

Figure 5: Structure of GA LP-TPG

The number of inserted vectors and bits change between successive patterns are obtained by using optimization based on genetic algorithm [3], to subsequently reduce the weighted switching activity (WSA) which in turns defines the total power consumption. Experimental results on ISCAS'85 Benchmark circuits showed 26% to 60% reduction in the number of the WSA_{peak} and up to 90% reduction in number of *WSA* and WSA_{avg} , without losing stuck-at fault coverage [3]. The only drawback of GA LP-TPG is the increased area overhead as compared with original LFSR [3]. ITPG proposed in [13] uses the same scheme with an addition of error detection and correction technique using viterbi decoder error detection and correction [13]. Genetic Algorithm Inserted Test Pattern Generator with Error Detection and Correction GAITPGEDC can highly reduce the weighted switching activity (WSA), during BIST application i.e. the average power and the peak power consumption are highly reduced [13]. The experimental results on ISCAS'85 Benchmark circuit and viterbi decoder for error detection and correction showed up 26% to 64% reduction in the number of WSAp without compromising on stuck-at fault coverage [13].

3.5 Seeds Optimization Technique

Seeds selection algorithm of Single Input Change (SIC) sequences based on Deterministic Automatic Test pattern Generation (ATPG) test patterns is proposed to reduce the test power consumption and test application time with high test fault coverage [22]. Low power Deterministic BIST demands the optimal selection of SIC seeds for a reliable and successful design. The figure below shows the generation of Random Single Input Change Test Patterns and a code transition circuit is been inserted between pseudo random ATPG and Circuit Under Test (CUT). Experimental results on ISCAS'85 Benchmarks showed that with proper selection of SIC seeds, the proposed scheme [22] can subsequently reduce the power consumption and application time in test mode.

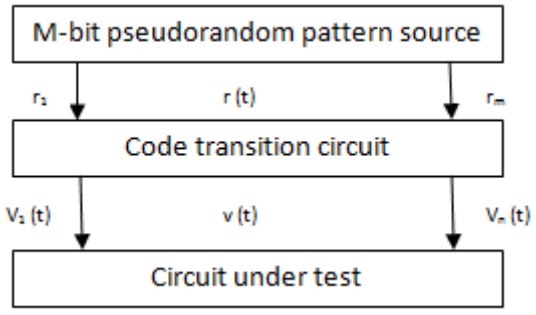

Figure 6: Generation principle of Random SIC test Sequences

3.6 Maximum Bipartite Matching

A new technique has been proposed in [16], for test pattern generation called Low-Transition Generalized Linear Feedback Shift Register (LT-GLFSR) which combines the bipartite (half fixed) and bit insertion (either 0 or 1) techniques [16]. A similar technique has been presented in [21], Gray code generators are used as a low power BIST solution. In this, the test application time is reduced by switching between different gray sequences during the application of test set [21]. The proposed architecture [16] consists of GLFSR and intermediate patterns insertion technique (Bipartite and bit insertion technique) that can be implemented by modified clock scheme codes generated by

Finite State Machine (FSM). The proposed technique not only controls the switching activity between the consecutive patterns (Hamming Distance) but also within the adjacent bits of same pattern i.e. within two consecutive patterns (bit insertion) and between individual patterns (bit swapping). The intermediate patterns inserted by bipartite and bit insertion technique takes minimal time to achieve desired fault coverage. The randomness of the patterns generated by LT-GLFSR is better than LFSR and GLFSR [16].

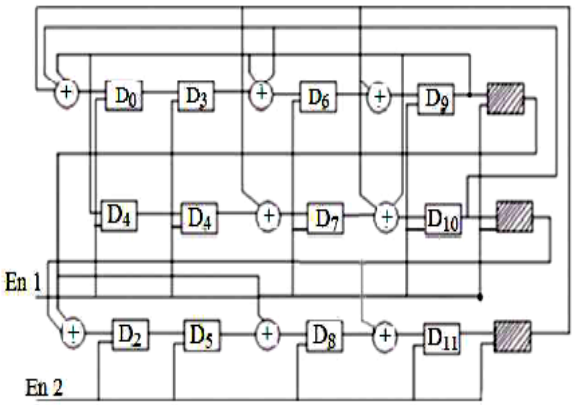

Figure 7: LT-GLFSR Architecture with Bipartite Technique

Experimental results in [16] as tested on ISCAS'85 benchmark circuits S298 and S526 are summed up in Table 2.

Table 2. Transition fault detected in S298

Pattern generation	Number of test pattern	Pattern reduction (%)	Power (mW)
LFSR	53	--	45.56
GLFSR	17	32.09	25.98
LT-GLFSR (Bipartite)	12	22.67	21.23
LT-GLFSR (Bipartite and Bit insertion)	8	15.09	18.23

3.7 Bit Swapping LFSR

Bit swapping LFSR is a modification done to the pseudo random test pattern generator to reduce the transition between the patterns generated. The LT-RTPG so formed reduces the switching activity during BIST by reducing the transitions at scan inputs during scan shift operations. The scheme proposed in [18], called Bit swapping LFSR uses an LFSR and a 2*1 multiplexer.

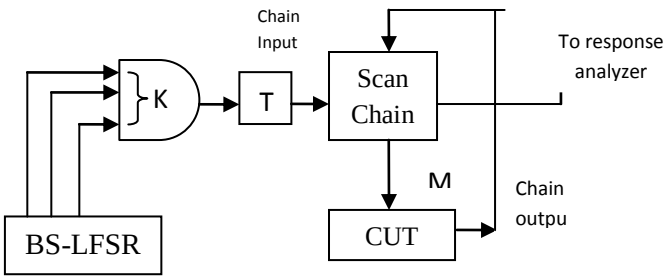

Figure 8: Low Transition RTPG

The proposed LT-RTPG significantly reduced the average and peak power consumption by 65% and 55% respectively when tested on ISCAS'89 benchmark circuit [18].

4. CONCLUSION

Different techniques for implementing BIST for testing various VLSI circuits have been discussed. Design of Test Pattern Generator (TPG) is the most important part in BIST as the pattern generation governs the test length and switching activity, which in turns effects the power consumption in test mode. If we can control this switching activity, we can subsequently reduce the power/energy consumption in testing activity. In Low Transition design of TPG, wherein we are controlling the transitions within the adjacent bits of test pattern and between the different generated patterns, better reduction in peak power and average power consumption can be achieved with no compromise on fault coverage.

5. FUTURE SCOPE

Low power is becoming the key research area in today's electronics industry. As stated earlier, for VLSI circuits, the power consumption is more in test mode than in normal mode of operation. So designing a Low Transition Low Power BIST for testing activity eliminates the need of external equipment for testing and reduces the power dissipation in test mode. Different techniques from literature can be tried to get a novel BIST design that can be used to test any circuit within its rated limits, providing better fault coverage and minimum peak power and average power consumption.

6. REFERENCES

[1] Bellos Maciej, Bakalis Dimitris and Nikolos Dimitris, "Scan Cell Ordering for Low power BIST" in Proceedings of the IEEE Computer Society Annual Symposium on VLSI Emerging Trends in VLSI Systems Design, 2004.

[2] Cao Bei, Xiao Liyi and Wang Yongsheng, "A Low Power Deterministic Test Pattern Generator for BIST Based on Cellular Automata" in *4th IEEE International Symposium on Electronic Design, Test & Applications*, pp. 266-268, 2008.

[3] Enmin Tan, Shengdong Song and Wenkang Shi, "Power Reduction in BIST Design Based on Genetic Algorithm and Vector-Inserted TPG" in *The Eighth International Conference on Electronic Measurement and Instruments*, pp. 533-537,2007.

[4] Ghosh Debjyoti, Bhunia Swarup and Roy Kaushik, "A Technique to Reduce Power and Test Application Time in BIST", in *Proceedings of the 10th IEEE International On-Line Testing Symposium (IOLTS'04),*2004.

[5] Girard P., Guiller L., Landrault C. and Pravossoudovitch S., "Low Power BIST Design by Hypergraph Partitioning: Methodology and Architectures" in *ITC International Test Conference*, pp. 652-661, 2000.

[6] Girard P., Guiller L., Landrault C. and Pravossoudovitch S., "An Adjacency-Based Test Pattern Generator for Low Power BIST Design", *IEEE*, pp. 459-464, 2000.

[7] Kilic Hurevren and Oktem Levent, "Low-Power Test Pattern Generator Design for BIST via Non Uniform Cellular Automata" in *IEEE*, pp. 212-215, 2005.

[8] undu S. and Chattopadhyay S., "Embedding a Low Power Test Set for Deterministic BIST using a Gray

Counter", in *Proceedings of the World Congress on Engineering*, Vol II, July 6-8, WCE-2011.

[9] Lai Nan-Cheng, Wang Sying-Jyan and Fu Yu-Hsuan, "Low Power BIST with Smoother and Scan-Chain Reorder" in *Asian Test Symposium*, 2004.

[10] Lee Jinkyu and Touba Nur A., "Low Power BIST Based on Scan Partitioning", in *International Symposium on Defect and Fault Tolerance in VLSI Systems*, IEEE 2005.

[11] Li Ji, Han Yinhe, Li Xiaowei, "Deterministic and Low Power BIST Based on Scan Slice Overlapping", *IEEE*, pp. 5670-5673, 2005.

[12] Manich S., Gabarro A., Lopez M., Figueras J., Girard P., Guiller L., Landrault C., Pravossoudovitch S., Teixeira P. and Santos M., "Low Power BIST by filtering Non-Detecting Vectors," in Proc. *European Test Workshop (ETW'99)*, pp. 165-170, 1999.

[13] M. Banu Fahmitha and N. Poornima, " BIST using genetic algorithm for error detection and correction" in *IEEE- International Conference on Advances In Engineering , Science and Management (ICAESM-2012)*, pp. 588-592,March 30,31,2012.

[14] Nayineni Prathyusha and Masthan S.K, "Power optimization of BIST circuit using low power LFSR" in *International Journal of Computer Trends and Technology*, vol 2 Issue 2,pp. 5-8, 2011.

[15] Nemati Nastaran, Simjour Amirhossein, Ghofrani Amirali and Navabi Zainalabedin, "Optimizing Parametric BIST Using Bio-inspired Computing Algorithms", in *24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 268-276, 2009.

[16] P. Sakthivel, NirmalKumar A. and Mayilsamy T., "Low Transition Test Pattern Generator Architecture for Built-in-Self-Test" in *American Journal of Applied Sciences*, pp. 1396-1406,2012.

[17] Parashar Umesh, "Improved Low Power Full Scan BIST", *IEEE*, pp. 1103-1106, 2007.

[18] Reddy C.Ravishankar, Zilani Shaik and Sumalatha V., "Low Power, Low Transition Random Pattern Generator" in *International Journal of Engineering Research and Technology (IJERT)*, Vol 1 Issue 5, pp. 1-6, July-2012.

[19] Sato Yasuo, Wang Senling, Kato Takaaki, Miyase Kohei and Kajihara Seiji," Low Power BIST for Scan-Shift and Capture Power" in *IEEE 21st Asian Test Symposium*, pp. 173-178, 2012.

[20] Tan Enmin and Wang Li, "A BIST design with Low Power Consumption Based on Genetic Algorithm" in *The Ninth International Conference on Electronic Measurement and Instruments*, pp. 2-526 - 2-529, ICEMI'2009.

[21] Voyiatzis I., Axiotis K., Papaspyrou N., Antonopoulou H. and Efstathiou C., "Test Set Embedding Into Low-power BIST Sequences using Maximum Bipartite Matching", in *16th Pan-Hellenic Conference on Informatics*, pp. 74-79, 2012.

[22] Xiao Liyi, Cao Bei, and Wang Yongsheng, "Seeds Optimization Algorithm of SIC Test sequences in Low Power BIST" in *IEEE*, 2010.

[23] Zhang Xiaodong, Shan Wenlei and Roy Kaushik, " Low-Power Weighted Random Pattern Testing", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 19, No. 11, November 2000.