

New Protocol of Aggressive Packet Combining Scheme

Yaka Bulu

Department of Electronics &
Communication Engineering,
National Institute of Technology
Yupia
Arunachal Pradesh

Swarnendu K

Chakraborty
Department of Computer
Science & Engineering,
National Institute of Technology
Yupia
Arunachal Pradesh

Chandan T Bhunia

Department of Computer
Science & Engineering,
National Institute of Technology
Yupia
Arunachal Pradesh

ABSTRACT

Aggressive Packet Combining (APC) scheme is well established for receiving correct packet in high error prone wireless link. In APC three copies of a packet are transmitted and receiver does bit wise majority decision to get the correct copy. The main research challenge in APC is that if two or more copies of the packet become erroneous at the particular bit location then majority logic fails to correct the error. In this paper we propose a new method of correction in APC which will address the limitation which occurs in conventional APC.

General Terms

Error correction capability

Keywords

Packet combining Scheme, Conventional Aggressive Packet Combining (CAPC) scheme

1. INTRODUCTION

In order to combat errors in computer/ data communication networks, ARQ (Automatic Repeat Request) techniques [1-5] with various modifications as applicable to in various communications environments are used. Leung [7] proposed an idea of Aggressive Packet Combining scheme (APC) for error control in wireless networks with the basic objective of fast error control in relatively higher noisy wireless networks. APC is well established and studied elsewhere [3-10]. Several modifications of APC are also reported elsewhere [2-8]. The modifications are due to increasing throughput, tackling various error syndromes and enhancing fast correction. In APC and/ or modified APCs, two or more copies of the packets are transmitted. Copies received by the receiver either error free or erroneous are used in receiver to correct errors by applying Packet Combining schemes differently in different situations. However in original APC, if an error occurs at same locations of erroneous packets, the application of the majority logic as in original APC fails to correct the error. To address the stated problem of APC we propose a new protocol of APC. Analytical results establish that the proposed new scheme provide better correction capability.

2. REVIEW OF PACKET COMBINING SCHEME (PC)

Chakraborty [11] suggested a simple technique where the receiver will correct limited error, one or two bit error, from the received erroneous copies. The technique proposed by Chakraborty is illustrated below:

We assume the original transmitted packet as “01010101.”

The packet erroneously received by the receiver as “11010101.” The receiver requests for retransmission of the received erroneous packet but keeps in store the received erroneous packet. The transmitter retransmits the packet, but

again the packet is received by the receiver erroneously as “00010101.” Chakraborty proposed that the receiver can correct the error by using two erroneous copies for a bit wise XOR operation between erroneous copies may be performed to locate the error position, in the present example being as follows:

First erroneous copy	11010101
Second erroneous copy	00010101

XOR	11000000

The error locations are identified as first and/or second bit from the left. Chakraborty suggested that the receiver can apply brute method to correct error by changing received “1” to “0” or vice versa on the received copies followed the application of error decoding method in use. In the example the average number of brute application will be 0.5, and in general 2^{n-1} if n bits are found in error. Several modifications of PC have been studied elsewhere [12-13] by Bhunia's.

3. REVIEW OF CONVENTIONAL APC

Aggressive Packet Combining scheme is a modification of MjPc (Majority Packet Combining) [14]. To illustrate APC it is assumed that an original packet 10101010 is transmitted between a sender and a receiver. In Aggressive Packet Combining (APC) the three copies of packet are sent for each packet between a source and a destination. The Majority logic is applied bit to bit on three copies of the packet. In table: I we have shown different possibilities of APC. In case (1) there is no error in the transmitted three copies. In case (2) receiver receives two copies of correct packet and one copy with an error, so correction is possible by majority logic. In case (3) and case (4) errors are present in two or more copies in which case correction is not possible.

Table:I: Different cases of APC Scheme

Case 1	Case 2	Case 3	Case 4
Copy-1= 10101010	Copy-1= 00101010	Copy-1= 00101010	Copy-1= 00101010
Copy-2= 10101010	Copy-2= 10101010	Copy-2= 00101010	Copy-2= 00101010
Copy-3= 10101010	Copy-3= 1010110	Copy-3= 10101010	Copy-3= 00101010
Correction Probability is (1-P ₃)	Correction Probability is (1-P ₂)P	Correction Probability is (1-P) ₂	Correction Probability is P ₃
Correction not required	Correction possible	Correction not possible	Correction not possible

4. NEW BASIC IDEA

In this new technique, instead of sending three packets of the original packets as in conventional APC, two packets are sent. If the received two packets are erroneous then XORing of both the erroneous packets are done to locate the error positions. Now receiver sends negative acknowledgement with erroneous bit positions information to the sender and also keeping the copies that has been received erroneously. And instead of retransmitting the whole packets sender sends only the erroneous bit positions by repeating each bit three times so even if the third received packets are erroneous the receiver by using majority logic with three successive bits get the original bits that have been transmitted and erroneous locations are corrected by comparing the bits obtained after majority logic with the erroneous bit locations in the first two received packets. Thus in this technique both horizontal and vertical checking of the received packets are done. This idea will become clearer by the following examples.

Examples:

I. Original packet-11001100

1 st erroneous packet-	110 1 1100
2 nd erroneous packet-	1 0101100

XOR	01110000

The error locations are identified as 5th, 6th and 7th bit locations from the right. Now sender sends only the erroneous bits by repeating each bit three times.

The third packet sent is 111 000 000 and again if it is received erroneously like 101 001 000 but by majority logic we can get the original string that has been sent like 101-1 (7th), 001-0 (6th), 000-0 (5th). Comparing third packet with the first erroneous packet, the 5th bit in the first erroneous packet is **1** but the actual bit is **0** so the first corrected packet is 11001100. Now comparing the second erroneous copy with the third packet, the 6th and 7th bits from right of the second packet shown in bold 1 and 0 respectively but the actual bits are 0 and 1 respectively so the 6th and 7th positions are corrected as 0 and 1 from the right. So the corrected packet is 11001100.

II. Original packet-10110100

1 st erroneous packet-	0 0110100
2 nd erroneous packet-	1 0010100

XOR	10100000

The error locations are identified as the 6th and the 8th locations from the right. After getting negative acknowledgement sender sends the 3rd packet as 111 111 and if it is received without error then by majority logic the 6th and 8th bits are 111-1, 111-1 respectively. Comparing third packet with the first erroneous packet, the 8th bit from the right in the first erroneous packet is **0** but the actual bit is **1** so the first corrected packet is 10110100.

Now comparing the second erroneous copy with the third packet, the 6th bit from right of the second packet shown in bold is 0 but the actual bit is 1 so the corrected packet is 10110100.

III. Original packet-01101001

1 st erroneous packet-	01 0 01101
2 nd erroneous packet-	011 0 0101

XOR	00101000

The error locations are identified as the 4th and the 6th locations from the right. After getting negative acknowledgement sender sends the 3rd packet as 111 111 and if it is received with an error then by majority logic the 4th and the 6th bits are 101-1 011-1 respectively. Comparing third packet with the first erroneous packet, the 6th bit from the right in the first erroneous packet is **0** but the actual bit is **1** so the first corrected packet is 01101001.

Now comparing the second erroneous copy with the third packet, the 4th bit from right of the second packet shown in bold is 0 but the actual bit is 1 so the corrected packet is 01101001.

IV. Original packet-11110000

1 st erroneous packet-	1 0110000
2 nd erroneous packet-	0 1110010

XOR	11000010

The error locations are identified as the 2nd, 7th and the 8th locations from the right. After getting negative acknowledgement sender sends the 3rd packet as 111111000 and if it is received with an error as 111 101 001 then by majority logic the 2nd, 7th and the 8th bits are 111-1 101-1 001-0 respectively. Comparing third packet with the first erroneous packet, the 7th bit from the right in the first erroneous packet is **0** but the actual bit is **1** so the first corrected packet is 11110000.

Now comparing the second erroneous copy with the third packet, the 2nd and the 8th bits from right of the second packet shown in bold are 1 and 0 respectively but the actual bits are 0 and 1 so the corrected packet is 11110000.

5. MATHEMATICAL COMPARISON OF CONVENTIONAL APC AND NEW PROPOSED SCHEME

In conventional APC original packets are sent three times at a time so in APC n=3 and the probability that a packet is in error for conventional APC is given by:

$$P_{eC} = [1-(1-\alpha)^n] * [1-(1-\alpha)^n] * [1-(1-\alpha)^n]$$

$$P_{eC} = [1-(1-\alpha)^n]^3 \text{ ----- (1)}$$

Where α is bit error rate (BER) and N is the number of bits in a packet.

In our proposed scheme instead of sending three packets, two packets are sent and if the packets are received erroneous then by XORing operation erroneous bit positions are found. And in the 3rd packet sender sends the bits which are in error by repeating each bit three times but not the whole packet. At the receiver side receiver performs majority logic of the received packets and starts horizontal checking starting from LSB bit.

In this scheme the probability that a packet is in error (P_{eN}) is given by

$$P_{eN} = [1 - (1 - \alpha)^n]^2 * [1 - (1 - \alpha^3)^n] \quad \text{-----(2)}$$

By using this new technique correction capability of APC increases more than that of the conventional APC.

6. SIMULATION RESULTS

Curves (Fig. 1 to 4) have been plotted for probability of packets in error for various values of n for conventional APC (P_{eC}) and new proposed scheme (P_{eN}) and various values of bit error rate (α) from 10^{-4} to 10^{-1} . We measure the performance in terms of error correction capability.

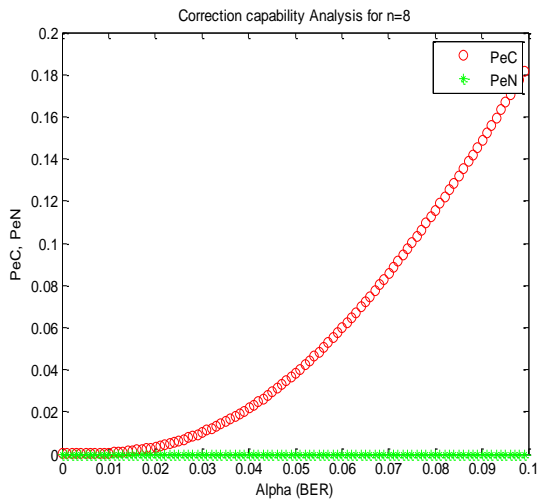


Fig.1 for n=8

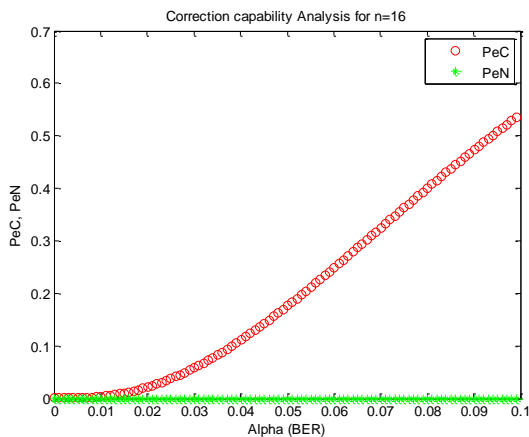


Fig. 2 for n=16

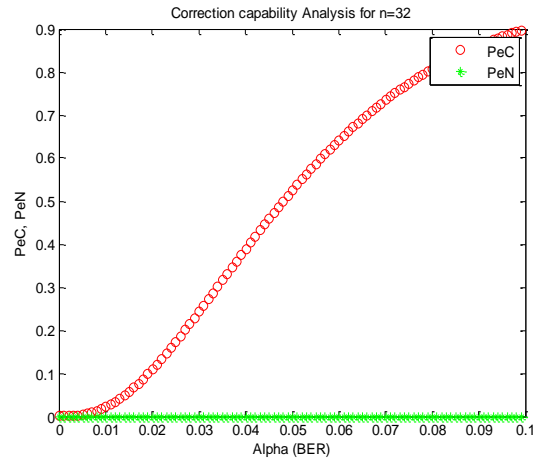


Fig. 3 for n=32

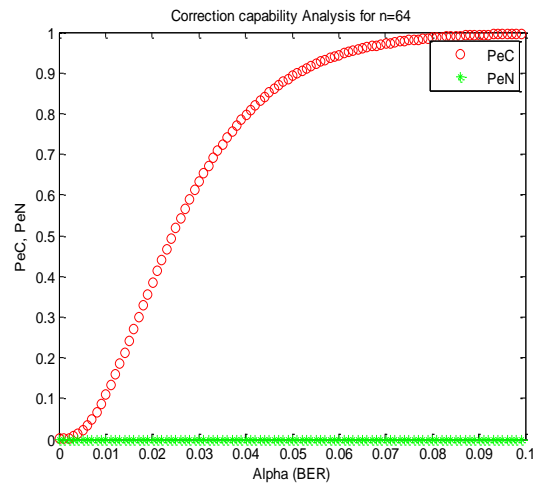


Fig.4 for n=64

7. CONCLUSIONS

In this paper, a new scheme of APC is proposed and studied. The new proposed scheme provides better correction capability than the conventional APC as observed from the results. Correction capability of this proposed scheme increases: (a) with increase in n (number of bits in packet), (b) with increase in bit error rate (α) as observed from simulation results.

Thus the performance of this scheme is superior than the conventional APC.

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