Architectures and Methodologies for Reducing Power in Multipliers: A Literature Survey

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ABSTRACT
Multiplier is the most basic unit of any electronic hardware whether it is microprocessor in cell phone or any DSP's processors for signal processing. So power dissipation by multiplier is the most important parameter which is needed to be taken care of. So a lot of researches have been made till now and lot of efforts has been made to decrease the power consumption of this basic unit. From last few years number of promising technologies came into existence which had opted by electronic industries to reduce the power consumption of whole system so the battery backup can be increased and less energy will be wasted for different computations. The most dominant technology in VLSI till now is cmos. The static power dissipation is due to leakage current and the dynamic power dissipation is due to switching transient current as well as charging and discharging of load capacitance. Power of any multiplier can be reduced by simply designing a full adder which will consumes very less power [8]. Number of techniques arrives in past researches to reduce the power consumption of multipliers. Reversible computing gives new direction to low power VLSI and important Reversible gates are mentioned in this paper. Various different architecture of multiplier using reversible gates for reducing power is discussed.

General term
Power dissipation, Reversible computing and reversible gates

Keywords
CMOS, VLSI, DSP, Dynamic power

1. INTRODUCTION
As, multiplier is very basic block which is used in almost all computing machines, the different architectures can be seen in literature which can reduce the number of computations and can also increase its speed. Due to tremendous development in computing machine the transistor density is increasing day by day and power dissipation by these CMOS circuit is becoming major problem these days. So researchers feel that CMOS technology will reach their limits in near future. Reversible computing gives new hope to researchers to improve their design in era of low power VLSI. Several researches have been made in this era and various new architectures of multipliers using reversible gates can be seen in literature. The rest of the paper is organized as follows. Section 2 explains the techniques for reducing the computations. In Section 3 an overview of reversible computing is given. In section 4 and section 5 architecture of multiplier using reversible gate and Vedic multiplier using reversible gates are discussed. Finally section 6 concludes the paper.

2. TECHNIQUES FOR LOWERING COMPUTATION
There are number of techniques for lowering the computations and various architectures was suggested in literature. It is quite obvious that lesser the number of computations lesser will be the power consumed by multiplier. Row bypassing, Column bypassing and Row and column both bypassing multipliers plays an important role for decreasing the number of computations.

2.1 Row bypassing multiplier
In these Row bypassing multiplier schemes the unnecessary computation is removed from the circuit by signal bypassing. When two unsigned numbers are multiplied, the multiplicand A = an-1 an-2, . . .,a0 and the multiplier B = bn-1 bn-2, . . . , b0, the product P = P2n- 1,P2n-2, . . . , P0, can be represented as the following equation [15]:

$$P=P0P1\ldots\ldots P2n\text{-}1=\sum_{i=0}^{n-1}\sum_{j=0}^{n-1}(a_i b_j)2^{i+j}$$

In the row bypassing scheme the 0's bit in the multiplier i.e B will lead to bypass the whole row in the multiplicand i.e A. The Row bypassing scheme disables the operation in some rows in order to save switching power consumption. To understand the row bypassing technique, let take an example of an unsigned 4×4 multiplication. In fig 2.1(a), if bit bj is 0, all product in row j (AiBj for 0 < i < n-1) are 0. As a result, the addition in corresponding row can be bypassed. For example, let b1 of fig 2.1(a) be 0. In this case, the output from the first row can be fed directly to the third row and the second row is disabled, thus the power dissipation can be reducing the switching activity.

$a_3\ a_2\ a_1\ a_0$ Input

X $b_3\ b_2\ b_1\ b_0$

$a_3b_0\ a_2b_0\ a_1b_0\ a_0b_0$

$a_3b_1\ a_2b_1\ a_1b_1\ a_0b_1$ Partial products

$a_3b_2\ a_2b_2\ a_1b_2\ a_0b_2$

$a_3b_3\ a_2b_3\ a_1b_3\ a_0b_3$

$p_7\ p_6\ p_5\ p_4\ p_3\ p_2\ p_1\ p_0$ Result

Fig 2.1(a)

In [12] an enhanced row by passing technique is used to reduce power dissipation by implement the multiplexing mechanism clock CMOS (C^2MOS) circuitry. Two different versions were provided, one emphasizing on low power and other focussing reduced circuit complexity. The circuit

overheads of both designs are confined to 23.4% and 12.8%, respectively. The power saved using this design is up to 17%.The design of enhanced row by passing multiplier is shown in fig 2.1(b)[12] for achieving low power dissipation. The comparison of Power consumption saving [12] of 8*8 Bypassing scheme multiplier is given in table 2.1(c) as per the design.

Table 2.1(c) Comparison of power consumption saving [12]

0.35µm	1.5v	1.6v	1.8v	2.0v	2.2v	2.5v
Design-1	-0.2%	2.5%	4.2%	9.2%	9.7%	8.9%
Design-2	-0.6%	2.0%	3.6%	8.2%	7.5%	5.0%

2.2 Column bypassing technique

In this technique, if the corresponding bit in the multiplicand is 0, the operations in a column can be disabled. There are two advantages of this technique. First, it eliminates the extra correcting circuit. Second, the modified FA (full adder) is simpler than that used in the row-bypassing multiplier [5].

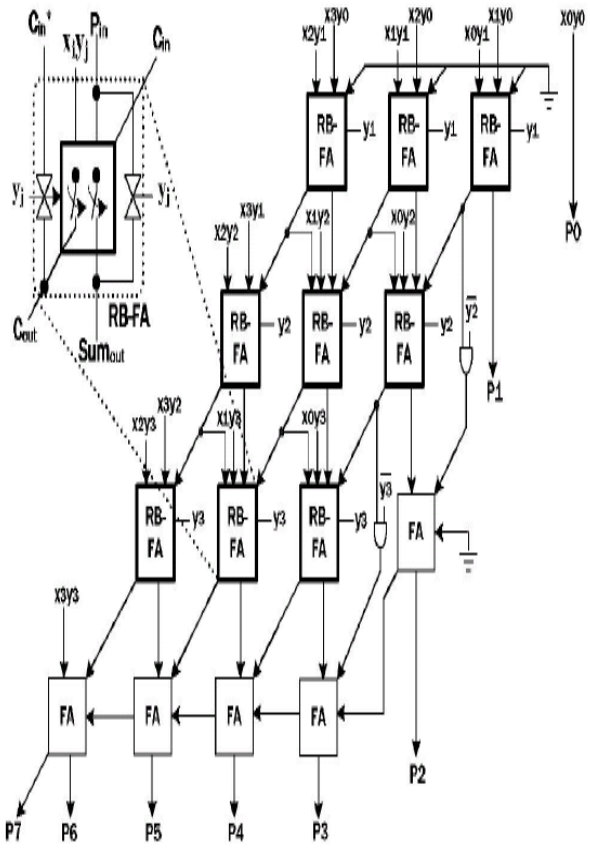


Fig 2.1(b) Architecture of parallel multiplier based on enhanced row by passing [12]

In this technique instead of bypassing the rows of full adder, columns of full adder are bypassed. In this more number of zeros are inserted in multiplicand which will decrease the switching activity. When a_j=0, the output of a column j adder cell $FA_{i,j}$ will be such that output carry bit is 0 and the output sum bit is equal to the output sum bit of $FA_{i-1,\ j+1}$.

In [8] the power consumption achieved is very less as compared to braun's multipier as shown in table 2.2(a) and later on the power was reduced more in [12].

Table 2.2(a) Power (mW) consumption

Multiplier type	Size					
	4*4	%	8*8	%	16*16	%
[8]	0.4298	99.4	2.25	97.4	7.15	89.3
Braun	0.4325	100	2.31	100	8.01	100

2.3 Row and column bypassing technique

In row and column bypassing technique instead of full adder some simplifications of half adder and full adder was done using which low power consumption is achieved. In [15] an adder cell was proposed which is shown in fig 2.3(a). Both the 0's in rows and columns taken care of so that computations can be reduced. Mux plays an important role here as it will bypass the rows and column when 0's exist.

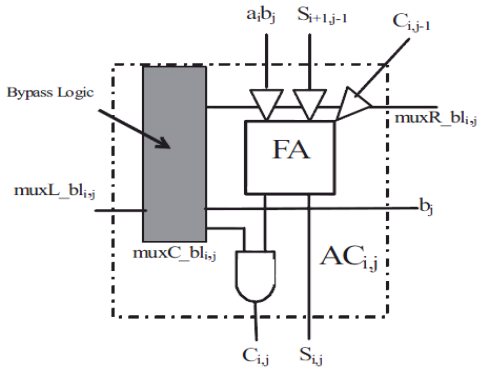


Fig 2.3(a) Adder cell

Power dissipation in this multiplier was very less as compared to other designs of array multipliers. The power dissipation in the proposed N*N Braun multiplier (mw) is shown in table 2.3(b).

Table 2.3(b)

Design	4*4 multiplier	8*8 multiplier	16*16 multiplier
(8)	.67(91.8%)	3.35(91.5%)	14.78(91.6%)
(15)	.54(74.0%)	2.79(76.2%)	11.73(72.7%)

So the row and column bypassing technique was able to achieve the lowest power consumption as by applying logic and by reducing mathematical calculations and by decreasing logic gates.

3. REVERSIBLE COMPUTING

Reversible computing is an upcoming technology and will be in demand in future in vlsi market. As the increase in clock frequency to achieve greater speed and increase in number of transistors packed onto a chip to achieve complexity of a conventional system results in increased power consumption. In the today's world almost all computers are made up of gates which are logically irreversible. Reversible gates have huge scope in future due it's less power dissipation characteristics. It has been proved that Boolean functions can be implemented using reversible gates. In the conventional gates every time when logical operations are performed the information about the input will be erased and dissipated as heat. Recently several researchers have focussed on the design and synthesis of reversible circuits. Reversible implementation can also be seen in thermodynamics and adiabatic cmos[20]. According to launder's principle the loss of single bit will lead to the dissipation of $KTln_2$ energy Where K is boltzmann's constant and T is, temperature of system. With the reversible computations one can achieve higher speed and high densities.

According to Moore's law the heat generated increases exponential as the bit or information is lost and in the coming decade this heat dissipation will get increased to intolerable amount. So, the only solution is to use that technology which brings revolution and will dramatically reduce heat dissipation and power consumption and that promising technology is reversible technology.

3.1 Reversible gates

To design the reversible circuits there is need of reversible gates. Till now number of reversible gates has been designed, but there are some important restrictions to make reversible circuit's i.e.

(a) Fan out is not permitted

(b) Loops are not permitted

Reversible gates are K input, K output gates in which each input pattern maps into unique output pattern. The term garbage output is the most important term in synthesis of reversible logic gates. A single output function of n variables will require at least n-1 garbage outputs, since the reversibility necessitates an equal number of outputs and inputs. Reversible logic imposes many design constraints that need to be either ensured or optimized for implementing any particular Boolean functions [22]. The most important reversible gates used for reversible logic synthesis are Feynman Gate, New Gate and Fredkin gate, Toffoli gate, Vnot gate [18]

3.1.1 Toffoli gate (VNOT Gate)

Toffoli gate is a reversible gate which is having quantum cost of 5. Input vector is I (A, B, C) and output vector is given as O (P, Q, R). The output for this gate is given as P=A, Q=B and R= (AB xor c) as shown in fig 3.1.1 (a) [18].

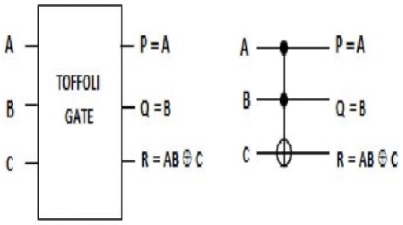
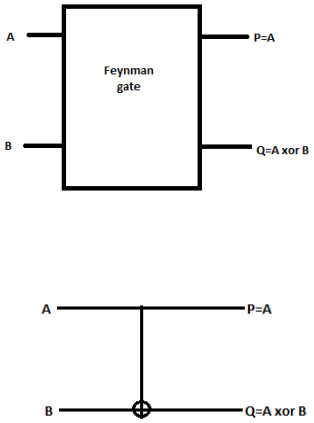


Fig 3.1.1(a) Toffoli Gate

3.1.2 Feynman gate

It is 2*2 reversible gate. The input vector is I (A, B) and the output vector is O (P, Q). The outputs are defined by P=A, Q=A xor B. Quantum cost of this gate is 1.This is very important gate as the fan out is not allowed in reversible logic so this gate can overcome this problem and is used as copying gate. This gate is shown in fig 3.1.2 (a).



3.1.2 (a) Feynman gate

3.1.3 Double Feynman Gate (F2G)

It is 3*3 gate. Input vector is I (A, B, C) and output vector is given as O (P, Q, R). Outputs are given by P=A Q= A xor B., R= A xor C as shown in fig 3.1.3(a) [18].

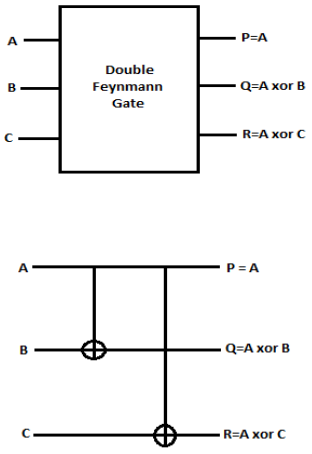


Fig 3.1.3 (a) Double Feynman gate

3.1.4 Fredkin gate

It is 3*3 reversible gate. The input vector is I(A,B,C) and the output vector is O (P,Q,R). The outputs are defined by P=A, Q=$\bar{A}$B xor AC, R=$\bar{A}$C xor AB. Its quantum cost is 5. This gate is as shown in fig 3.1.4(a) [18].

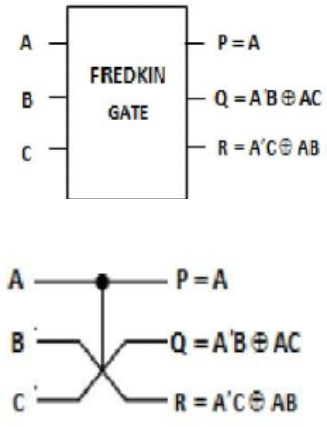


Fig 3.1.4 (a) Fredkin Gate

3.1.5 Peres Gate

Fig 3.1.5 (a) shows the Peres gate. It is 3*3 reversible gates. The input vector is I (A, B, C) and the output vector is O (P, Q, and R). The output t is given by P= A, Q= A xor B, R= A.B xor C. Quantum cost of this gate is 4.

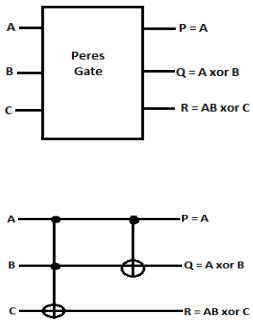


Fig 3.1.5 (a) Peres Gate

3.1.6 TSG Gate

It is 4*4 reversible gate. The input vector is I(A,B,C,D) and the output vector is O (P,Q,R,S). The output t is given by as shown in fig 3.1.6 (a)[18].

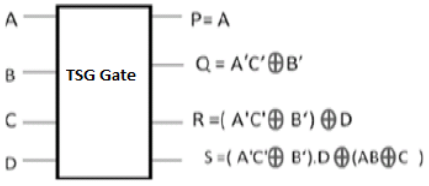


Fig 3.1.6 (a) TSG Gate

In fig 3.1.6 (b) TSG gate working as reversible full adder is shown.

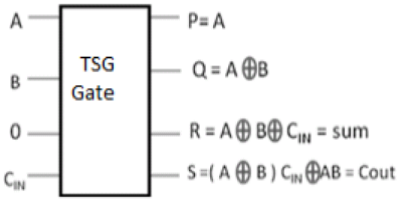


Fig 3.1.6 (b) TSG gate as reversible full adder

4. MULTIPLIER USING REVERSIBLE GATES

The important property of reversible gates is the information is never lost and dissipates very less heat. So it is very much in demand in recent days in VLSI. As these technology is very much aware about power dissipation. Various applications of reversible computing can be seen in quantum computers which consists of quantum logic gates having qubits and with each qubits information is associated corresponding to the classical bit value i.e. 0 or 1. After the research of TSG reversible gate various new architecture of low power multiplier was given and the design of novel reversible multiplier was shown in paper [10]. In this paper firstly partial generation of product terms are formed using fredkin gate as shown in fig 4(a) [10]

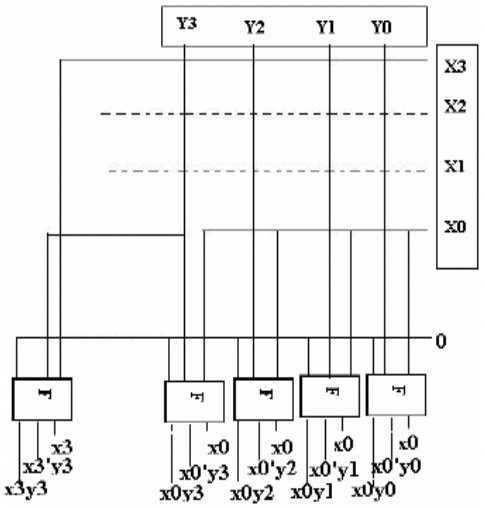


Fig 4 (a) Partial Product generation using Fredkin gate

In the above architecture the partial product which is generated is given to TSG gate as its inputs and TSG as full adder is used to give the output of multiplier. The architecture for this multiplier is given in fig 4(b) [10]. This architecture of reversible adder requires total of N*(N-1) reversible full adder cell where N is number of bits. The propagation delay of this multiplier is given as d+N*d' $[Log_2N]$ where d and d' are the propagation delays of a Fredkin gate and reversible TSG gate (adder) respectively. In this proposed reversible multiplier total of 29 reversible gates are used. But there was no improvement in garbage output. It was still poor for this kind of multiplier.

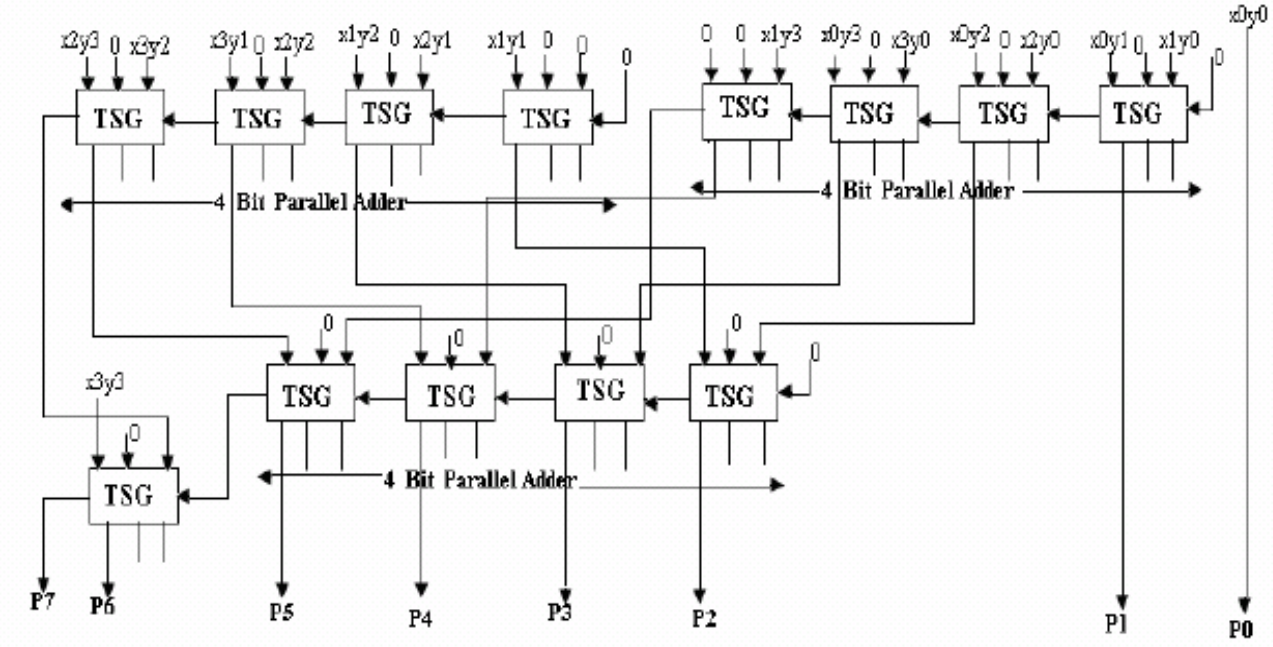


Fig 4 (b) Proposed 4*4 Novel Reversible Multiplier

5. VEDIC MATHEMATIC APPROACH

Number of architecture has been proposed using reversible gates for low power multiplier. After TSG gate, the HNG reversible gate came into existence which has quantum cost of 6 and also act as full adder alone and till now it is efficient reversible full adder as shown in fig 5 (a) [28].

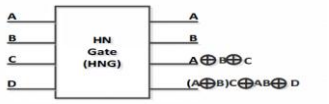


Fig 5(a) HNG

In this kind of Vedic multiplier the emphasis was given on low power and speed of multiplier. In this a technique of Vedic mathematics known as Urdhva Tiryakbhayam (UT) is used for multiplication [28].The number of gates used, the number of constant inputs and quantum cost is minimum till now in this Vedic multiplier. The garbage output is more in this multiplier so still there is chance to decrease it by using adder which can also acts as universal gate. The parameters are shown in table 5 (b) [28]

Table 5 (b) Comparison of multiplier designs

Multiplier	No. of gates	Constant Inputs	Garbage Outputs	Quantum Cost
[28]	37	29	62	162
[10]	53	58	58	286

6. CONCLUSION

There is huge scope of reversible computing in low power VLSI and this low power consumption requirement can be improved both by improving architecture as well as looking more into reversible circuits. By implementing both row and column bypassing technique in multiplier and using reversible gates, low power requirement can be met. HNG gate is efficient full adder till now as comparing with other in literature. The main aim should be decreasing number of garbage outputs and lesser number of gates. Thus this paper provides an important review for looking into the problem of this low power consumption.

7. FUTURE WORK

There is lot of scope for optimizing the reversible multiplier more by inventing new gates which have lesser garbage output. Reversible multiplier if implemented by using both row and column by passing by inventing necessary gates with lesser number of garbage outputs will consume very less power for higher order multiplier. By employing testing on reversible multiplier the research can be further enhanced. Reversible BILBO can be designed and used on low power multiplier so that multiplier will become self testable. Wallace tree multiplier can be designed by designing efficient reversible compressor which will also consume less power and will make the multiplier less complex.

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