Design and Simulation of a Low Power Viterbi Decoder using Constraint Length Nine

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ABSTRACT
Viterbi Decoder is the dominant module to determining the power consumption of the system. High speed and low power design of Viterbi Decoder with data rate1/2 and convolution encoding with a constraint length K = 9 is presented in this paper. The Proposed Viterbi decoder can be reduce the power consumption without reducing the decoding speed and also increases the length of the bits. The operating frequency of convolution encoder and Viterbi decoded is 306.65MHz and power consumption is 45.01Mw using Xpower tools in Xilinx and Spartan 3E FPGA kit.

Keywords
Viterbi decoder, Low power, Xilinx power estimator, Spartan3E, high speed.

1. INTRODUCTION
In today's digital communications, the reliability and efficiency data transmission is most concerning issue for communication channels. Error correction technique acts as a important role in communication systems. The error correction technique increases the capacity by adding redundant information for the source data transmission.

In the late 1940's the approach to error correction coding taken by modern digital communications system started with ground breaking work of Shannon, Hamming and Golay. The theoretical limits of reliable communication were defined by the Shannon while Hamming and Golay were developing the first practical error control schemes. The Hamming codes and Golay codes are categorized as a linear block codes.

In 1954, a new class of linear block codes named Reed-Muller codes were discovered by Muller[4]. Reed-Muller Codes allowed more flexibility in the size of the code and the number of correctable errors per code word. The following discovery code was the cyclic codes[10]. Cyclic codes are also called cyclic redundancy check (CRC) codes primarily used today for the error detection applications ratherthan for error correction. Bose-Chaudhuri-Hocquenghem(BCH) codes are the important subclass of the cyclic codes which discovered by Hocquenghem in 1959 and by the team of Bose and Ray-Chaudhuri in 1960. Then the BCH codes were extended to the non-binary case (q > 2) by Reed and Solomon in 1960. The Reed-Solomon (RS) codes have found the extensive applications in such systems as Compact Disk (CD) players, Digital Versatile Disk (DVD) players and the Cellular Digital Packet Data (CDPD) standard when the efficient decoding algorithm was introduced by Berlekamp in 1967.

All communication channels are subject to the additive white Gaussian noise (AWGN) around the environment. Forward error correction (FEC) techniques are used in the Transmitter to encode the data stream and receiver to detect and correct bits in errors, hence minimize the bit error rate (BER)to improve the performance[1][9]. RS decoding algorithm complexity is relatively low and can be implemented in hardware at very high data rates and seems to be an ideal code assigns for any application. However, RS codes achieve very weekly in AWGN channel. Due to weaknesses of using the block codes for error correction in useful channels, a different approach of coding called convolutional coding. The convolutional coding had been introduced in 1955. Convolutional encoding with Viterbi decoding is a powerful FEC technique that is particularly suited to a channel in which the transmitted signal is corrupted mainly by AWGN. The convolution encoding with viterbi decoding operates on data stream and has memory that uses previous bits to encode, and has good performance with low implementation cost.

The Viterbi algorithm (VA) was proposed in 1967 by Andrew Viterbi [3][4] and is used for decoding a bit stream that has been encoded using FEC code. The convolutional encoder adds idleness to a continuous stream of input data by using a linear shift register. The Convolutional Encoder and Viterbi Decoder used in the Digital Communications System is shown in Fig:1. Most of the Viterbi decoders in the market are a parameterizable intelligent property (IP) core with an efficient algorithm for decoding of one convolutionally-encoded sequence only. In addition, the cost for the convolutional encoder and Viterbi decoder are expensive for a specified design because of the patent issue. Therefore, to realize an adaptive convolutional encoder and Viterbi decoder on a field programmable gate array (FPGA) board is very demanding. In this paper, we concern with designing and implementing a convolutional encoder and Viterbi decoder which are the essential block in digital communication systems using FPGA technology.

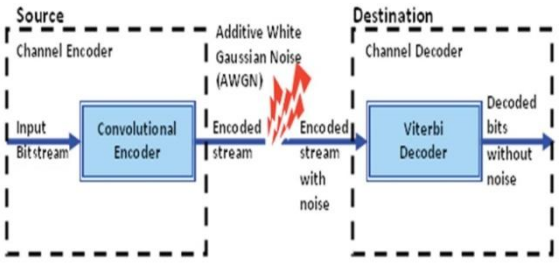

Fig 1: Convolutional encoder and Viterbi decoder.

2. CONVOLUTIONAL ENCODER

A convolutional code is a type of error-correcting code which differs a lot from block codes[1]. First, the former does not have code words made up of distinct data sections and block sections. Instead, redundant bits are distributed throughout the coded data. Second, the encoder of the former contains memory and the *n* encoder outputs at any given time unit depend not only on the *k* inputs at that time unit but also on m previous input blocks. Convolutional codes are sometimes referred as trellis codes. Normally, convolutional encoding is simple, but decoding is much more difficult.

Convolutional codes are usually characterized by two parameters and the patterns of *n* modulo-2 adders. The two important parameters are the code rate and constraint length. The code rate (k/n) where the number of output bits must equal or bigger than the input bits (*n*,*k*), is expressed as a ratio of the number of bits into the Convolutional encoder *k* to the number of channel symbols output by the Convolutional encoder *n* in a given encoder cycle[1]. To convolutionally encode data, start with *m* memory registers (flip flop), each holding 1 input bit. Unless if not fixed, all memory registers start with a value of 0.Theencoder has *n* modulo-2 adders, and *n* generator polynomials, one for each adder. An input bit *m1* is fed into the left most register. Using the generator polynomials and the existing values in the remaining registers, the encoder outputs *n* bits. As shown in Fig:2, where we have a general encoder designed with a code rate (k/n) of 1/2 and an information sequence that is being shifted in to the register *m* of 1 bit at a time. The shift register has a constraint length (K) of 3, equal to the number of stages in the register. The output from the encoder is called code symbols. At initialization all stages in the encoder shall be initially set to zero. The output of the encoder is determined by the generator polynomial equations.

Since the complexity of the encoder increases exponentially with the constraint length, none of the encoders uses more than a constraint length of 9, for practical reasons.

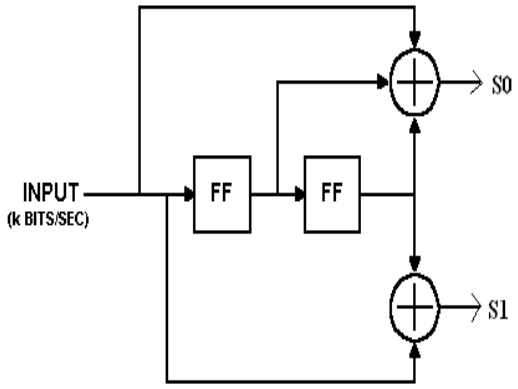

Fig 2: Convolutional encoder with data rate of 1/2 and constraint length 3.

3. VITERBI DECODING ALGORITHM

Viterbi decoding is one of two types of decoding algorithms [3]used with convolutional encoding the other type is sequential decoding. Sequential decoding has the benefit of that it can perform very well with long-constraint-length convolution codes, but it has a variable decoding time. A conversation on sequential decoding algorithms is further than the scope of this paper.

Viterbi decoding has the advantage that it has a fixed decoding time[5][6]. It is well suited to hardware decoder execution. But its computational necessities grow exponentially as a function of the constraint length, so it is generally limited in practice to constraint lengths of K= 9 or less. Stanford Telecom produces a K= 9 Viterbi decoder that operates at rates up to 96 kbps, and a K=7Viterbi decoder that operates at up to 45Mbps.AdvancedWireless Technologies (AWT) offers a K = 9 Viterbi decoder that operates at rates up to 2 Mbps. For years, convolutional coding with Viterbi decoding has been the predominant FEC technique used in space communications, particularly in geo stationary satellite communication networks, such as VSAT (very small aperture terminal) networks. I think the most common variant used in VSAT networks is rate 1/2 convolutional coding using a code with a constraint length K= 9. With this code, you can transmit binary or quaternary phase-shift-keyed (BPSK or QPSK) signals with at least 5 dB less power than you'd need without it. That is a reduction in watts of more than a factor of three.

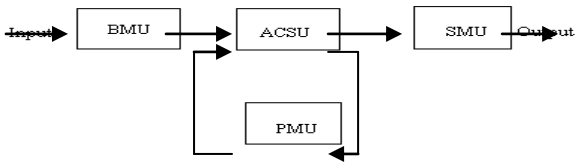

Fig 3: Block diagram of Viterbi decoder.

4. IMPLEMENTATION OF VITERBI DECODER

The major tasks in the Viterbi decoder process are as follows:

- Branch metric unit
- Add compare -select unit.
- Path metric unit
- Survivor metric unit

Fig.3 shows the proposed Viterbi decoder. This section discusses the different parts of the Viterbi decoding process[7]. Analog signals are quantized and converted into digital signals in the quantization block. The frame boundaries of code words and symbol boundaries were detected by the synchronization block. We assume that a Viterbi decoder receives parallel successive code symbols, in which the boundaries of the symbols and the frames have been identified.

4.1 Branch Metric Unit

Branch metric unit is used to generate branch metrics[4], which are hamming distances of input data from 00, 01, 10 and 11. The BM unit is used to calculate branch metric for all trellis branches from the input data[5]. We choose absolute difference as measure for branch metric. These branch metrics are considered as equaling the weights of the branches

4.2 ACS (Add Compare Select) Unit

A new value of the state metrics has to be computed at each time instant. In other words, the state metrics have to be updated every clock cycle. Because of this recursion,

pipelining, a common approach to increase the throughput of the system, is not applicable. The Add-Compare-Select (ACS) unit hence is the module that consumes the most power and area.

Since the state metrics are always positive numbers and since only positive branch metrics are added to them, the accumulated metrics would grow indefinitely without normalization. The operation of the ACS unit is shown in Fig. 4. The new branch metrics are added to previous state metrics to form the candidates for the new state metrics. The comparison can be done by using the subtraction of the two candidate state metrics, and the MSB of the difference points to a larger one of two.

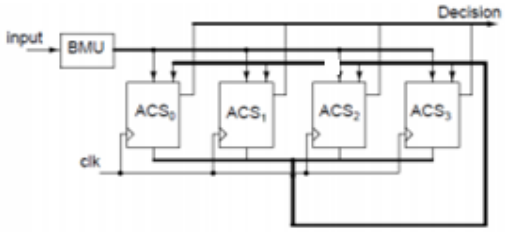

Fig 4: ACS Unit.

4.3 Path Metric unit

Memory is required to store the survivor Path Matrix Unit (PMU)[2]. The word length of the memory depends on the number of the ACS sub-blocks used in the design or the total number of states in the decoder or k^2 (where k is the International Journal of Modeling and Optimization, Vol. 3, No. 1, February 2013 16constraint length, 5 in our case), and the depth of the memory depends on the trellis length. The memory depth usually should be kept two times the trellis length or two blocks of memory equal to trellis length. We have for our project k = 5and trellis length equal to 32, so the memory block used is64x16. The memory used is dual port. One port for writing the data and other for reading the data, as we need to write and read the data simultaneously and that to from different addresses. Memory should write data synchronously but the reading of the data should be asynchronous to keep the latency low or better manage the synchronous behavior of the full system.

4.4 Survivor metric unit

In this the output data is obtained in survivor metric unit (SMU). In this survivor metric unit two bits obtained the LSB bits are neglected only the MSB bits are taken as output. So, smu is output decision unit.

5. SIMULATION AND SYNTHESIS RESULTS

Synthesis is a process of constructing a gate level netlist from a register transfer level model of a circuit described in Verilog HDL .Increase the design size and complexity, as well as improvement in design synthesis and simulation tools, have made Hardware Description Languages (HDLs) the preferred design languages of most integrated circuit designers. The two important HDL synthesis and simulation languages are Verilog and VHDL. Both have been adopted as IEEE standards.

5.1SimulationWaveforms of Convolution Encoder and Viterbi Decoder

The Simulation Waveform of Viterbi Decoder is shown in Figure 9 (For Rate ½ and K = 9). The simulation is done by using Modelsim and the speed and resource utilization is generated and synthesized using Xilinx Synthesis Tool (XST).

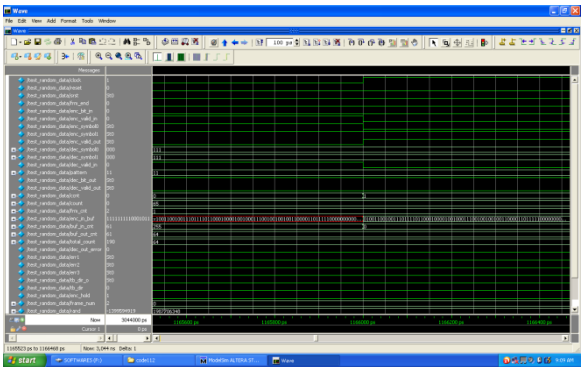

Fig 5: Simulation result of convolution encoder

In the above simulation waveform the convolution encoder encoded and store the 256 bits in the one half of the cycle is shown in above fig:5.

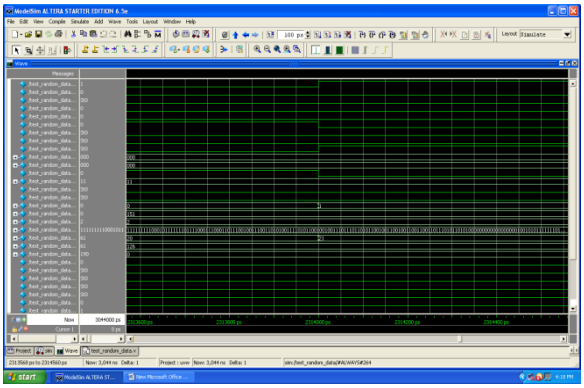

Fig 6: Simulation result of viterbi decoder.

In the above simulation waveform the viterbi decoder decoded the encoded bit stream and give the output on the second half of the cycle is shown in above fig:6.

5.2 Device Utilization Report

This synthesis report is generated after the compilation of Design for the targeted Xilinx SPARTAN 3E based Xc3s400a FPGA Device. Here, The Design unit is not implemented on targeted FPGA Device. This report contains about Timing and power summary.

6. COMPARISON OF RESULTS

TABLE 1

Parameters	Existing system	Proposed system
Data rate	¾	1/2
Constraint length	7	9
No of bits stored for each cycle	2^(7-1)=64 bits	2^(9-1)=256 bits
Frequency	446.4MHz	306.65MHz
Power	20.069mW	45.01mW

In this paper final result the data rate is decrease to 1/2 and the constraint length increases to 9, so at the output number of bits stored for each cycle increases to 256 bits. The frequency decreases to 306.65 MHz and the power consumption increases to 45.01mW.But when compared with the previous system the 256 bits transmission power increases to 4times that is 81mW used but our proposed system only 45.01mW consumed so power reduced to 50%.

7. CONCLUSIONS

In this Paper Resource optimized Viterbi Decoder with rate 1/2 and constraint length 9 has been proposed. The proposed Viterbi Decoder has been designed with Verilog using trace back method. The designed Viterbi Decoder has been simulated using Modelsim simulator and synthesized with Xilinx ISE. The simulated and synthesized results show that proposed design can work at an estimated frequency of 306.65 MHz for constraint length 9 respectively by using considerable less resources of target FPGA device SPARTAN 3E. This Paper also shows impact of constraint length on the performance. The comparative analysis result shows that as constraint length increases VLSI hardware complexity increases and Max. Frequency decreases and constraint length increases bit error rate decreases.

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