Performance Analysis of Gate-All-Around Field Effect Transistor for CMOS Nanoscale Devices

Awanit Sharma
Research Scholar, ITM,
Gwalior, India

Shyam Akashe
Associate Professor, ECED
ITM University

ABSTRACT
This paper explains the performance analysis of Gate-All-Around silicon nanowire with 80nm diameter field effect transistor based CMOS based device utilizing the 45-nm technology. Simulation and analysis of nanowire (NW) CMOS inverter show that there is the reduction of 70% in leakage power and delay minimization of 25% as compared with 180 nm channel length.Gate-All-Aorund (GAA) configuration provides better and low drain induced barrier lowering (DIBL) ~63.3mV/V and competent Subthresold slope ~95mV/V. GAA achieved the better voltage gain of ~10.1 V/V .Static noise margin improved with 400mv. It provides high on drive current ~6mA this is validated that the threshold voltage of GAA field effect transistor.

Keywords
Gate-All-Around (GAA); silicon nanowire; Drain induced barrier lowering (DIBL); Metal oxide semiconductor field effect transistor (MOSFET)

1. INTRODUCTION
The continuous scaling of Gate-All-Around silicon nanowire field effect transistor FET as compared with single gate and double gate FET shows better short channel control over other structures [1]. GAA silicon nanowire FET is most promising candidate for future CMOS based electronic systems due to their gate controllability, low leakage, high on-off ration and enhanced carrier transport property. Analytical models of GAA fet for parameter extraction of devices is described in [2] , most of these models and SCE models describe the effectiveness of ideal GAA structure with quadruple cross section were reported in this paper . [3] Gate-all-around (GAA) Nanowire FET have been fabricated by top-down and bottom-up design [3], [4].Gate-All-Around (GAA) nanowire Field effect transistor has researched excellent electrostatic control over the channel surrounded by conducting gate and provides higher transconductance [5].Gate all-around (GAA) MOSFETs have captivated considerable observation as compared with double-gate and tri-gate [6], [7].Simulation and analysis shows that gate-all-around GAA configuration provides excellent performance owing to considerable effect of short channel as compared with other structures [8]..DIBL Suppression, and excellent Subthresold slope is advantage of GAA devices. Downscaling of channel length to 45 nm of MOSFET is restricting factor of static power consumption due to increase leakage in off state [9].In this paper performance analysis of NW CMOS inverter [10], [11], [12],carried out using Cadence virtuoso tool on 45nm technology and comparison have done for wire(channel) length of 180 nm with same configuration. This paper is divided into 5 sections. Section 2 describes the simulation and analysis of silicon NW nanowire GAA gate-all-around field effect transistor (FET) .Section 3 provides the nanowire CMOS Inverter performance results. Section 4 provides comparison of GAA gate-all-around NW CMOS inverter different parameters on channel length such as 180 nm and 45 nm.

2. GAA FET DESIGN CONCEPT AND SIMULATION
Figure.1 describes a circuit comparable to a developed model of GAA FET with applied drain to source voltage (VDS) of 1.2 V in 45nm technology.GAA NW FET circuit implementation is achieved by three parallel transistor corresponding to the gate surround at front and two lateral junction. Substrate can be used as the back gate to form a gate-all-around GAA structure. Diameter of nanowire is equivalent to width W for CMOS p-transistors and n-transistors (same for both cases) with gate length L to be fixed. Silicon nanowire integrations are to be done with gate spacing 160 nm, source to drain S/D length extension of 140 nm, S/D metal width 60 nm and gate width 120 nm leading to implementation of a nanowire. In this paper nanowire consider as the channel of length 45 nm. Diameter of nanowire for both n-FET and p-FET kept 80 nm and channel length reduced to 45 nm and gate width achieved to 120nm.On drive current IDS increase or decrease when negative or positive voltage due to increase or decrease majority charge carriers (hole). nanowire thus operated in accumulation mode FET generally p-transistors. VT threshold voltage observed before FET enter into accumulation mode. Voltage supply VDD of 1 V is applied that improve threshold voltage and a better response of drain current (ID) versus gate to source voltage (VGS) ID–VGS is obtained as given in figure 2. .Large p-FET on drive current is observed that is higher than n-FET is achieved due to high mobility of carriers in respect of two lateral gates orientation. Figure 2 (a) and (b) shows transfer graph of ID-VGS for n-FET and p-FET.

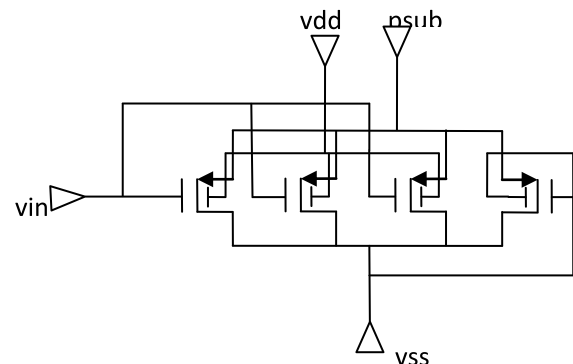

Fig.1(a) GAA p-FET schematic view.

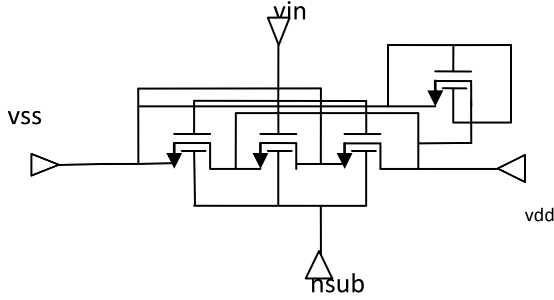

Fig. 1(b) GAA n-FET schematic view

Asymmetry is reported in p-FET and n-FET configuration and pull-down logic is observed due to similar channel length of wire 45 nm [9].For VDS = 1.2 V,VT threshold voltage for p-MOS and n-MOS are -0.2 and ~0.32 V. Similarly for VDS = 0.6 V, VT are -0.74 and~0.82 V. Figure 3 shows different output characteristics curve.ID versus VDS curve shows high drive current 25mA (PMOS) and 11.2mA (NMOS) for gate-source voltage(VGS = 1 V).Channel current is generally described by Fermi and silicon body potential.

$$I_{DS} = W\mu Q(x)\frac{(d\varphi_F(x))}{dx} \quad (1)$$

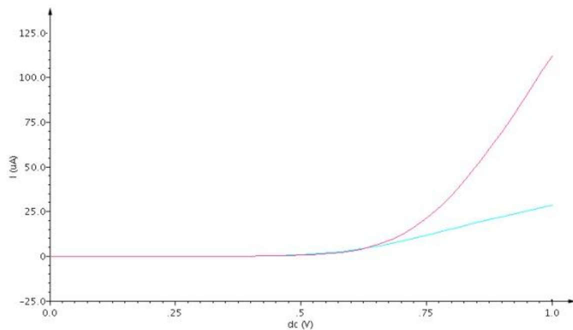

Fig. 2(a.*)* n-FET characteristics curve I_{DS} versus V_{GS} with V_{DS} = 1 V and 0.1 V

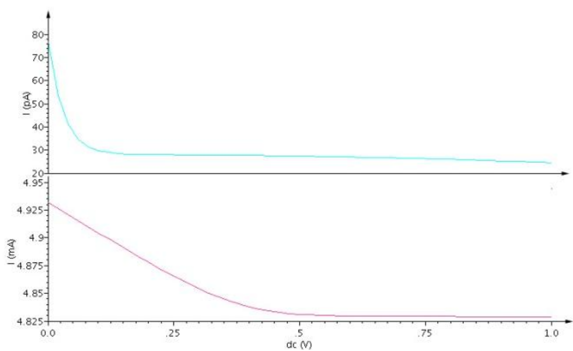

Fig. 2(b*)* p-FET characteristics curve I_{DS} versus V_{GS} with V_{DS} = 1 V and 0.1 V

Where w is width of FET , μ is mobility of charge carriers, Q denote the charge density and $\varphi_F(x)$ is potential (Fermi).GAA nanowire can be modeled using 1-D charge model .Current expression describe in terms of charge density at both end of channel [13].

$$I_{DS} = \frac{2\pi R}{L}\mu\left[2\frac{KT}{q}(Q_s - Q_d) + \frac{(Q_s^2 - Q_d^2)}{2C_{OX}} + \frac{KT}{q}Q_0 \log\left[\frac{Q_d + Q_0}{Q_d - Q_0}\right]\right] \quad (2)$$

$$Q_0 = 4\left(\frac{KTC_{OX}}{q}\right) \quad (3)$$

Where Qs and Qd are the density of charge carriers at the source and drain end of FET, R is radius of nanowire ,COX is capacitance of gate oxide.

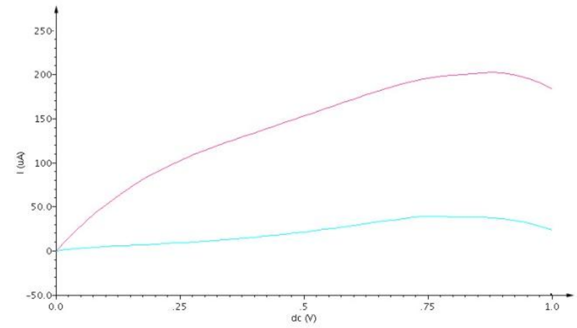

Fig. 3(a) I_D-V_{DS} curve for V_{GS} = 1 V and V_{GS} = 0.6 V.

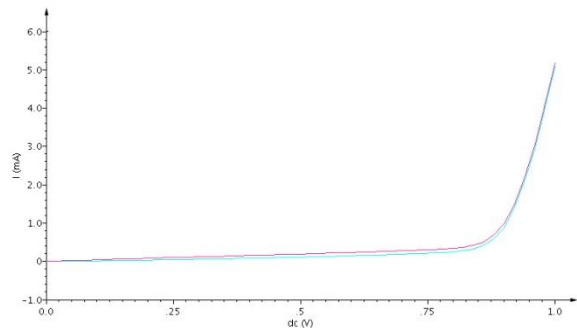

Fig. 3(b) I_D-V_{DS} curve for V_{GS} = 1 V and V_{GS} = 0.6 V.

Channel length of 45 nm for both p-FET and n-FET is fixed. Leakage current minimization occurs due to volume inversion of surrounding gate [14].As substrate is used as back gate for gate-all-around structure that made to be grounded then there some asymmetry observed in the output characteristics. Current intensity is low in the direction of forward bias of drain.ID saturation current is observed 5.7mA for VGS = 1 V. Performance of GAA transistor is described by respective parameter that include generally, the Sub threshold slope (SS) the drain induced barrier lowering (DIBL), transconductance (gm), on-off current ratio (ION / IOFF) and mobility of transistor (μ). The Subthresold slope (SS) can be defined is the inverse slope of ID -VGS curve that is observed one decade change in on drive current IDS.SS can be calculated by equation

$$SS = \frac{\Delta V_{DS}}{\log(\Delta I_{DS})} \quad (4)$$

$$S_{SS} = \ln(10)\frac{KT}{q}\left(1 + \frac{C_d}{C_{OX}}\right) \quad (5)$$

Where Cd is the capacitance at drain end and COX is the gate oxide capacitance. Low power CMOS devices generally required minimization of Subthresold swing value.SS is achieved to the value of 110mV/dec in GAA NW devices for channel length of 45 nm. In cylindrical nanowire GAA FET, the SS and DIBL generally keep short channel effect control that generally depend on α = L/2λ, a scaling factor on gate length and λ the natural length of the FET depend on εsi and εox that is dielectric constants of silicon and silicon oxide, where tsi and tox are the nanowire diameter and thickness of the gate dielectric.Natural length [15] is defined by below given equation.

$$\lambda = \sqrt{\frac{\varepsilon_{si}^2 t_{si}^2 \ln\left(1+\frac{2t_{ox}}{t_{si}}\right)+\varepsilon_{ox} t_{si}^2}{16\varepsilon_{ox}}} \quad (6)$$

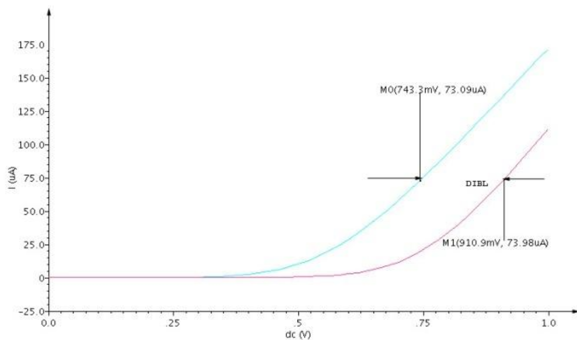

Fig. 4(a) Show DIBL (mV/V) curve of NW GAA FET

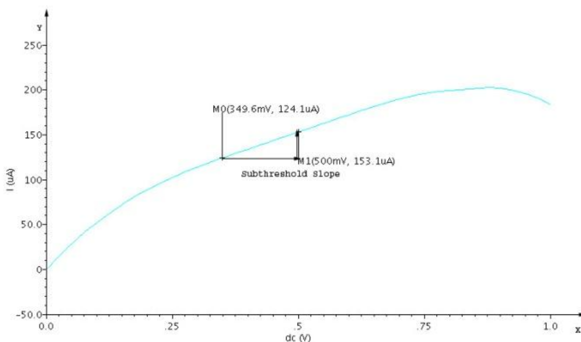

Fig.4(b) Represent curve of SS (Subthresold Slope) in mV/V.

DIBL can be defined transition of slope of curve due to change in threshold voltage when voltage supply VDD is given at two different voltage levels.

$$\mathrm{DIBL} = \frac{V_{t1} - V_{t2}}{V_{DS}\,(1V) - V_{DS}(0.1V)} \quad (7)$$

Where Vt1 and Vt2 are the threshold voltage at different VDS level. VDD = 1 V and 0.6 V is applied then gate-all-around structure achieved better and good performance with and low drain-induced barrier lowering(DIBL) (28 mV/V),sharp gate electrostatic control. Linear region of the characteristics curve of IDS versus VGS curve at VDS supply of 1 V show the transconductance gm that is slope of the curve. The transconductance is obtained 63.8µs/µm when channel length fixed to 45 nm. High transconductance observed due to surrounding gate structure.ION/IOFF ratio can be evaluated by observing the saturation current that is ION and depletion current that is IOFF in the graph of IDS versus VGS on logarithmic scale.ION/IOFF ratio come to 1.4×107.The mobility of charge carriers (hole) of silicon nanowire transistor can be evaluated by revealed its transconductance with the help of equation.

$$\mu_M = \frac{g_m L^2}{C N V_{ds}} \quad (8)$$

$$g_m = \frac{dI_{DS}}{dV_{GS}} \quad (9)$$

Where gm is transconductance, μ_M is mobility of charge carriers and Lis the length of nanowire where C represent capacitance of gate of nanowire ,L represent gate length, N represent number of nanowire [15].Gate capacitance can be evaluated with the help of equation described by expression.

$$C = \frac{2\varepsilon_0 \varepsilon_{sio_2} L}{\ln\left(r_G / r_{NW}\right)} \quad (10)$$

Where ϵ0 is the permittivity, ϵsio2 is the dielectric constant of the gate SiO2, rG is gate electrode inner radius, and rNW is the radius of nanowire. Average mobility of nanowire is obtained that becomes high as previously observed [16], [17].Figure 4 shows DIBL effect with transition of threshold voltage and Subthreshold slope that provide better electrostatic gate control due to surrounding gate structure.

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3. CMOS DEVICE (INVERTER) SIMULATION AND ANALYSIS

CMOS inverters are designed with GAA configuration that kept same nanowire diameter (equivalent to width W in CMOS) for p-transistors and n-transistors with channel lengths 45 nm to describe static and dynamic performances. This configuration has same diameter of wire 80nm for p-MOS and n-MOS. There is little asymmetry observed in drive current due to the same length L of n and p configuration of MOSFET. Figure 5 shows typical layout of GAA CMOS inverter.

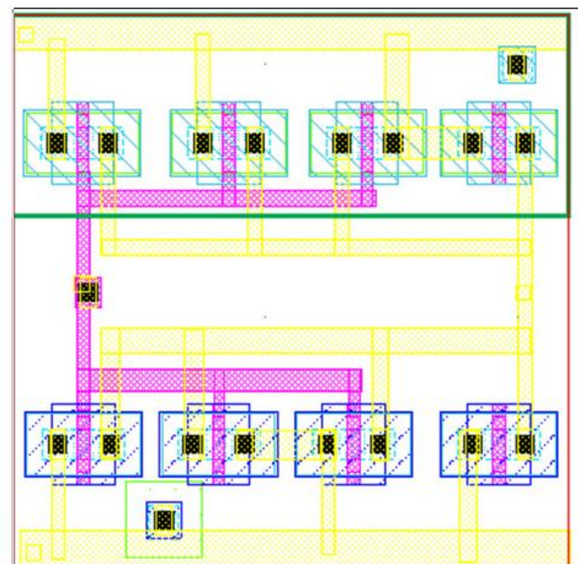

Fig. 5 Show layout of GAA Nanowire CMOS inverter

Inverter analysis shows sharp voltage transfer characteristics with high noise margin(NMH = 0.82 V and NML = 0.41 V)

with gain of ~10.1 for supply voltage VDD = 1 V. The noise margins and the gain are comparable with the fabricated lateral device characteristics observed in [12].].Noise margin can be calculated by analyzing the static behavior curve.

$$NM_H = V_{OH} - V_{IL} \quad (11)$$

$$NM_L = V_{IL} - V_{OL} \quad (12)$$

$$SNM = \min(NM_H, NM_L) \quad (13)$$

Figure 6 shows inverter static characteristics curve for simulated GAA inverter. The static characteristic of input-output curve of GAA silicon nanowire is revealed output flow is smaller due to faster rise and fall time of input. Lower current at peak flows in inverter during switching occurs from low to high or vice-versa. Short-circuit power dissipation occurs which can be minimized by properly design [17].Power dissipation come out when VDD = 1 V is 15.58 pW.

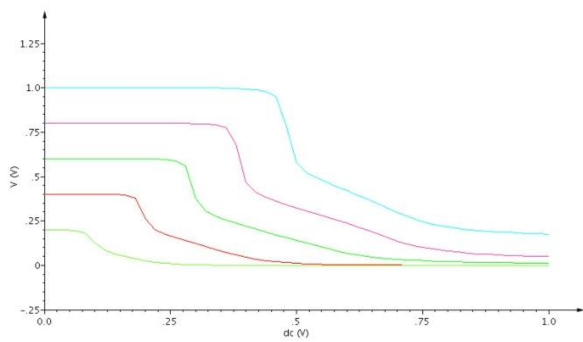

Fig. 6(a) Output transition (VOUT)-Input transition (VIN)

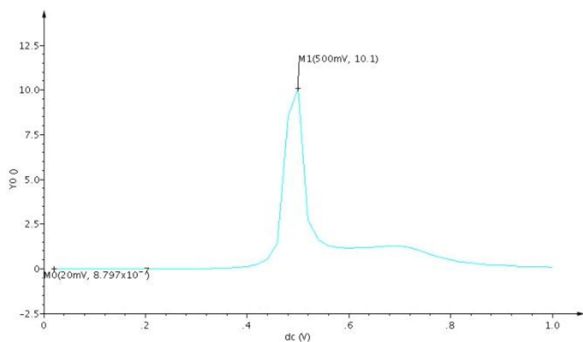

Fig. 6(b)Voltage gain versus Input pulse (VIN) at VDD = 1

The dynamic characteristics of single nanowire (80 nm diameter) inverters channel lengths of 45nm is shown in Figure 7.The dynamic behavior is performed by supply of voltage pulse of 1 V. Asymmetry is noticed in rise and fall duration in the inverter is associated to the discrepancy in n-MOS and p-MOS impulse with both FET being design on same wire with diameter of 80 nm. The dynamic characteristic observed when 20ns pulse of 1 V is applied having rise and fall time of 1 ns. Fig 7 show inverted characteristics of input signal. Larger load revealed lower drive potential, amplitude of output pulse is smaller than input pulse. Delay of inverter is observed 0.39 ns by fixed the channel length to 45 nm it becomes lower than when scaling of channel length is done. GAA inverter achieved 70% reduction of leakage power and 85% saving the power with supply of voltage VDD = 1 V. Low leakage power 15.58 pw and average power consumption 2.8 µw is evaluated in 45 nm technology. A reduction of delay up to 45% when scaling of channel length from 180 nm to 45 nm is done. Results of simulated inverter better than reported Fin-FET based inverter [18-20].

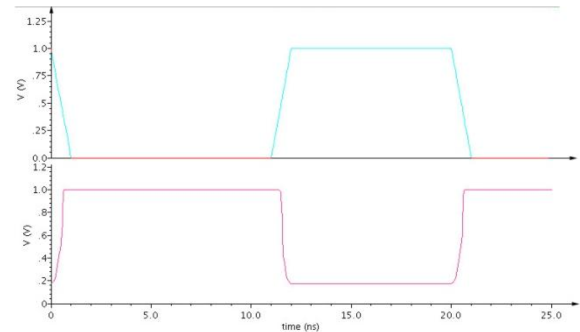

Fig. 7 Dynamic performance curve of CMOS inverter.

4. RESULTS AND ANALYSIS

GAA inverter developed by 45 nm technology using Cadence tool is compared with 180 nm channel length. Low DIBL and high subthreshold slope is observed in 45 nm. Table 1 shows the comparison of different output parameters in respect of channel length. Inverter configuration has a reduction of delay (30%) and static power decrease is observed when comparison is done with 180 nm channel length.GAA inverter provide 85% lower power consumption than same configuration in 180 nm. High voltage gain ~10.1 and high noise margin (NMH = 0.82 V and NML = 0.41 V), therefore overall performance enhanced. GAA NW devices have excellent performance in respect of scaling of channel length. Short channel effect moderately reduced compared to planar one.GAA observed better improved performance result where scaling of channel is done.

Table 1. Output parameters values of silicon nanowire FET at different channel length.

Output Parameters	Nanowire = 180 nm	Nanowire = 45 nm
Average Power(µW)	26.91	2.08
Leakage Power(pW)	42.79	15.58
Delay(ns)	0.57	0.39
Voltage gain(V/V)	7.07	10.1
Transconductance(µs/µm)	12.28	63.8
SNM(V)	0.14	0.33
DIBL	110 mV/V	64 mV/V
Subthresold	42.68 mV/dec	95 mV/dec
I_{ON}/I_{OFF}	5×10^6	1.4×10^7

5. CONCLUSION

This paper observed the GAA silicon nanowire CMOS inverter configuration using 45 nm technology. Inverter show

low static power dissipation 15.58 pW and improved average power consumption 2.08 μW as scaling is done on channel length from 180 nm to 45 nm.GAA has lower delay 0.39 ns in channel length 45 nm as compared with larger channel length of 180 nm. High noise margin estimation 0.33 V, sharp transition characteristics, low drain induced lower barrier DIBL 64mV/V ,and better Subthreshold slope 95mV/dec introduce excellent performance as compared with increased channel length.

6. ACKNOWLEDGEMENT

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