FPGA based Histogram Equalization Technique to Recognize Characters in Handwritten Scriptures of Palm Leaves

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BSTRACT
Multi-core processors play a vital role in the application such as image processing. In this manuscript the focus is made on such types of imaging applications where in which, the image processing is done on handwritten scriptures of palm leaves to study its mechanics of characters inscribed. Here in this paper the approach adopted is the digital image reconstruction with acquiring of the discrete projection image data. This manuscript highlights the important research directions which combine the image based analysis with exciting new developments in Field Programmable Gate Array (FPGA) which is based multi-core processor technology is utilized for image processing approaches. In the present research work we propose the method of FPGA based histogram equalization technique to recognize characters of Handwritten Scriptures in palm leaves in the form of discrete projections data . The FPGA used here is Virtex-4 the synthesis and analysis results are compared with the theoretical calculations.

Keywords
Histogram Equalization, Pattern Recognition, Image reconstruction, Discrete Projections , FPGA, HDL coder

1. INTRODUCTION
Analysis of the images with imaging methods which consists of the potential for the analysis of character properties such as detecting the pattern of the character, inscribed on the palm leaves constructs have the greater impact in a modern image processing based engineering. Detecting the pattern of the character on the palm leaf is the challenging problem that has been extensively studied over the years; still a correct solution is yet to be obtained. Histogram equalization method is one of the techniques where in which the original image of a historical handwriting [1] which is blur in nature is considered and the image is enhanced in terms of brightness and contrast using this technique. So that the characters inscribed on the palm leafs can be read more accurately. In this manuscript the objective is to design a digital system based on Field Programmable Gate Array (FPGA) technology which manages the visual information of character patterns inscribed on palm leafs which facilitates the design methods of computer aided mathematical modeling tools helpful for pattern recognition. Here in this manuscript the individual characters are not recognized but the entire script inscribed on a palm leaf is enhanced for clarity using the histogram equalization method, and by using FPGA the digital implementation is performed. The initial results involve the original image of palm leaf manuscript followed by the histogram equalized image along with a plot of histogram equalized image.

2. RELATED WORK
In the year 2008 , Olarik Surinta and Rapeeporn Chamchong in their work[1] considered the palm leaf manuscript on which image processing operations were performed such as back ground elimination, line and character segmentation. The work in [1] involved the design of the algorithm which first converts the color image into a grey image, then converts the grey image into a binary image using Otsu's algorithm, and finally produces the segmented lines and characters using projection profile analysis. In [2] the work presented involves the unique method of data collection initiated with recognizing the characters from palm leaf manuscripts, and the building of the palm leaf character database is described in the paper in [2]. The earliest forms of handwritten characters are considered as the written media consisting of knowledge hub for different subjects such as astrology, medicine in the histological documents [3]. In the current research work the novelty present is based on a FPGA based system design which is implemented aiming to extract the accurate data from the palm leaf manuscript with digital hardware implementation.

3. MATERIALS AND METHODS
In this research work, the software tool used is MATLAB R 2013-a, which is considered as a real time simulation environment for model based design applications [4]. The input image of the palm leaf consisting of handwritten characters in a tagged image format which is blur in nature is considered as the reference source of RGB which is then passed through the histogram equalization algorithm block , from which the obtained output is histogram equalized image which has the enhanced brightness and contrast. In the histogram plot section the original image and histogram equalized image is considered and compared with each other to obtain a comparison plot between original and histogram equalized image. The histogram viewer in MATLAB R 2013- displays the obtained comparison plots. For FPGA prototyping the technique utilized is HDL coder tool present in MATLAB R-2013-a, which takes the script written in MATLAB as the input and converts the script into a hardware description language (HDL) code for rapid prototyping on FPGA. The simulation and the synthesis results are obtained through the XILINX ISE v 8.1 software integrated development environment which is integrated in MATLAB for FPGA design. The FPGA design further involves the placement and routing of the mapped entity of pixel values of the scriptures inscribed on the palm leaf is mapped on the chip. The FPGA selected in this research work is Virtex-4 .

4. BLOCK DIAGRAM

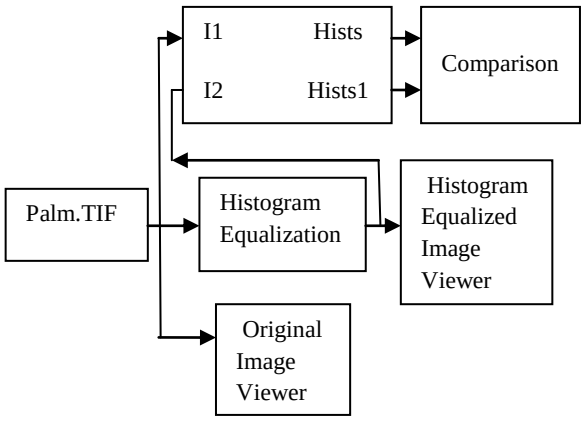

Fig1 Block Diagram of Histogram Equalization Algorithm

Above figure 1 illustrates the block diagram of histogram equalization algorithm in which the input image considered is palm.tif which in tagged image information format is passed through the histogram equalization algorithm and further through histogram equalized image viewer which displays the image of the histogram.

5. ALGORITHM DESIGN IN MATLAB

The histogram equalization algorithm is illustrated in the following steps for the function designed:-

a. Start
b. Define x_out, y_out , pixel_out , in the function.
c. Equate the above function to histogram equivalent of x_in , y_in , pixel_in , width , height set of values in the function.
d. Assign persistence to histogram, transfer function, histogram index, and cumulative sum.
e. Initialize the histogram, transfer function, histogram index, and cumulative sum to zero.

Figure out the index values based on which we locate the frame.

f. Read the Histogram
g. Read the Transfer Function
h. If :
   valid part of frame add one to pixel bin and keep transfer function value

   Then :

   Add the pixel to binary and write back the same value in the cumulative sum

i. In the blanking time index empty all the binary values and reset all values to zero
j. Write the Histogram
k. Write the transfer function
   Stop

A test script is designed in MATLAB r 2013-a inputs the original image and calculates the dimensions of the original input image in terms of height and width. Here the horizontal blanking is set to default value that is 20 and the vertical blanking should be set to maximum to filter the histogram. The figure 2 elucidates the original image of the palm leaf which has to be passed through the histogram equalization block for enhancing the image in terms of brightness and contrast.

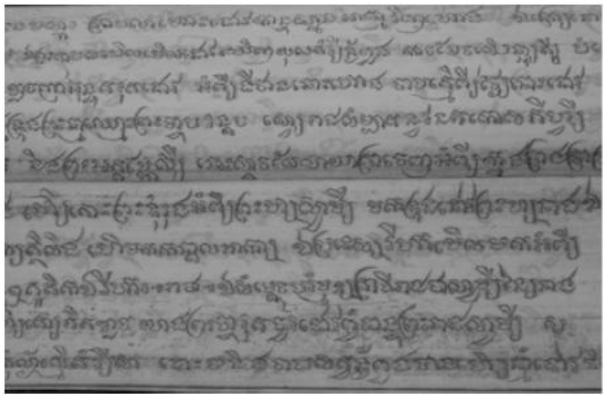

Fig 2 Original Image of Palm leaf

The figure 3 below illustrates the histogram equalized image which is enhanced image in terms of pixels values are improved compared to the previous blur input original image.

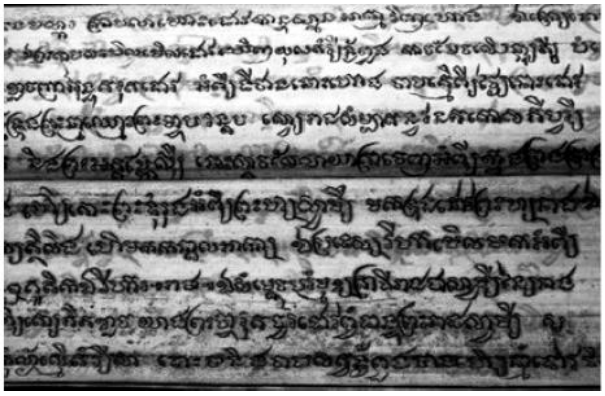

Fig 3 Histogram Equalized Image of Palm leaf

The figure 4 below illustrates the histogram of the original image and histogram equalized image in separate segments.

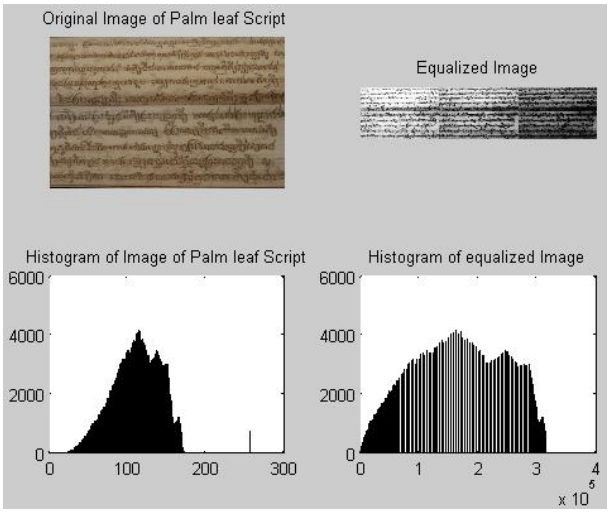

Fig 4 Histogram Equalization plots for original and equalized image

Here the original image of the palm leaf script is considered and further equalized. The histograms plots are obtained for both original and equalized image as seen in the above figure4. The figure 5 below illustrates the comparison plot of the histograms of original and equalized image obtained from the above figure 4.

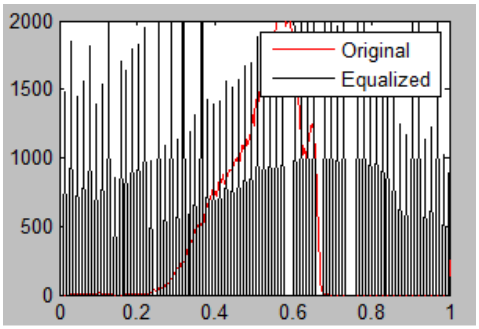

Fig 5 Comparison Plot of Original and Equalized image

6. FPGA PROTOTYPING IN MATLAB

The software tool used for FPGA prototyping is HDL coder which is based on a plug-in used inside the MATLAB R-2013-a which takes the input in the form of MATLAB script and converts it into the FPGA based HDL code for rapid prototyping of the design. Here the first step involves the defining the input types for the script in MATLAB. Here the input types are defined as type double 1x1 for x_in, y_in, pixel_in, height and width as shown in below figure 6.

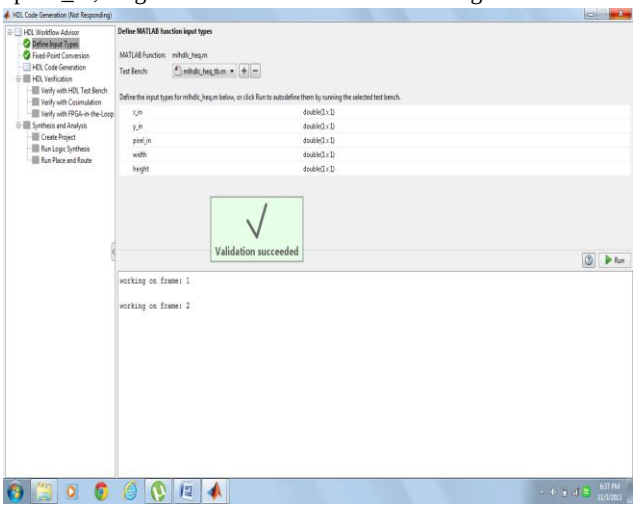

Fig 6 MATLAB HDL Coder menu Window

The following lines of output are obtained after running the test numerics in the HDL coder. In this case log inputs and outputs for the comparison plots are selected.

```
### Analyzing the design 'mlhdlc_heq'
### Analyzing the test bench(es) 'mlhdlc_heq_tb'
### Begin Floating Point Simulation
working on frame: 1
working on frame: 2
### Floating Point Simulation Completed in 255.7428 sec(s)
### Begin Fixed Point Simulation : mlhdlc_heq_tb
working on frame: 1
working on frame: 2
### Beginning fixed point error analysis ####
Errors are calculated as follows after simulation for each
output variable:
Errors (E) -- >Floating-point Values Fixed-point Values
Maximum Positive Error (Mpe)---> max(E)
* (max(E)>0)
Maximum Negative Error (Mne) ---> min(E) * (min(E)<0)
Top Error (TE) ----------------> Mpe (if Mpe > abs(Mne) )
otherwise Mne)
Maximum Absolute Value (MAE) ---> max(abs(Floating-
point values))
Maximum Percentage Error (MPE) -> 100 * (TE / MAE)
------ Output variable : x_out ----------
Max Positive Error 0
Max Negative Error 0
Max Absolute Value 1405
Max Percentage Error 0
Generating comparison plot...
---- Output variable : y_out --------
Max Positive Error 0
Max Negative Error 0
Max Absolute Value 310
Max Percentage Error 0
Generating comparison plot...
-------Output variable: pixel_out -------
Max Positive Error 0
Max Negative Error 0
Max Absolute Value 414414
Max Percentage Error 0
Generating comparison plot...
### Fixed Point Simulation Completed in 269.7425 sec(s)
### Elapsed Time: 525.7028 sec(s)
```

The comparison plots generated are as follows in figures 7, 8, and 9 below along with error plot:

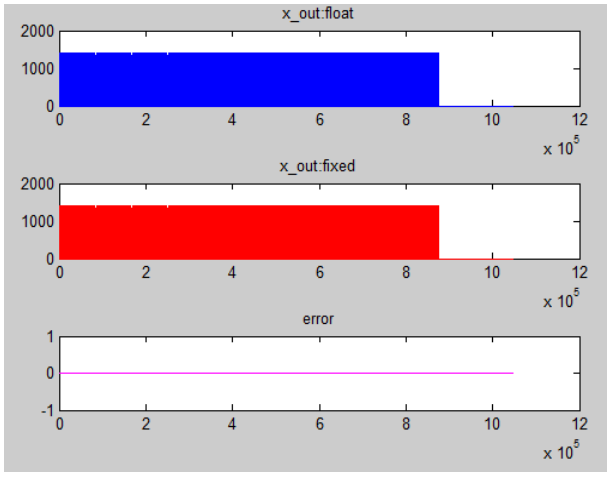

Fig 7 Comparison plot for x_out fixed and float

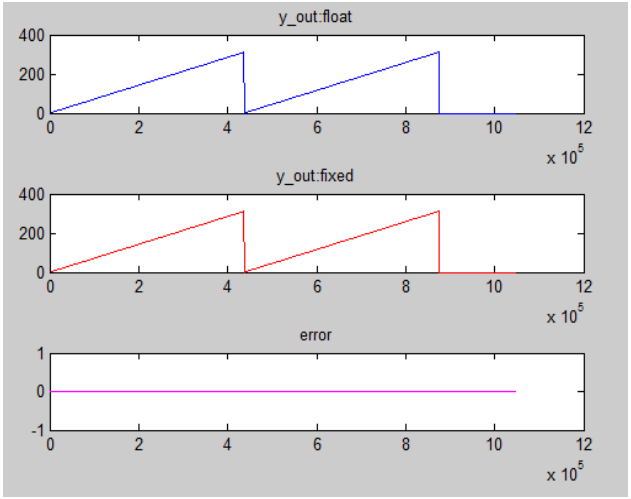

Fig 8 Comparison plot for y_out fixed and float along with error analysis

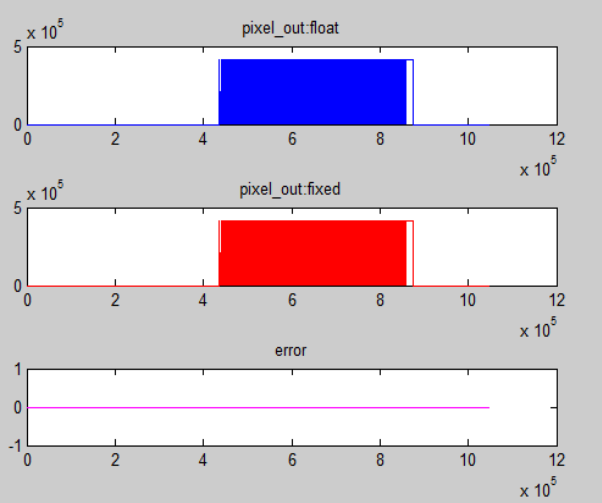

Fig 9 Comparison plot for pixel out fixed and float

The summarized HDL resource utilization report is elucidated below table 1:

S. No	Entity	Numbers
1	Multipliers	0
2	Adders/Subtractors	28
3	Registers	101
4	RAMs	2
5	Multiplexers	35
6	10x10-bit Adder	1
7	16x16-bit Adder :	1
8	8x8-bit Adder	2
9	9x9-bit Adder :	8
10	13x13-bit Adder	1
11	32x32-bit Adder :	2
12	20x20-bit Adder	1
13	15-bit-2-to-1 Mux	4
14	8-bit 2-to-1 Mux	4
15	8-bit 2-to-1 Mux	5
16	13-bit 2-to-1 Mux	7
17	19-bit 2-to-1 Mux	5

Table 1 Resource Utilization Summary

The device under test (DUT) requires an initial pipeline setup latency. Each output port experiences these additional delays.
Output port 0: 4 cycles
Output port 1: 4 cycles
Output port 2: 4 cycles
Output port 3: 4 cycles

The FPGA register transistor logic (RTL) synthesis [5] diagram designed is as obtained in XILINX-ISE design v 8.1 illustrated in figure 10. The block elucidates the details of schematic consisting of input details of height with vector of 8:0 , pixel_in with the vector value of 8:0 , width of the vector of value 8:0 ,x_in of the vector value of 10:0 ,y_in with the vector value of 8:0 , clock ,clock enable , and reset. The output pins are defined as pixel_out of 18:0 vector value ,x_out having the vector value of 10:0 ,along with the y_out of the vector value of 8:0 and the chip enable signal(ce_out). The entire FPGA design is ported on FPGA through the ACE file designed is as shown in figure 11, which is 3.55% of full utilization memory size of the remaining 124.0 bits.

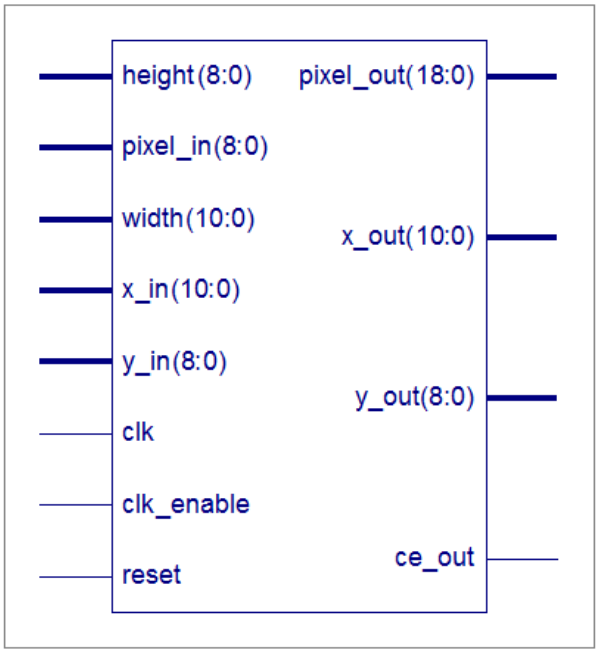

Fig 10 RTL synthesis block

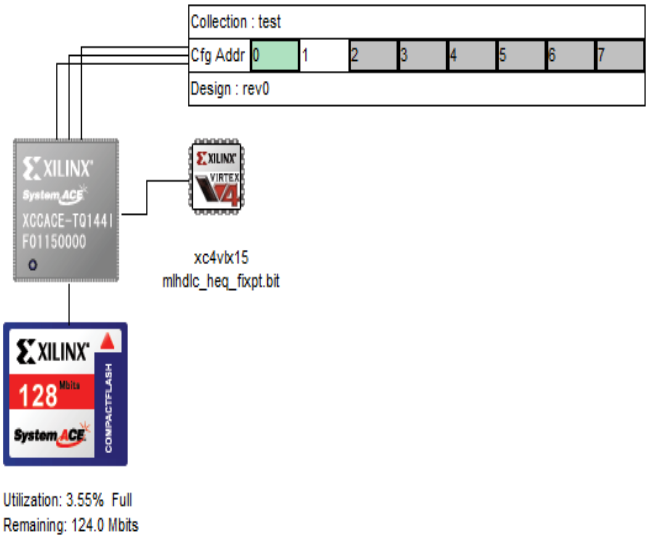

Fig 11 Generated ACE file in Xilinx Environment

7. CONCLUSIONS

In the present research work the method of FPGA based histogram equalization technique is elucidated to recognize characters of Handwritten Scriptures in palm leaves. The FPGA used here is Virtex-4 the synthesis and analysis results are compared with the theoretical calculations.

8. FUTURE SCOPE

The future scope of this work involves the discrete projections of data consisting of medical images instead of hand written scriptures of palm leaves, here we aim to remap the real x-ray projection data in to the form of discrete projections, from a digital PxQ pixel grid at discrete projection angles p:q. The minor area of research is considered as image reconstruction and projection mapping . The entire design can be mapped on the ARM/FPGA based multi core processor. Also compare the images reconstructed from Mojette-adapted projection data using Finite Radon Transform, direct back-projections and iterative reconstruction methods and also to examine the robustness of the reconstructed images to tailored levels of

noise added to real and simulated projection data. Here it is proposed to obtain the graphical evidence of reconstructed image quality for a variety of discrete projection and reconstruction methods for a defined range of noise levels and noise distributions. We also propose evaluate the methods to tune and improve the image reconstruction quality by applying regularization methods to the inversion filters for direct back-projection approach.

9. REFERENCES

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