Design of RS and D-Flip-Flop using AlGaAs/GaAs MODFET Technology

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ABSTRACT
This paper enumerates high speed design of RS & D- flip-flop using AlGaAs/GaAs MODFET. The proposed Flip Flop is having less number of transistors than existing designs. Simulation results show lowest average power and least delay than existing designs. This Flip-Flop having less number of transistors.It can be efficiently used in VLSI ICs. In the verification by simulation, the proposed flip-flops appear to have better speed of operation. It is simple and suitable to SPICE simulation of hybrid digital ICs.

Keywords
Flip-Flop, MODFET, delay, PDP, power consumption.

1. INTRODUCTION
Technology scaling of a transistor feature size has provided a remarkable innovation in silicon industry for the past few decades. Designers are striving for semiconductor area, higher speed, low power consumption and reliability due to ever increasing demand and popularity of portable electronics. With the increasing use of mobile devices, consumer electronics markets demand a stringent constraint on reducing the power dissipation. In order to reduce the complexity of circuit design, the digital circuits are designed to be synchronous circuits. The memory elements in a sequential circuit are called flip-flops. A flip-flop has two outputs, one for the normal value and one for the complement value of the stored bit. Binary information can enter into a flip-flop in a variety of ways and gives rise to different types of flip-flops. MODFETs are used in integrated circuits as digital on-off switch. FETs can also be used as amplifiers for large amounts of current using a small voltage as a control signals. Both of these are made possible by the FET's unique current-voltage characteristics. MODFETs are heterojunctions. This means that the semiconductors used have dissimilar band gaps. When a heterojunction is formed, the conduction band and the valence band throughout the material must bend in order to form a continuous level.The Modulation doping field effect transistor has demonstrated characteristics which make it highly suitable for high performance high speed system. In this paper describes high speed RS & D-flip flops using MODFET technology. In this paper, logic gates are designed using RTL logic, So the number of transistors used for making Flip Flops is very less and the area of the Flip Flops is also reduced. The design for low power issues can't be overcome without precised power prediction and optimization tools. Therefore, the critical need for certain tools to calculate power dissipation during the design to meet the power constraints to ignore the costly redesign effort. Power consumption is affected by many factors, $P = \alpha Cf$ [7].

2. CIRCUIT DESIGN

2.1 RS FLIP FLOP
Please use a 9-point Times Roman font, or other Roman font When using logic gates as building blocks, the fundamental latch is the simple SR latch, where S and R stands for set and reset. And it can be constructed from a pair of cross-coupled NOR gate logic. The stored bit is present on the output marked Q.

While the S and R inputs are both low, feedback maintained the Q and Q outputs in a constant state, with Q the complement of Q. If S(set) is pulsed high while R (Reset) is held low, then the Q output is forced to high, and stays high when S will returns to low, similarly, if R is pulsed high while S(set) is held low, then the Q output is forced to low, and stays low when R returns to low. The logic diagram of SR flip flops is shown in fig.2 and circuit diagram is shown in fig.3. Clocked RS Flip-flop operates as a standard bistable latch but the outputs are only activated when a logic "1" is applied to its EN input and deactivated by a logic "0". The property of this flip-flop is summarized in its characteristic table where Qn is the logic state of the previous output and Qn+1 is that of the next output and the clock input being at logic 1 for all the R and S input combinations. The logic diagram of clocked SR flip flops is shown in fig.3 and circuit diagram is shown in fig.4

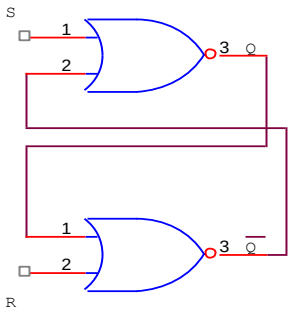

Fig 1: Logic diagram of SR Flip Flops using NOR gate

Table 1. SR latch operation

S	R	Action
0	0	No Change
0	1	Q = 1
1	0	Q = 0
1	1	Restricted combination

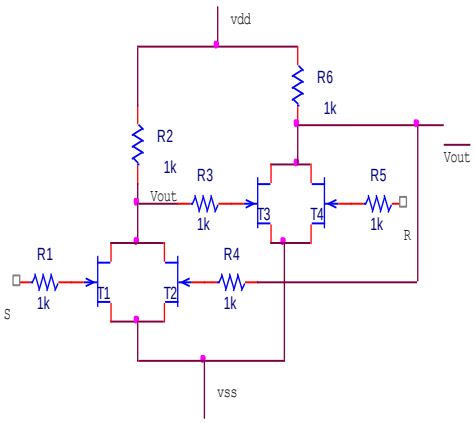

Fig 2: Circuit diagram of SR Flip Flops using NOR gate

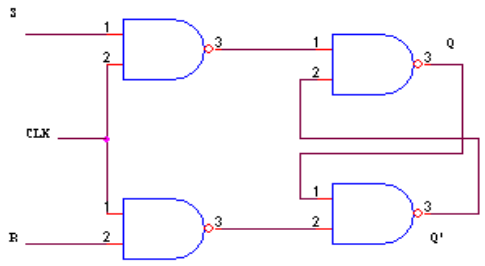

Fig 3: Logic diagram of Clocked SR Flip Flops using NAND gate

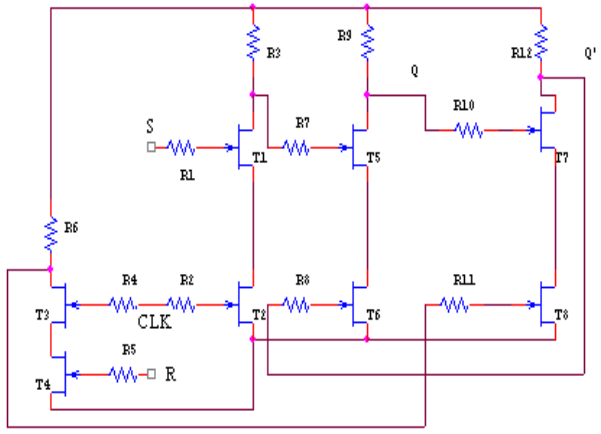

Fig 4: Circuit diagram of Clocked SR Flip Flops using NAND gate

2.2 D FLIP FLOP

The D flip-flop is shown in Figure 6 is a modification of the clocked SR(Set-Reset) flip-flop. The D input goes directly into the S input and the complement of the D input goes to the R(Reset) input. The D input is sampled during the occurrence of a clock pulse. If it is 1(on), the flip-flop is switched to the set state (unless it was already set). If it is 0(off), the flip-flop switches to the clear state. The logic diagram of D flip flops is shown in fig.6 and circuit diagram is shown in fig.7

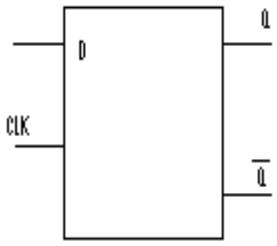

Fig 5: Symbol for an D Flip Flop

Table 2. Truth table for D flip-flop

Clk	D	Q
0	0	0
0	1	1
1	0	0
1	1	1

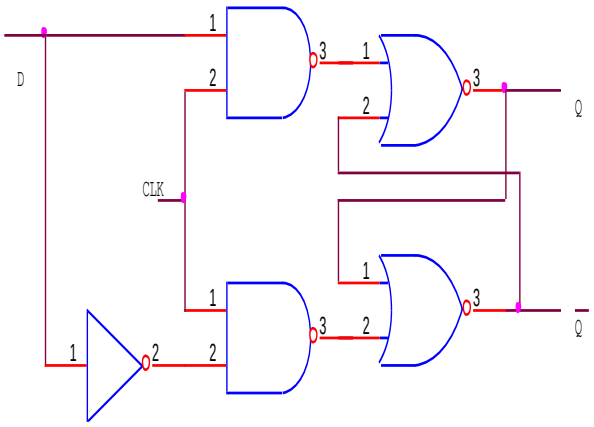

Fig 6: Logic diagram of D Flip Flops

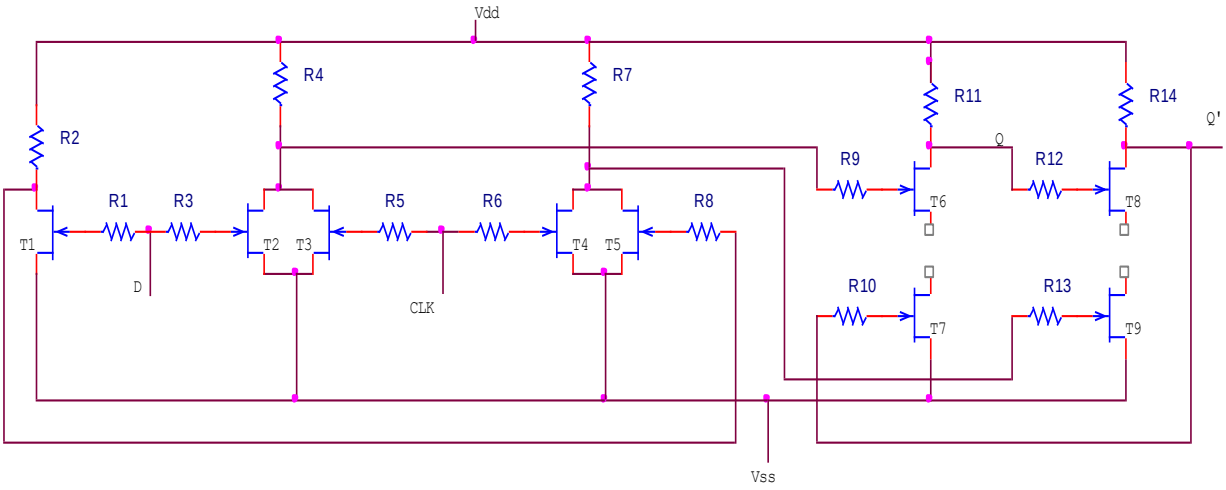

Fig 7: Circuit Diagram of D Flip Flop using MODFET

3. PERFORMANCE ANALYSIS

To evaluate the performance of proposed RS and D flip flop using MODFET technology. Simulations are carried out using PSPICE tool in nominal conditions with operating frequency at 1GHz. Transient analysis of the proposed RS and D flip flop using MODFET technology is shown in figure 9 and 10.

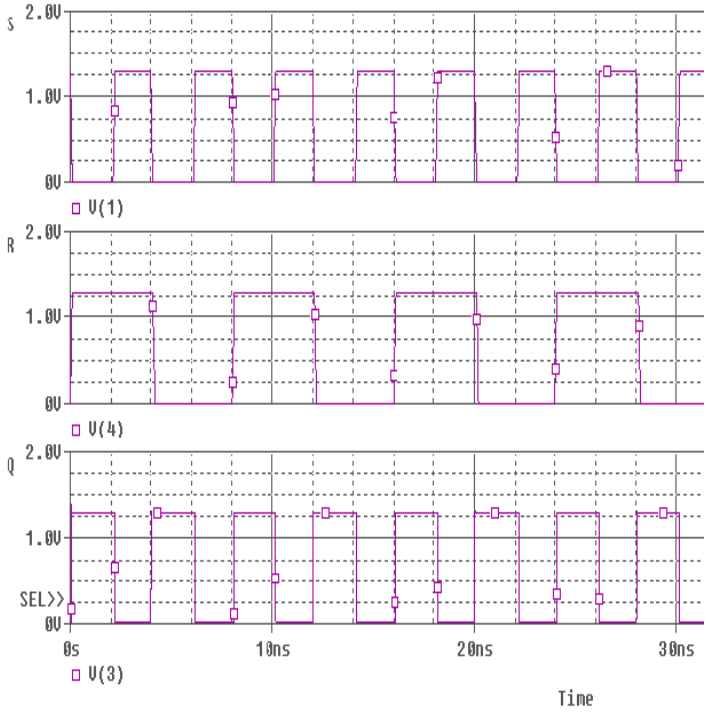

Fig 8: Output waveform for proposed RS Flip Flop

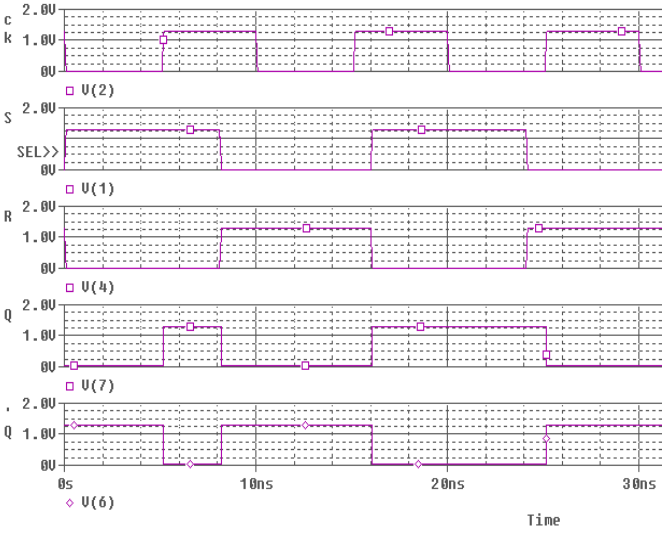

Fig 9: Output waveform for proposed Clociked RS Flip Flop

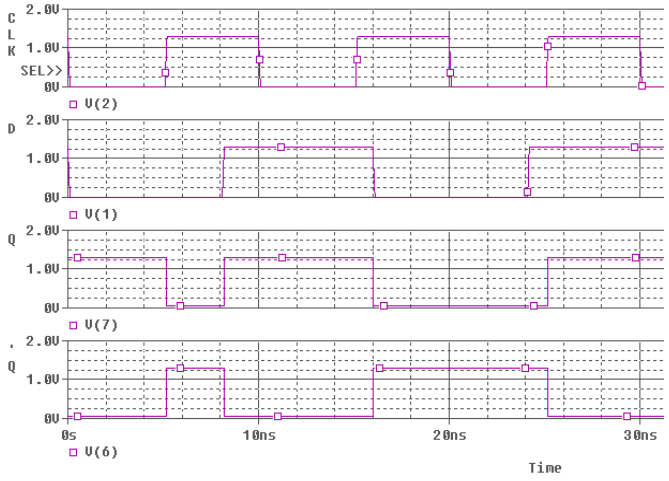

Fig 10: Output waveform for proposed D Flip Flop

5. COMPARISON OF MOSFET, AND MODFET D FLIP-FLOPS

The proposed RS and D flip flop using MODFET is designed and compared with several conventional Flip-Flops. Each Flip-Flop is optimized for power delay product. The proposed flip flop is having lesser number of clocked transistors than the other flip flop. Simulation results for power, delay, PDP and area at nominal conditions for the Flip-Flops are summarized in Table 3. And comparison graph is shown in the fig.11a, 11b, 11c.

Table 2. Comparison of MOSFET, CNTFET and Proposed MODFET D flip flops

Device	Delay ($*10^{-12}$ Sec)	Power ($*10^{-6}$W)	PDP ($*10^{-17}$ J)
Con. DFF	55	4.23	23.27
Proposed DFF	26	2.80	7.28

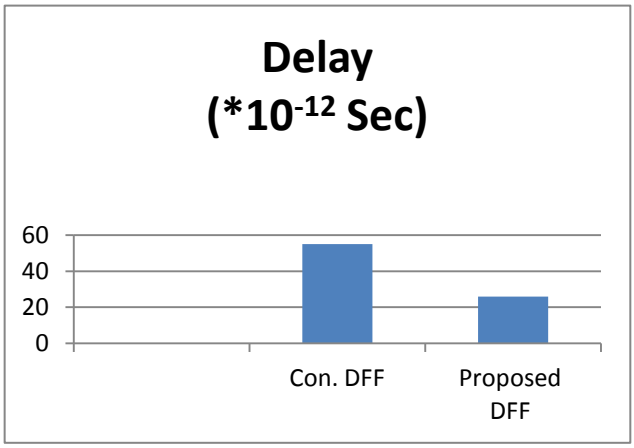

Fig 11a: Comparison of MOSFET and MODFET – Delay

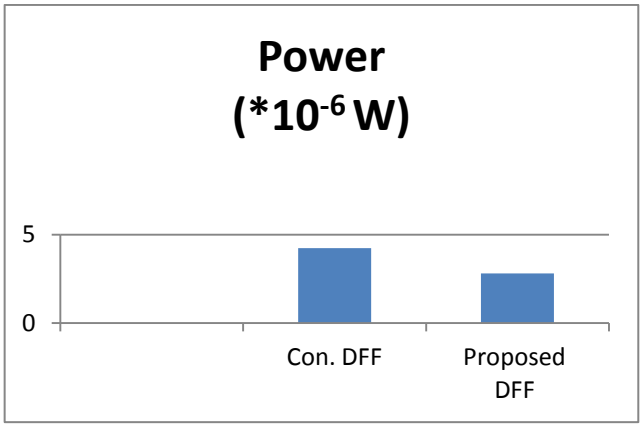

Fig 11b: Comparison of MOSFET and MODFET – Power

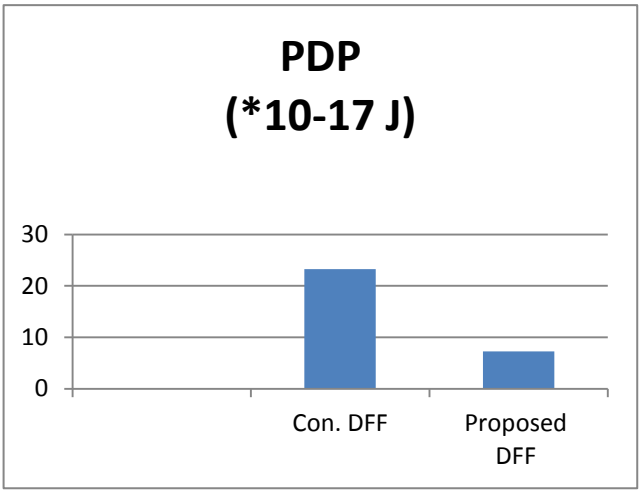

Fig 11c: Comparison of MOSFET and MODFET - PDP

6. CONCLUSION

This paper deals with designed of an efficient RS and D flip flop using AlGaAs/GaAs MODFET technologies. The Flip Flop are simulated in PSPICE with operating voltage of 1V and operating frequency at 1GHz in MODFET and compared the performances. MODFET based flip flop have 55% less power consumption, delay has also decreased and power delay product (PDP) has been reduced 70% than MOSFET design. The rise time and fall time has also been decreased. The MODFET based flip flop are more efficient in average power, delay, power delay product, rise time and fall time. Hence from performance analysis of an RS and D flip flop using MODFET is more efficient for low power and high performance applications.

7. ACKNOWLEDGMENTS

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