CMOS Layout for Low Power Four Bit Adiabatic Binary Multiplier

Sonal Jain
M.TECH*(VLSI DESIGN)
LNCT Bhopal
Madhya Pradesh

Monika Kapoor
Associate Professor
LNCT Bhopal
Madhya Pradesh

ABSTRACT
Due to high complexity of VLSI systems used in various applications power dissipation becomes a limiting factor in VLSI circuits and systems, which arises from its switching activity influenced by the supply voltage and effective capacitance. Charging and discharging of the node capacitances in CMOS circuits creates power dissipation called as dynamic power dissipation .Thus to reduce dynamic power dissipation an adiabatic switching techniques is used in which the signal energies stored on circuit capacitances may be recycled instead of dissipated as heat. This can reduce the power dissipation but requires more number of transistors. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy. Power dissipation is achieved by recovering the energy in the recover phase of the supply clock. Here a four bit digital multiplier is designed through the charge recovery logic and positive feedback adiabatic switching techniques are used for the design of above logic. Here all the gates , half adder , full adder are design using adiabatic switching techniques.

Keywords
Adiabatic logic, Microwind, Multiplication, Energy Recovery, Power Supply

1. INTRODUCTION
A binary multiplier is a basic block of electronic circuit used in microprocessors to multiply two binary numbers. The multiplier segment is design using continuous addition of binary numbers. For this we can design the full adders which is the series connection of two half adder. The half adders are design using XOR, AND, NOT adiabatic gates. A variety of computer arithmetic techniques can be used to implement a digital multiplier.[2][3] Most techniques involve computing a set of partial products, and then summing the partial products together.This process is similar to the method taught to primary school children for conducting long multiplication on base-10 integers, but has been modified here for application to a base-2 (binary) numeral system.In binary multiplication each long number is multiplied by one digit (either 0 or 1), and that is much easier than in decimal, as the product by 0 or 1 is just 0 or the same number. Therefore, the multiplication of two binary numbers comes down to calculating partial products (which are 0 or the first number), shifting them left, and then adding them together (a binary addition):

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     1111
   x 1111
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     1111   (this is 1111 x 1)
    1111    (this is 1111 x 1, shifted one position to the left)
   1111     (this is 1111 x 1, shifted two positions to the left)
+ 1111      (this is 1111 x 1, shifted three positions to the left)
 =========
 11100001   (this is 125 in binary)
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Implementations Older multiplier architectures employed a shifter and accumulator to sum each partial product, often one partial product per cycle, trading off speed for die area. Modern multiplier architectures use the Baugh–Wooley algorithm, Wallace trees, or Dadda multipliers to add the partial products together in a single cycle. The performance of the Wallace tree implementation is sometimes improved by modified Booth encoding one of the two multiplicands, which reduces the number of partial products that must be summed.

Power Dissipation in CMOS circuits
Power dissipation in digital CMOS circuits can be classified into two types: dynamic power dissipation and static power dissipation. Dynamic power dissipation is due to high-to-low and low-to-high signal switching in circuits. Static power dissipation depends on the logic states of the circuit. It does not depend on signal switching. The average power dissipation in a digital CMOS circuit can be given by the following equation

$$Pavg = Psw + Psc + Pleak + Pstatic$$

Where, Psw is the capacitive switching power dissipation, Psc is the short-circuit power dissipation, Pleak is the power dissipation due to leakage currents and Pstatic is the static power dissipation due to non-leakage static currents. Capacitive switching power and short-circuit power are components of dynamic power dissipation. Leakage power is a major component of static power dissipation in CMOS circuits, though there might be some non-leakage currents that contribute to a small percentage of static power dissipation.

Principle of adiabatic switching
The word ***ADIABATIC*** describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. Adiabatic switching can be achieved by charging the capacitor from a time varying voltage source or constant current source. In the on-resistance of the pMOS network, the energy dissipation in conventional CMOS circuits is caused by the channel resistance of the transistor. The dissipation through the channel resistance R is then:

$$Edissipate=PxT=I^2RT=(C_LVdd/T)^2RT$$
$$=(RC_L/T)\ C_LVdd^2$$

Thus we can say that the dissipated energy is smaller than for the conventional case if the charging time T >>2RC and can be made small by increasing the charging time. A portion of the energy thus stored in the capacitance can also be reclaimed by reversing the current source direction, allowing the charge to be transferred from the capacitance back into the supply. Adiabatic logic circuits thus require non-standard power supplies with time-varying voltage, also called pulsed power supplies. All the charge on the load capacitance is recovered by the power supply.

2. PROPOSED METHOD

The parallel multiplier uses combinational; a circuit only and thus operates much faster than serial multiplier. The basic building block of multiplier is full adder block shown in fig 1and its CMOS layout is shown in fig 2. For 4 bit multiplication the total number of full adder (FA) block require are 4x3=12 and the total AND logic gate i.e partial product (PP) requires are 16. The full adder block generates output as sum = A xor b xor c, and Cout= A.B +B.C+A.C.In general the number of full adder required is n(n-1)Each A.B product is realize using AND logic gate. Each output bit is computed by adding the appropriate A.B in the respective column and carries from previous column. The all Logic gates are design by Improved Efficient Charge Recovery (IECRL) adiabatic logic.[4] The circuit becomes low power faster but hardware complexity is also high. To reduce the power dissipation, the circuit designer can minimize the switching event, decrease the node capacitance, reduce the voltage swing or apply a combination of these methods. Yet, in all these cases, the energy drawn from the power supply is used only once before being dissipated. To increase the energy efficiency of the logic circuits, other measures can be introduced for recycling the energy drawn from the power supply.[9] Improved Efficient Charge Recovery Logic (IECRL) IECRL , improves ECRL with the addition of a pair of cross-coupled NMOS devices. This produces a logic family that is based around a pair of cross-coupled inverters, a structure that is identical to the storage elements in a Static RAM (SRAM). The cross-coupled NMOS devices are an improvement over ECRL because they provide a pulldown path to ground that remains even after the charge is recovered from the gates of the evaluation FETs. However, because of the two extra NMOS devices, it will require a larger area in which to be implemented. Figure 3 shows an inverter/buffer (also in buffer configuration) implemented using the IECRL style.

3. RESULT ANALYSIS

The basic building block of multiplier is full adder block shown in fig 1and its CMOS layout is shown in fig 2. For 4 bit multiplication the total number of full adder (FA) block require are 4x3=12 and the total AND logic gate i.e partial product (PP) requires are 16.

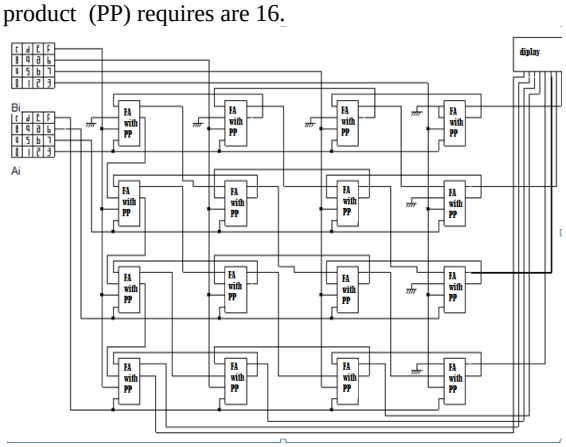

Fig.1 Block diagram for 4 bit multiplier

The cross-coupled NMOS devices are an improvement over ECRL because they provide a pulldown path to ground that remains even after the charge is recovered from the gates of the evaluation FETs. However, because of the two extra NMOS devices, it will require a larger area in which to be implemented.

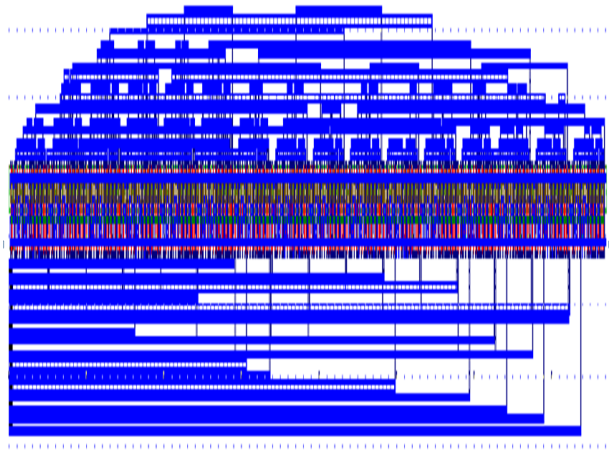

Fig.2 CMOS layout design for 4 bit multiplier

Fig 5 and 6 shows adiabatic Inverter power dissipation from supply to output (1 uW) and maximum current from supply to output (0.130mA).

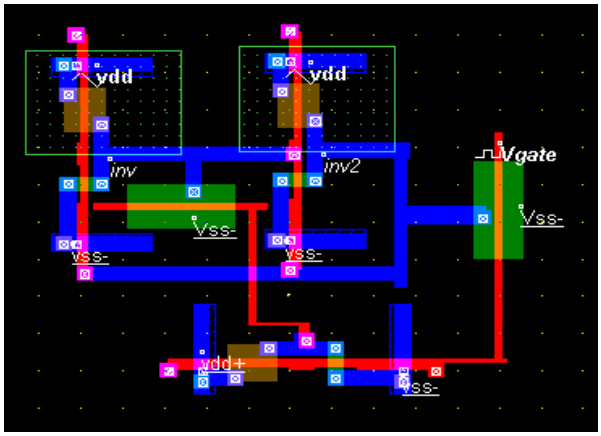

Fig. 3 Adiabatic Inverter logic IECRL

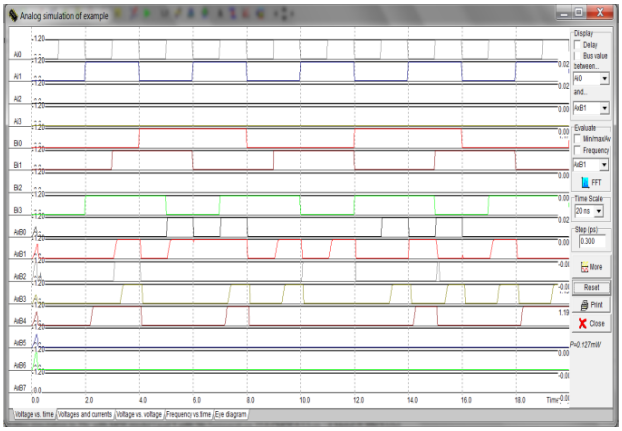

Fig.4 Simulation for 4 bit data multiplication

Table 1: For 16 product multiplier

Paper reference	By Chip Hong Chan Paper publish in ieee transaction oct 2012	By Guoqing Deng and Chunhong Chen publish in ieee transaction 2012	By Ivan Padilla publish in ieee transactio n 2012	Proposes techniques
Number of MOSFET	1008 T	6439 T		1512 T
Power dissipatio n	0.69uW(Pd) +0.392uW(Ps) =1.082uW	250uW	0.48 to 5.28mW	1 nW to 0.4 uW
Optimum supply freq.	10000	-- as standard DC	-- as standard DC	10000 as non standard DC
Delay	3.55ns	45ns	20ns	20ns to 40ns
% power minimiza tion	20.8%	20%	10%	25%

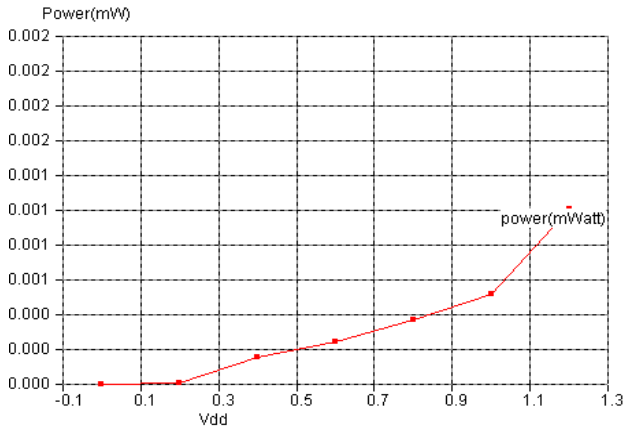

Fig.5 Adiabatic Inverter power dissipation from supply to output (1 uW)

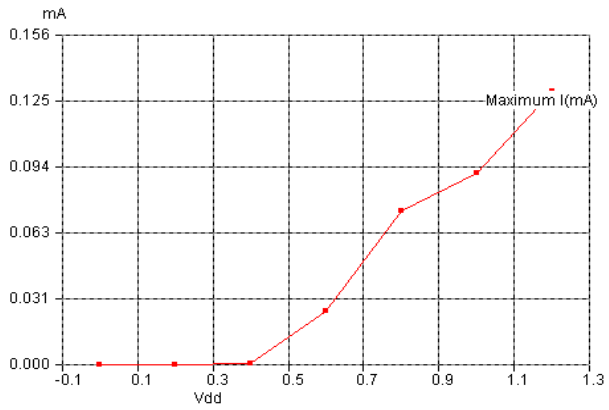

Fig.6 Adiabatic Inverter maximum current from supply to output (0.130mA).

4. CONCLUSION

For 4 bit multiplication the total number of full adder (FA) block require are 4x3=12 and the total AND logic gate i.e partial product (PP) requires are 16.Power reduction is achieved by recovering the energy in the recover phase of the supply clock in the range of nanowatt to microwatt. If input changes from zero to Vdd, the voltage drops abruptly across the load capacitor and ground through NMOS. All the charge on the load capacitance is recovered by the power supply.Adiabatic logic achieves low power by maintaining small potential differences across the transistors while they are conducting, and allowing the charge stored in the output load capacitors to be recycled . The circuit becomes low power faster but hardware complexity is also high.

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