Effect of Supply Voltage on Ability and Stability in IP3 SRAM Bit-Cell at 45nm CMOS Technology using N-Curve

Toshiyanka Goswami[1], Jyoti Yadav[2], Shilpi Birla[3], Neeraj Kr. Shukla[4]
[1,2,4]VLSI Design Group, ITM University, Gurgaon, India
[3]Sir Padampat Singhania University, Bhatewar, Udaipur, India

ABSTRACT
The Leakage power, performance, data retentation, and stability are the key challenges in Static Random Access Memory (SRAM) at Deep-Sub-Micron (DSM) CMOS technology. In the DSM technology, when threshold voltage, channel length, and gate oxide thickness are reduced, leakage currents in deep sub-micrometer regimes causes power dissipation in CMOS digital circuits which may affect the data ability and stability in the SRAM. In this work the effect of supply voltage has been observed in the IP3 SRAM Bit-Cell using N-Curve methodology at the room temperature (RT). To see the effect of supply voltage variations on the stability and ability parameters in the 6T and IP3 SRAM Bit-Cells, the supply voltage has been varied from 0.6V to 1.0V in step of 0.1V. It has been seen that the read, write stability and ability are comparable in both cells at RT. The other design parameters taken from the CMOS technology available on 45nm are as t_{OX} = 2.4 nm, V_{thn} = 0.224 V, and V_{thp} = 0.24 V at RT = 27°C.

Keywords
N-Curve, SRAM, Stability, SINM, SVNM, WTI, WTV.

1. INTRODUCTION
In a high performance System on Chip (SOC), according to the International Technology Roadmap (ITRS) for semiconductors, 90% of the chip-area will be occupied by the memory core by 2014 [1]. This shows an increasing demand for memory in near future. The SRAMs are facing design challenges in order to maintain the sufficient level of cell stability margins and leakage power threats, both in dynamic and standby modes of memory operations due to device scaling. The leakage current (gate leakage and subthreshold leakage) increases when CMOS transistors are scaled down [2][3].

To manage constrained tradeoffs like overall power consumption, performance, stability and area, the SRAMs are designed for specific target applications, e.g., high-end computing, portable multimedia products, implantable biomedical electronics devices, consumer electronics, wireless sensor networks, etc.

In order to keep the overall power consumption low [4], the scaling of supply voltage is one of the popular and effective way [P = (V_{DD}^2)*f] among others power reduction techniques. But the SRAM cell stability also reduces due to supply voltage scaling [5][6].

In this work, the effect of supply voltage on stability in IP3 SRAM Bit-Cell is observed. The IP3 SRAM Bit-Cell has an integrated two sub-cell structures, one for write and other for read operation in the active mode.

This paper presents the introduction in Section-I and a brief outline of the Conventional 6T and IP3 SRAM Bit-Cells in Section II. The Section III discusses about the stability, ability and N-curve technique for Bit-Cell's performance measurement. And the design simulation work is given in Section IV. Finally, the conclusion is presented in Section V.

2. THE 6T AND IP3 SRAM BIT-CELLS
The popular choice of cache memories is the six-transistor Bit-Cell. It has two inverters connected back to back to hold data during standby mode of the memory cell. The two nmos transistors (access transistors) are used to access data (in and out) from the Bit-Cell. The access transistors are switched-ON/OFF with the help of a common Word Line (WL). The data in the bit cell is written through bit lines (BL and BLB) when WL is 'high'. The data is hold (stored) at the memory cell by keeping the WL 'low' and keeping the bit lines at pre-charge state. When the data is to be read from the cell, the WL is made 'high' to discharge the bit line and the data is being sensed by the sense-amplifier [7].

The Improved P3 (IP3) SRAM Bit-Cell has a separate data write sub-cell and a data read sub-cell section [7]. The data write section has dual role of data write and data hold whereas the read sub cell is used to read the data from the Bit-Cell. When the memory is in the standby mode a drowsy voltage (0.35V) is applied to the cell [8][9].

3. STABILITY AND ABILITY MEASUREMENTS USING N-CURVE
In addition to the Static Noise Margin (SNM) which is being drawn from the butterfly curve to comment on the stability of the SRAM Bit-Cell, the N-curve is a latest developed technique which is becoming popular to predict the overall cell stability (read and write stability) and ability (read and write ability).

In Fig.1, A and C are stable points and B is metastable point. The voltage difference between A and B is the maximum DC noise voltage at storage node of the bit cell before the change in content of the bit cell. This voltage difference is known as SVNM (Static Voltage Noise Margin). At SVNM, the maximum current that injects in SRAM cell is called SINM (Static Current Noise Margin) which is negative due to its direction.

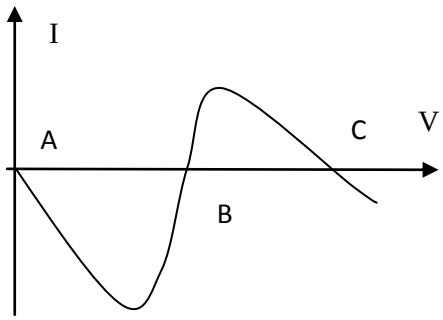

Fig. 1 The N-Curve [10]

In write operation, the bit lines voltage is pulled from V_{DD} to ground to discharge '1'. This voltage difference is shown between B and C which is known as WTV (Write Trip Voltage). At WTV, the amount of current which is needed to write the cell is called WTI (Write Trip Current). Although the cell is having larger SINM but it has small value of SVNM and is stable because value of charge that is to be discharged is large during write operation [10]. The peak between A and B is the measure of the SINM and the peak between B and C is the measure of the WTI.

4. N-CURVE SIMULATION SRAM BIT-CELLS

The design simulation of 6T and IP3 SRAM Bit-Cells is performed at a supply-voltage range variation from 0.6V to 1.0V, in a step variation of 0.1V.

4.1 Static Voltage Noise Margin

As supply voltage is increasing, SVNM is also increasing for both Conventional 6T SRAM Bit-Cell and IP3 SRAM Bit-Cell. The values of SVNM at different supply voltages are approximately equal for both types of Bit-Cells. The variation in SVNM has been seen in an average range of 1.846mV, Fig. 2.

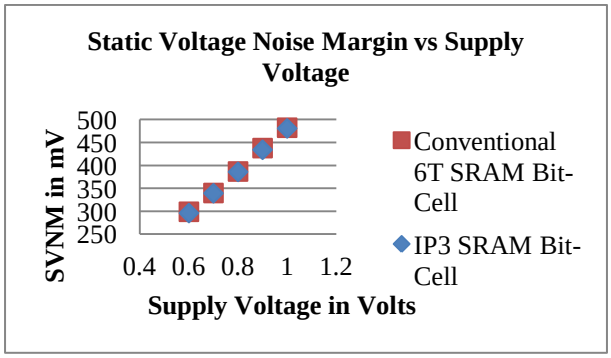

Fig. 2. Static Voltage Noise Margin vs Supply Voltage

4.2 Static Current Noise Margin

The SINM of Conventional 6T SRAM Bit-Cell is increasing exponentially whereas SINM is increasing linearly in IP3 Bit-Cell. The variation occurred in SINM is in an average range of 9.852uA, Fig. 3.

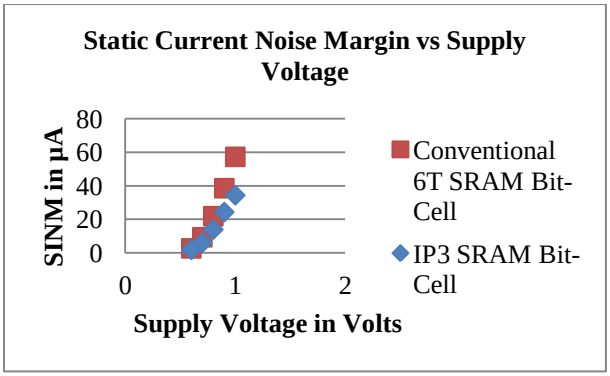

Fig. 3. Static Current Noise Margin vs Supply Voltage

4.3 Write Trip Voltage

Due to increase in supply voltage, WTV of Conventional 6T SRAM Bit-Cell increases linearly. The WTV of IP3 SRAM Bit-Cell shows an average variation of 28.266mV, Fig. 4.

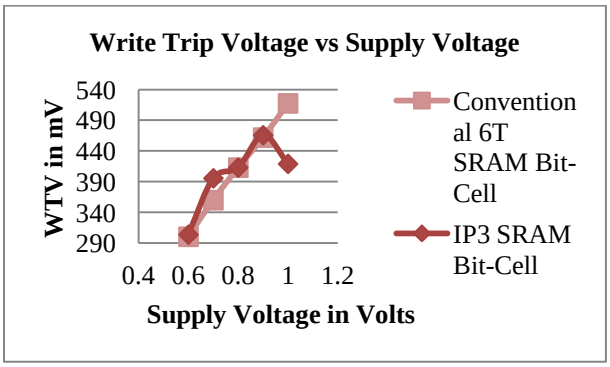

Fig. 4. Write Trip Voltage vs Supply Voltage

4.4 Write Trip Current

As supply voltage increases, WTI of both Conventional 6T SRAM and IP3 SRAM Bit-Cell increases linearly with nearly equal values at different supply voltages. It is observed that variation in WTI is in an average range of 0.133uA, Fig. 5.

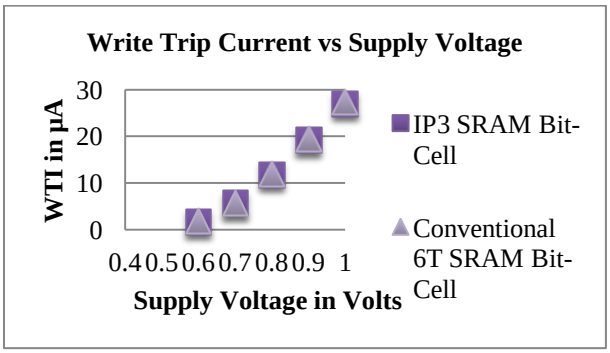

Fig. 5. Write Trip Current vs Supply Voltage

5. CONCLUSIONS

In a supply voltage variation from 0.6V to 1.0V in a step size of 0.1V, the different parameters of stability such as SVNM, SINM, WTV and WTI have been extracted. The maximum tolerable DC noise voltage of IP3 SRAM Bit-Cell is found very close to the Conventional 6T SRAM Bit-Cell and it is within a limit of 0.17% to 0.9%. The Conventional 6T SRAM cell has shown an improved maximum current injection capability of 33% to 40% before the flipping of the content of the cell. The write stability of the IP3 SRAM Bit-Cell is enhanced as compared to Conventional 6T SRAM Bit-Cell. Compared to Conventional 6T SRAM Bit-Cell, a very small variation of 1% to 2% is observed in the current level of the IP3 SRAM Bit-Cell, when both the bit-lines are pre-charged at V_{DD}. This shows that the read stability, readability, and writability of the IP3 SRAM Bit-Cell is comparable to the Conventional 6T SRAM Bit-Cell. The Conventional 6T SRAM has good write stability. Since the power consumption level of the IP3 SRAM Bit-Cell is better as compared to conventional 6T SRAM cell, the IP3 SRAM may be used as a low-power and stability assured bit cell in memory design.

6. ACKNOWLEDGMENTS

The authors are grateful to their organizations for their help and support to carry-out this work.

7. REFERENCES

[1] International Technology Roadmap For Semiconductors 2003. URL: http://www.publicitrs.net

[2] Zhang L.J., Wu C., Ma Y.Q., Zheng J.B. and Mao L.F., "Leakage Power Reduction Techniques of 55 nm SRAM Cells," *IETE Tech. Rev.*, vol. 28, No. 2, pp. 135-145, 2011

[3] Lo C.H. and Huang S.Y., "P-P-N Based 10T SRAM Cell for Low-Leakage and Resilient Subthreshold Operation," *IEEE J. Solid-State Circuits*, vol. 46, No. 3, pp. 695-704, 2011.

[4] Kao K. M., Lee W. C., Liu W., Jin X., Su P., Fung S. K. H., An J. X., Yu B., and Hu C., "BSIM4 Gate Leakage Model Including Source-Drain Partition," *Electron Devices Meeting Conf.*, San Francisco, pp. 815-818,10-13 Dec. 2000.

[5] De V., and Borkar S., "Technology and design challenges for low power and high performance," *Proc. Int. Symp. 1999 Low Power Electronics and Design Conf.*, San Diego, pp. 163–168, 17 Aug. 1999.

[6] Roy K., Mukhopadhyay S., and Mahmoodi-Meimand H., "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits", *Proc. IEEE*, vol. 91, No. 2, pp. 305-327, Feb., 2003.

[7] Singh R. K., Pattanaik M., and Shukla N., "Characterization of a Novel Low-Power SRAM Bit-Cell Structure at Deep Sub-Micron CMOS Technology for Multimedia Applications," Circuits and Systems, *Scientific Research*, vol. 3, No. 1, pp. 23-28, Jan. 2012.

[8] Flautnern K., Kim N.S., Martin S., Blaauw D. and Mudge T., "Drowsy Caches: Simple Techniques for Reducing Leakage Power," *29th Annual Int. Symp. 2002 Computer Architecture Conf.*, Anchorage, , pp. 148-157, 25-29 May 2002.

[9] Kim C.H., Kim J. J., Mukhopadhyay S. and Roy K., "A Forward Body-Biased Low-Leakage SRAM Cache: Device, Circuit and Architecture Considerations," *IEEE Trans. Very Large Scale Integr. (VLSI)Syst.*, vol. 13, No. 3, pp. 349-357, 2005.

[10] Archana Bai, "SRAM Cell Modeling for Read Stability and Write Ability," Int. J. Emer. Tech. Comp. and App. Sci. (IJETCAS), vol. 2, No. 1, pp. 26-31, 2012.

8. AUTHOR'S PROFILE

[1]**Toshiyanka Goswami**, student B.Tech (Completed) at ITM, Gurgaon, in the Electronics & Communication Engineering discipline. Her main area of interest is Semiconductor Materials & Device Modeling, Low-Power Digital VLSI Design, and its Multimedia applications.

[2]**Jyoti Yadav**, pursuing M.tech from ITM University, Gurgaon in VLSI(Very Large Scale Integrated Circuits) discipline and have done B.Tech from Gurgaon College of Engineering for Women, Bilaspur in ECE(Electronics and Communication Engineering). Her main area of interest is Low - Power Digital VLSI Design and its Bio Medical applications.

[3]**S. Birla**, (IACSIT, IAENG), a Ph.D. Scholar at the UK Technical University, Dehradun (Uttarakhand) India is an Asst. Professor in the Department of Electronics & Communication Engineering, Sir Padampat Singhania University, Udaipur (Rajasthan) India. She has received her M.Tech. (VLSI Design) and B.E. (Electronics & Communication Engineering) Degrees from the University of Rajasthan, Jaipur (Rajasthan) India and MITS University, Laxmangarh, (Rajasthan) India, respectively. Her main research interests are in Low-Power VLSI Design and its Multimedia Applications, RF-SiP, and Low-Power CMOS Circuit Design.

[4]**Neeraj Kr. Shukla**, (IETE, IE, IACSIT, IAENG, CSI, ISTE, VSI-India), an Associate Professor in the Department of Electrical, Electronics & Communication Engineering, and Project Manager – VLSI Design at ITM University, Gurgaon, (Haryana) India. He received his PhD from UK Technical University, Dehradun in Low-Power SRAM Design and M.Tech. (Electronics Engineering) and B.Tech. (Electronics & Telecommunication Engineering) Degrees from the J.K. Institute of Applied Physics & Technology, University of Allahabad, Allahabad (Uttar Pradesh) India in the year of 1998 and 2000, respectively. He has more than 50 Publications in the Journals and Conferences of National and International repute. His main research interests are in Low-Power Digital VLSI Design and its Multimedia Applications, Digital Hardware Design, Open Source EDA, Scripting and their role in VLSI Design, and RTL Design.