Noise Sensitivity Analysis of 5 Stages Voltage Controlled Ring Oscillator at nm Technology

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ABSTRACT
In present paper, design of differential ring oscillator using replica bias circuit has been presented. Qualitative analysis of jitter and phase noise of differential ring oscillators in the time and frequency domain is presented respectively which shows great results for the design issues of voltage controlled ring oscillator. The effect of the different number of transistors and their symmetrical arrangement to phase noise and jitter is analyzed. Good agreement between qualitative and quantitative measurements is observed using the cadence virtuoso tool, which is exceedingly applicable in ultra high speed Wi-Fi communications.

Keywords
Ring oscillator, Replica bias, Phase noise and Jitter.

1. INTRODUCTION
In present scenario almost every digital and electronic system shows oscillatory behavior and oscillators have become the most inescapable and unavoidable component of all optical and digital devices and communication systems. Two most commonly used voltage controlled oscillators are conventional LC tank and CMOS based ring oscillators [1]-[4] but CMOS based ring oscillator have great advancement over LC tank oscillator as it had no requirement of inductor on chip and exhibits wide tuning range of frequency of GHz range [5]-[6] and CMOS technology is better in terms of a lesser amount of power expenditure and a broad tuning range of operating frequency [7]-[10]. A block diagram of five-stage single ended ring oscillator is depicted below in Figure 1:

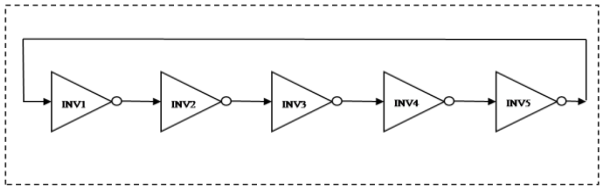

Fig 1: Single ended five stage voltage controlled ring oscillator

The necessary condition to oscillate is unity voltage gain provided that phase shift of 2π, which can be attain by providing π/N phase shift followed by dc inversion [11]. Assuming t_d is the delay of each stage the signal must go through each stage twice to achieve total period of 2Nt_d. Hence oscillation frequency may be given as:

$$\mathbf{f = \frac{1}{2Nt_d}} \quad \textbf{(1)}$$

Where N is the number of stages [8], [12].

Here in this paper we have used the VCO using the differential stages because of the fact that differential output has the property to reduce noise from various sources like from the power supply and common mode noise. This is shown in Figure 2:

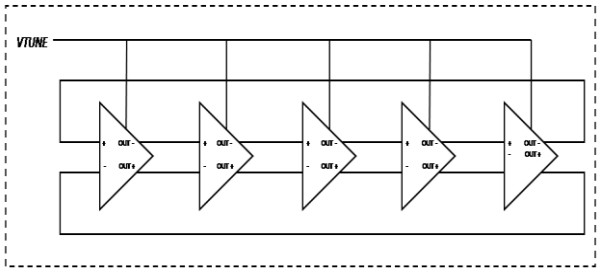

Fig 2: 5 stages differential voltage controlled ring oscillator

VCO has a significant application in PLL devices because of the fact that frequency of oscillation is proportionate to the tail current of the differential rings [13]-[14]. For the most part of any oscillator random perturbations in the output frequency of any circuit be expressed in terms of noise which can mainly rely on phase noise and timing jitter [5], which are directly imparted the timing accuracy in the process of phase alignment[6]-[7] and frequency transitions. Here our approach would give us advantages of cost and size by using fully integrated low noise voltage controlled ring Oscillators[9]-[10] that are being increasingly adapted in many other applications. The aim of this paper is to parallel analysis of phase noise and jitter [11], [12] so that the tradeoff between them can be measured in qualitative as well as in a quantitative manner at 45 nm scale using differential stages. Simulations are done on the cadence virtuoso tool.

2. CIRCUIT DISCRIPTION

2.1 Delay cell
CMOS inverter can be used as a delay element which is cascaded throughout the circuit to provide DC inversion [16]. In this paper the delay cell is designed by the five CMOS transistors. Here we have used Maneates delay cell for the study noise sensitivity analysis of ring oscillator because of the fact that it shows good supply noise rejection and extensively used in phase lock loop and clock generator circuits. A symmetric load transistor pair delay cell is shown below apart of being symmetric load it also uses biasing.

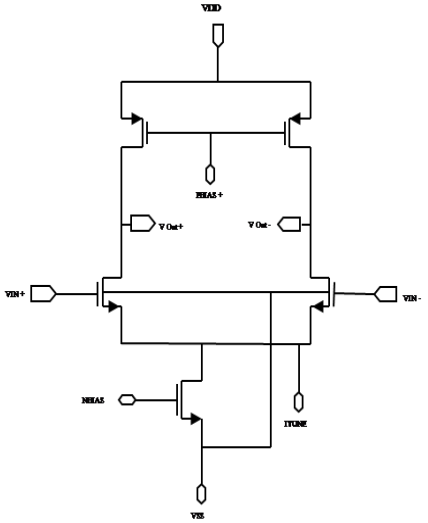

Fig 3: Schematic of the delay cell

2.2 Biasing circuit

A constant biasing scheme is most widely used. In this circuit we have used the more complicated replica biasing scheme because of having the advancement that VCO becomes less susceptible to thermal and other various types of variations [19]-[20] that are made on circuit, it also has the benefit to maintain the Vswing voltage to a constant value. For a high frequency operating region of 2.4 GHz and avoiding the inconsistency of the tuning current to perpetuate the voltage drop constant across current sources a replica bias played a significant role here in our circuit.

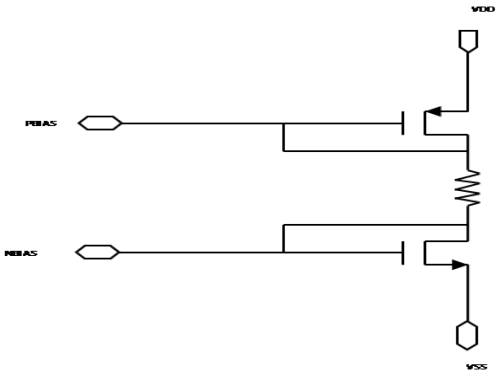

Fig 4: Schematic of biasing Circuit

2.3 Tuning circuit

Tuning circuit is designed here to conserve the effect of frequency variations, Here in present paper we have chosen the tuning voltage range from 0 V to 0.7 V i.e. the corresponding values of $V_{tune}(min)$ = 0 V and $V_{tune}(max)$ = 0.7 V. Gain of Ring oscillator can be given as :

$$A_{vco} = \frac{df}{dV_{tune}} \qquad (2)$$

$$= \frac{f_{max} - f_{min}}{V_{tune}(min) - V_{tune}(max)}$$

$$= \frac{2.4 - 1.88\ (Ghz)}{0 - 0.7\ (V)}$$

$$= - 0.737\ MHz/V$$

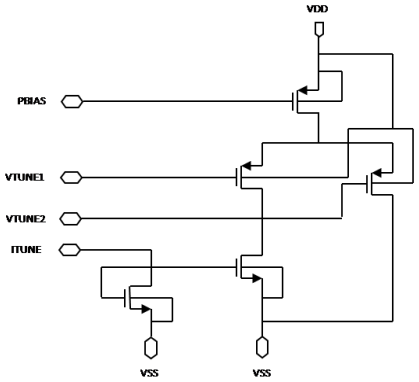

Fig 5: Schematic of the tuning circuit

2.4 Overall circuit design

In this project we have used the 5 stage slow slewing saturated delay cell ring oscillator in cascaded manner with a combination of replica bias and a tuning circuit. A slow slewing saturated delay cell is used here for having a longer gate delay and it is a current based delay cell because deferential source coupled pair is used. The overall circuit with a delay cell, replica bias and tuning circuit is shown below:

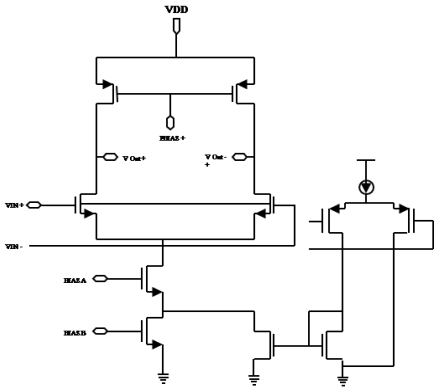

Fig 6: Overall circuit of slow slewing saturated delay cell

According to Barkhausen criterion, the necessary condition for the oscillation of ring oscillator is given by following equations (3) and (4). We can see from here that overall magnitude of loop function must be one and total phase difference must be equal to twice the multiple of π.

$$|A_1(j\omega).A_2(j\omega).A_3(j\omega) \ldots \ldots A_N(j\omega)| = 1 \qquad (3)$$

$$\angle A(j\omega) = \alpha = \arctan(\omega RC) = \frac{2K\pi}{N} \qquad (4)$$

In the case of a linear model of ring oscillator with transconductance parallel loaded of R & C. The gain of stages in inverting mode can be explained as:

$$A_1(j\omega) = A_2(j\omega) = \ldots\ldots = A_N(j\omega) = \frac{-g_m R}{1+j\omega RC} \qquad (5)$$

The resistance of the source coupled transistors can be adjusted by the gate voltage, which is formulated here. It can be seen in fig. (1) That two pmos transistors act as a sub-threshold forward biased diode.

$$R_{sd} = \left(\frac{\partial V_{sd}}{\partial I_{sd}}\right) = \left(\frac{n_p V_t}{I_{sd}}\right)\left(\frac{e^{\left(\frac{V_{sd}}{V_t}\right)} - 1}{(n_p - 1)e^{\left(\frac{V_{sd}}{V_t}\right)} + 1}\right) \quad (6)$$

Gate voltage has an exponential effect on the I_{sd}which is expressed in equation (7) below:

$$I_{sd} = I_0 . e^{\frac{V_{dg} - V_{t0}}{n_p . V_t}} \left(e^{\frac{V_{sd}}{V_t}} - 1\right) \quad (7)$$

For this reason, the resistance has to be tightly controlled while using the current controlled oscillator. So R_{sd} can be adjusted with the application of replica bias feedback controlled gate voltage.

By using the triode equation, we can determine the size ratio (W/L) of any transistor of the circuit presented in Fig. (6):

$$R = \frac{1}{K_p \left(\frac{W}{L}\right)_3 \left(|V_{gs}| - |V_{tp}| - |V_{ds}| \right)} \quad (8)$$

2.5 Phase Noise as a Lorentzian Spectrum

The oscillator's response will be characterized in terms of the phase noise, which describes the response of the oscillator to white and flicker noise sources. Phase noise can be expressed in terms of Lorentzian Spectrum as:

$$£(f) = \frac{1}{\pi} . \frac{\pi f_{osc}^2 k}{(\pi f_{osc}^2 k)^2 + f^2} \quad (9)$$

Where k is a scalar constant that describes the phase noise of the oscillator (in the absence of 1/fNoise and ignoring any noise floor).The Lorentzian spectrum has the property that the total power in £ from minus infinity to plus infinity is 1. This means that phase noise doesn't change the total power of the oscillator, it merely broadens its spectral peak.

2.6 Jitter measurement

The noise of a ring oscillator is commonly characterized in terms of jitter. Generally an ideal ring oscillator shows equal spacing between each transition but practically these transitions are not equal and these undesired perturbations or uncertainties in the timing events are the main cause of Jitter.

Absolute jitter given by the sum of each period variation from the average:

$$\sigma_{abs}(t = N\tau_{avg}) = \sum_{n=1}^{N} \tau_n - \tau_{avg} \quad (10)$$

Different way of measuring jitter is in time domain can be given as:

$$\sigma_{abs}^2(t) = kt \quad (11)$$

3. RESULT AND SIMULATION

In the present paper simulation results have been performed on the cadence simulation tool. Figure 7 shows the transient output of voltage controlled ring oscillator by which we can observe the oscillatory behavior of the circuit.

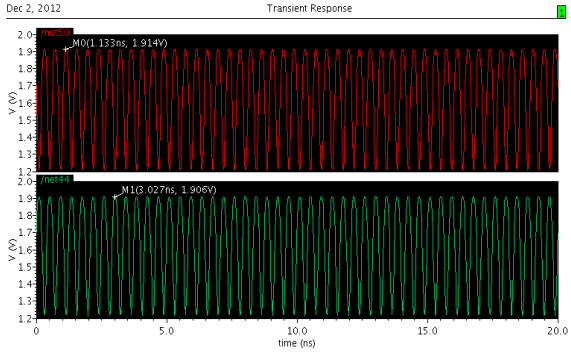

Fig 7: Transient output waveform of VCO at 45 nm. Technology

Figure 8 shows noise response of the voltage controlled ring oscillator. We can see from figure that it shows peak value of 1.008P10^{-14} at .7v supply and 400m Hz frequency.

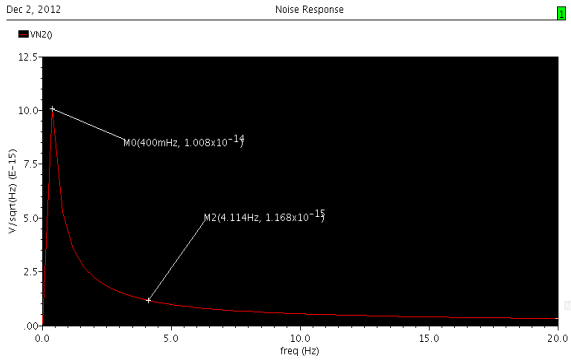

Fig 8: Noise response of VCO (45 nm. technology)

Figure 9 shows output noise of ring VCO measured at .7v supply voltage which shows its peak value at 400 mHz frequency as 31.75 µV/sqrt (Hz) and further reduces as the frequency increases.

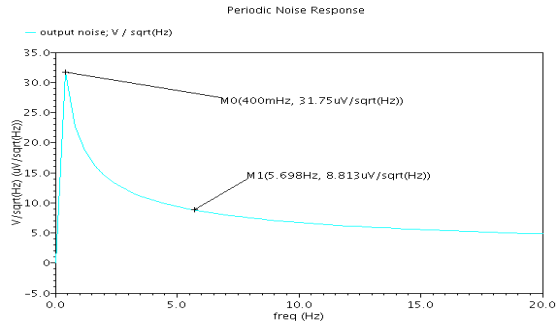

Fig 9: Output noise response of VCO (45 nm. technology)

Figure 10 shows noise figure response of ring VCO measured at .7v supply voltage. Noise figure (NF) is the measure of degradation of the signal-to-noise ratio (SNR), caused by components in signal chain. It is a number by which the performance of a signal receiver can be specified. Here the

performance of signal receiver holds good values up to the range of 2.4 GHz frequency.

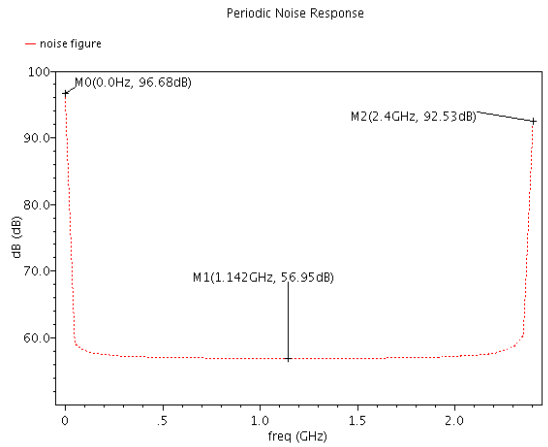

Fig 10: Noise figure (45 nm. technology)

Figure 11 represents the output waveform of timing jitter of the ring oscillator circuit by which low jitter design can be formed.

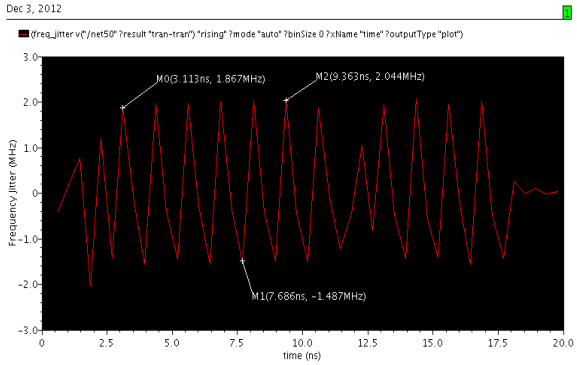

Fig 11: Timing jitter waveform of Ring VCO (45 nm. technology)

Table 1. Noise sensitivity analysis of Ring VCO at varying frequency

Frequency	Output noise(μV/sqrt(Hz))	Pnoise (dB/Hz)
0.4Hz	31.75	7.963
6.954Hz	7.942	20.69
10.00	6.354	23.72
15.00	5.126	24.58
20.00	5.124	25.11

Table 2. Jitter analysis of Ring Oscillator in time domain

	Frequency (MHz)	Jitter (ns)
Delay Cell	1.231	2.413
	1.867	3.113
	1.964	3.557
	2.044	9.363

4. CONCLUSION

Analysis of the jitter and phase noise of single-ended and differential delay cells was presented. The effect of the frequency variation and their effect on the phase noise and jitter are analyzed. Explicit expressions were analyzed to provide a simple, direct means of relating phase noise and jitter performance for qualitative and quantitative measurement.

5. ACKNOWLEDGEMENT

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