Design and Performance Estimation of low Power Frequency Divider in 45nm CMOS Technology

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ABSTRACT
This paper presents a low power low voltage CMOS frequency divider using power gating technique, that's why it reduces the overall power consumption of circuit and increases the efficiency of circuit. This paper demonstrate various parameters and shows reduced leakage power ($0.45*10^{-12}$), Delay (6.26 psec) and noise margin (11.53 dB) of the circuit to analyze its performance in 45nm technology with power gating technology. The simulation results were done with cadence tool virtuoso environment at room temperature 27ºC with various supply voltage ranges (0.7 to 1.2 V).

Keywords
Frequency divider, power gating technique, leakage power, Delay, Noise margin.

1. INTRODUCTION
Frequency dividers are useful circuit in many communication applications for example frequency synthesizers, Timing Recovery circuits and clock generations. It also works functional in many communication applications. The approaching of frequency divider CMOS technologies for high-speed applications has established in numbers of circuits. Low-voltage and power operation of CMOS dividers makes them attractive integration of communication system. Common prototype for dividers are static, Dynamic, injection locked and regenerative frequency divider. Injection-locked frequency divider employs an oscillator with center tape frequency is locked to harmonic incoming signal frequency. Dynamic and injection-locked dividers can achieve high frequencies and low power, they have a narrow frequency ranges. Static dividers with inductive peaking have also been shown to achieve higher frequencies, but they require large inductor area. The ½ frequency dividers are form two D latches in master slave configurations with negative feedback. This paper focus the design of frequency divider that can be applied toward massively parallel I/Os, which imparts broad frequency ranges, area, and power, are key criteria. [3,4]. Wireless communication industry currently experiencing tremendous growth in Wireless LAN application, IEEE 802.11 multiple standards has widely adopted in short-range communication [1,4]. The frequency synthesizer saretypically forms a Phase-Locked Loop (PLL), it is a major and critical component of a wireless transceiver, because it operates at high frequency consumes large portion of total power in the transceivers. Several different standards operation of 2.4 GHz 802.11b/g, 5.2 GHz 802.11a/ HIPERLAN-2 network, thus, multi-standard frequency synthesizer are desired in operation under different wireless system. Numerous research pains have carry out in multi-band multi-standard receivers [3-9]. Performance while power consumption and channel selection of frequency synthesizers are limited by two important building blocks, namely frequency dividers and voltage-controlled oscillators (VCO). The fractional-N frequency synthesizer has used to achieve high resolutions. Recently battery operated wireless communications has been popular for many application. Totrim down battery size, the power consumption of PLL, consumes the largest amount of power in wireless front end, needs to reduce. Injection-locked divider (ILD) uses output frequency of oscillator and modulated with a frequency mixer this realizes high operations of frequency along with low power consumption [2-3]. On other hand HILDs using a ring oscillator instead of an LC resonator [4,5] consume relatively large amount of power but exhibit narrow locking range. The frequency band further than 100 GHz is roughly located at the lower end of the THz frequency band (0.1THz-10THz).This frequency has been applied to various fields of bio-chemical detection, imaging, radio astronomy, plasma diagnostics, radar, remote sensing and so forth. This band is attracting increasing attention for communication application as the demand for high speed data communication keeps increasing. The paper carried out with power gating technique synchronies in circuit through which low power consumption and controlled leakage has been introduced into frequency divider circuit.

2. CIRCUIT DESCRIPTION

2.1 Frequency Divider
Tspc based divider topology is based upon the D type Flip-Flops. It was firstly projected by Yuan & svensson in 1989.This require only one clock phase and having nine transistors, due to small number of transistor and small delay of D to 'out' the operational frequencies can chosen to high ranges. Tspc dividers This paper presents a low power low voltage CMOS frequency divider using power gating technique, that's why it reduces the overall power consumption of circuit and increases the efficiency of circuit. This paper demonstrate various parameters and shows reduced leakage power (0.45×10^{-12}), Delay (6.26psec) and noise margin (11.53) of the circuit to analyze its performance in 45nm technology with power gating technology. The simulation results were done with cadence tool virtuoso environment at room temperature 27ºC with various supply voltage ranges (0.7V to 1.2V)

Tspc based divider are suitable structural design for divider as compared to static dividers when working over high frequency. Conversely Tspc requires input clock having nearly rail to rail voltage hang, this makes an order to achieve high frequency operations. Operation of Tspc D-type Flip-flop is also follow and consists two working nodes evaluation mode,Hold mode. When clk is at high the D type Flip-flop works as evaluation mode if node a is at high the transistor mn1,mn2 are turned on. Node n0 will be pulled low and output 2 becomes high. If node n0 is low the transistor mn1 is

turned off & node n1 which previously is pre-charged remains high. Thus the state of outB becomes low. Therefore node n0 transparent to node output out B becomes evaluation mode. When clk is at low D type Flip-flop work in hold mode namely precharged mode. Node n1 is pre-charged to high through, transistors mn2 & mn3 are off the value of outB is held. Fig explains the working of divide by two circuits which have clk input as output of previous stage and output being feedback to D as input. As the value of node 1 is inverted to value of input D when data is at node, it is transmitted to outB in evaluation mode. The data is at outB and becomes inverted to value of input D. when output node of outB is feedback to the node D outB will toggle to its own state after two clock of cycles.

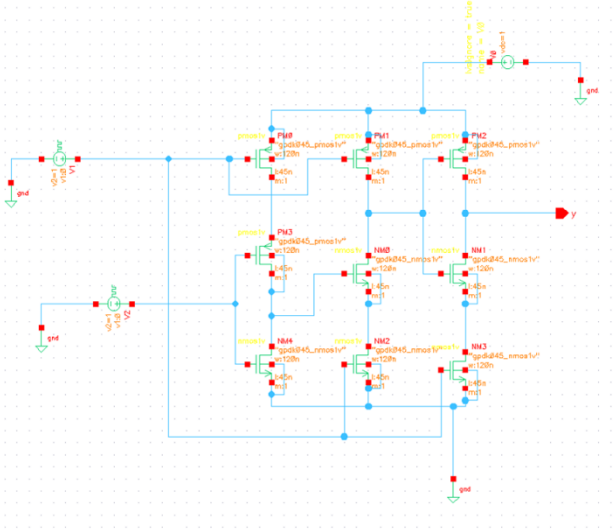

Figure 1. Tspc based frequency divider

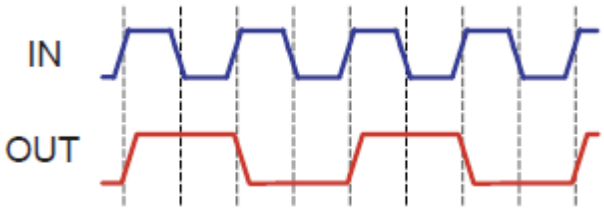

Figure 2. Waveform of Tspc based frequency divider

2.2 Power gating technique

Many vendors in low power embedded products are now including power gating capability in form of sleep mode it typically operate under software control [12] [15]. When operating system sense long idle loop one of several processors cores continue to run at maximum operating frequencies, as the other cores are power gated off [17].

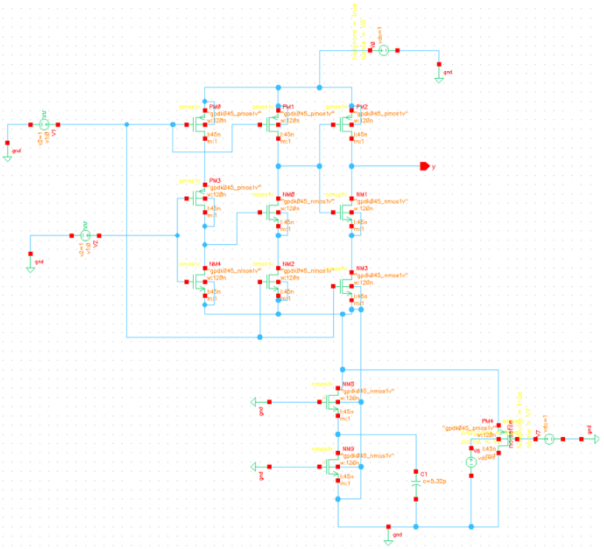

Figure 3. Tspc based frequency divider with power gating technique

By turning sleep transistor off during sleep period, conversely all internal capacitive nodes of logic block and virtual VDD node is discharge at steady state value near ground (Gnd). During power mode transition an instant charge current passes through sleep transistor, its operating saturation regions and creates current surges elsewhere. Since of itself inductance of the off chip bonding wires and the parasitic inductance inherent to the on chip power rails, due to these surges results in voltage fluctuation in the power rails. If magnitude of voltage drop is greater than noise margin of circuit, the circuit may erroneously latch to wrong value or switch at wrong time. In active mode sleep transistors in power-gating structure operates in linear region, at which it modeled by resistor active. This generates small voltage drop Vvgn equal to *i*active × *r*active, where *i*active is the total current demand of logic block operating in active mode. The voltage drop reduces the gates drive capability from Vdd to Vdd/V Gnd and increases threshold voltage of NMOS pull-down device due body effect. Both affect speed of circuit, that's why sleep transistor should not be small. In supply mode sleep transistor operate at cut-off region and may be modeled by an open switch. In this mode, the sleep transistor limit leakage current, except internal capacitive load connected to Vgnd node through NMOS pull down device are charged up to steady-state value near Vdd.

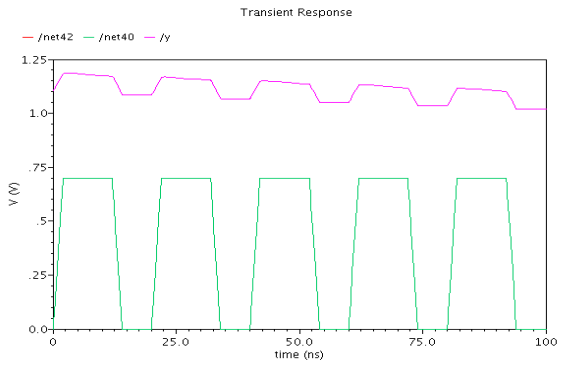

Figure 4. Wave form of Tspc based frequency divider with power gating technique

If the sleep transistors are abruptly turned on all the charge are trapped in internal capacitive node and the Vgnd node discharge rapidly through switched NMOS pull down path of logic blocks and sleep transistors. For that time the sleep transistors operate in saturation region and may be modeled by current source. The current that flows through sleep transistors at this situation are much larger than active-mode current Iactive and this current surge induce voltage fluctuation in power distribution networks.

3. SIMULATION RESULT

The circuit work simulated in cadence for 45nm technology from the result table, we are getting effective and average reduction result in delay, leakage power and noise margin with power gating technique as compare to basic TSPC frequency divider design technique

3.1 Leakage power

In frequency divider either the transistors are in off mode or in ON mode due to switching of opposite level leakage is introduced into devices. The power consumption in frequency divider consume a power off 1.66nw power gating technique power consumes is 5.16nw then, we finally getting the average result of frequency divider with power gating technique at 0.45pw so we achieved a power reduction of (0.45×10^{-12}), this shows more power reduction in comparison to power gating at 45nm technology, so from this we analyses a power reduction of 24% using power gating technique with frequency divider. It can also be observed through varied supply voltage as shown in comparison table below

$$P_{leackage} = I_{leakage} \cdot v_{dd} \qquad (1)$$

Where, $I_{leakage}$=leakage current and V_{dd} = power supply.

Table 1 leakage power

Voltage	Leakage power of frequency divider	Leakage power of frequency divider with power gating technique
0.7 V	0.81 nW	0.45 pW
1 V	1.29 nW	12.88 pW
1.2 V	8.64 nW	35.2pW

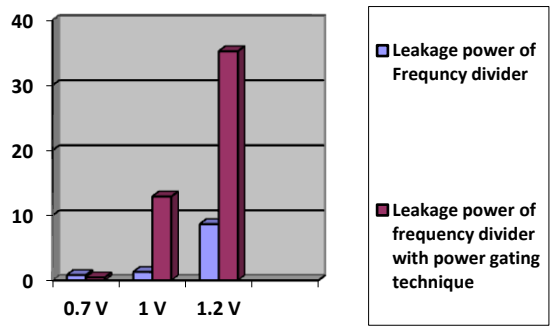

Figure 5. Delay analysis of frequency divider and frequency divider with power gating technique

The leakage power is calculated by this formula and we calculate the effective power in frequency divider with power gating technique (0.45×10^{-12}) with supply voltage vdd= 0.7V

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3.2 Delay

The time difference between the input increasing the reference voltage and output changing the logic state is known as the propagation delay, propagation delay time of frequency divider generally varies as a function with amplitude of input a larger input will result in a smaller delay time. Delay time of the circuit is measured as the average of response time of gate for positive, negative output transition of sine wave. The comparative analysis of various circuit delay time is shown below. Delay will reduce when the voltage is increased, the main goal of using the frequency divider in our project, that we can set the threshold limits as per our requirement. In this we observe that power gating based frequency divider gives a better performance as compared to power gating frequency divider, due to lower threshold voltage of frequency divider, we also observe that the signal rise and fall time lower provides fast signal propagation and less delay in 45nm technology

The Delay of the through during a signal transition is given as;

$$\text{Delay} = 0.69\ R_{eq}\ X\ C_L \qquad (2)$$

Where in above equation R_{eq} is the resistance that is implemented using the feed through cell and C_L is the load capacitance.

Table 2 Propagation Delay

Voltage	Delay of frequency divider	Delay of frequency divider with power gating technique
0.7 V	5.69 nsec	6.26 psec
1 V	9.23 nsec	36.95 psec
1.2 V	14.54 nsec	42.87 psec

Propagation delay of frequency divider respectively (5.69 nsec) and with power gating technique have used delay is (6.26psec.).

3.3 Noise margin

The voltage difference between the graduate output level and the required input voltage level of a circuit is known as noise margin and we get the effective result with power gating technique as compare to conventional frequency divider, which is show below through the comparative analysis.

4. CONCLUSION

Proposed Frequency divider is modified by using transistors having less average power consumption with decreases in area, delay is also decreased by using only six PMOS as because delay is more concentrated to PMOS due to less mobility of holes compared to electrons, power gating based Frequency divider is created by using transistor and have better performance than the Frequency divider as there are fewer transistor counts by which area is reduced and delay is

also reduced; the average power consumption of the proposed Frequency divider is less in comparison to the conventional Frequency divider, measured result correctly verified the principle of operation and characteristic of the low-power Frequency divider circuit. The circuit has been used for the design of low power.

5. ACKNOWLEDGMENTS

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