Analysis and Implementation of Modified Feedthrough Logic for High Speed and Low Power Structures

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ABSTRACT
In this paper, the design of a low power and high performance dynamic circuit using a new CMOS domino logic family called feedthrough logic is presented. The need for faster circuits with low power dissipation has made it common practice to use feedthrough logic. The proposed circuit for low power improves dynamic power consumption as compared to the existing feedthrough logic and improves its speed. The proposed circuit is simulated using 90nm with power supply 0.9 V CMOS process technology from Cadence(R) Virtuoso(R). Exhaustive simulation results in Cadence environment be evidence for that the proposed modified FTL structure has an advantage in reduction of the dynamic power approximately by 55% and accomplish a speed up to 45% on 8-bit ripple carry adder in contrast to existing feedthrough logic.

Keywords
CMOS digital integrated circuits, CMOS logic circuits, Feedthrough logic (FTL), High-speed arithmetic circuits, Low-power arithmetic circuits

1. INTRODUCTION
The need for high performance and portable devices increasing day by day. Rapid growth in VLSI technology enhancing all these features from generation to generation. The brisk increase in this semiconductor technology leads the feature sizes to be shrinking by using deep-submicron processes.

Continuous technology scaling and increased frequency of operation of VLSI circuits leads to increase in power density which raises thermal management problem. Therefore design of low power VLSI circuit technique is a demanding task without sacrificing its performance. This paper presents the design of a low power dynamic circuit using a new CMOS domino logic family called feedthrough (FTL) logic. Dynamic logic circuits are more noteworthy because of its faster speed and lesser transistor requirement as compared to static CMOS logic circuits. The need for faster circuits force designers to use FTL as compared static and domino CMOS logic and the requirement of output inverter for cascading of various logic blocks in domino logic are eradicated in the proposed FTL designs.

FTL logic has advantages over the conventional logics like design litheness, usage in domino like cascaded stages, differential style, and multiple output logic with iterative networks. It can also be pipelined with fast dynamic latches.

The dynamic power dissipated in a standard CMOS digital gate is given by [8]

$$P_{dynamic} = V_{dd}F_{clk}\sum_i V_{i\,swing}\, C_{iload}\alpha_i \quad \text{.....[1]}$$

Where V_{dd} is the supply voltage, F_{clk} denotes the system clock frequency, $V_{i\,swing}$ is the voltage swing at node i, $C_{i\,load}$ is the load capacitance at node i, α_i the activity factor at node i.

This paper presents the design of modified FTL structure which further reduces the dynamic power consumption of the existing FTL structures [5]. In order to prove the usefulness of the proposed modified FTL structure, an 8-bit RCA is designed and all the existing and modified FTL logics have been implemented on it, and these circuits are simulated on Cadence(R) Virtuoso(R) in 90nm with power supply 0.9V.

The paper is organized as follows: FTL principle of operation is explained in section 2. Proposed modified FTL is explained in section 3. Simulation results and comparisons are shown in section 4. The conclusions are specified in section 5.

2. FTL PRINCIPLE OF OPERATION
The basic structure of a FTL gate is shown in Fig. 1(a) . It consists of an nMOS logic network (nMOS block), an nMOS transistor (T_r) for resetting the output node to low logic level, together with a pull up pMOS load transistor (T_p). T_r and T_p are controlled by the clock signal (Ø)[5].

The basic principle of operation of a FTL circuit in CMOS was available [9] and is explained here. During the high phase of clock (reset phase), the FTL output node is pulled to ground (GND) through T_r where as when clock goes low (evaluation phase),T_r is turned off, and the output node in the interim evaluates to either high or low logic levels. If the logic network evaluates to high, node out is pulled up toward V_{cc}, else it will be pulled down to ground. Since in FTL the output is reset to low, the call for inverters to restore the polarity of the output node is eliminated.

When the clock signal falls, the outputs of the cascaded gates begin to rise to the gate threshold voltage V_{TH}. At this voltage point FTL is differentiated from other logic families as all gates in the circuit are in a high gain point. At this point any small variation in the input nodes would cause a fast variation of the voltage at the output node, whereas in other logic families the inputs need to cross the threshold voltage to begin transition. Moreover, in FTL when the valid inputs to a gate are asserted, the gate outputs need only make a partial transition from V_{TH} to V_{OH} or V_{OL}. The higher speed of FTL is due to the reduction in both low-to-high and high-to-low propagation time delays.

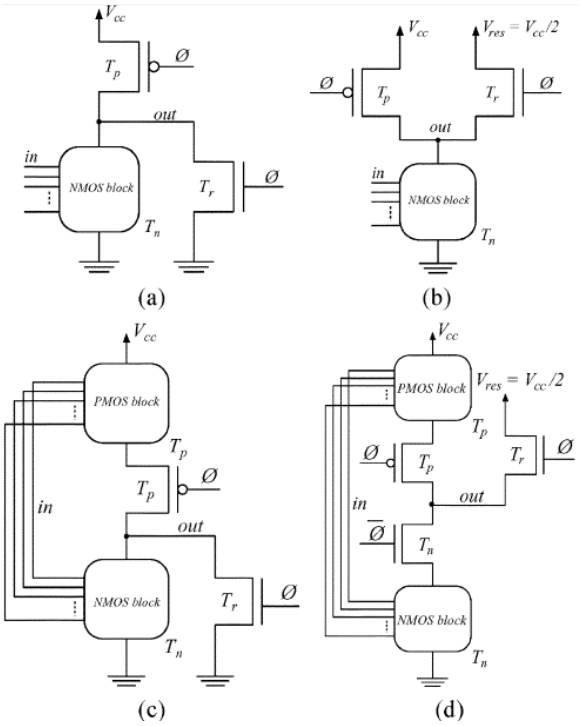

Fig. 1. FTL structures. (a) HS0: high-speed structure with V_{res} = 0.(b) HS06: high-speed structure with V_{res} = V_{cc} /2. (c) LP0: low-power structure with V_{res} = 0. (d) LP06: low-power structure with V_{res} = V_{cc} /2 [5].

3. Modified FTL Structures

The dynamic power consumption of FTL structures is improved by the modified circuit shown in Fig. 2 The high speed structures are modified by placing a pMOS transistor between the logic block and power supply as shown in fig. 2(a) and 2(b). Normally the total power supply is applied to the logic block. Instead of that reduced power supply is applied to the logic block in proposed method by placing pMOS transistor between the power supply and the logic block. This results in average power reduction by square law dependency of V_{DD}. By using modified FTL circuit the delay can also be reduced for low power applications (standard fully complementary) as shown in fig. 2(c) and 2(d).

In this approach, an nMOS transistor is kept between the logic block and power supply. This nMOS acts like Gate way for power supply to the logic block. In active mode the transistor is on, it provides some resistance by which it reduces power supply applies to the basic block which outcome in reduction of average power. In inactive mode this nMOS will be kept off by which the logic block is gets cut off from the power supply. This leads to reduction in the leakage power.

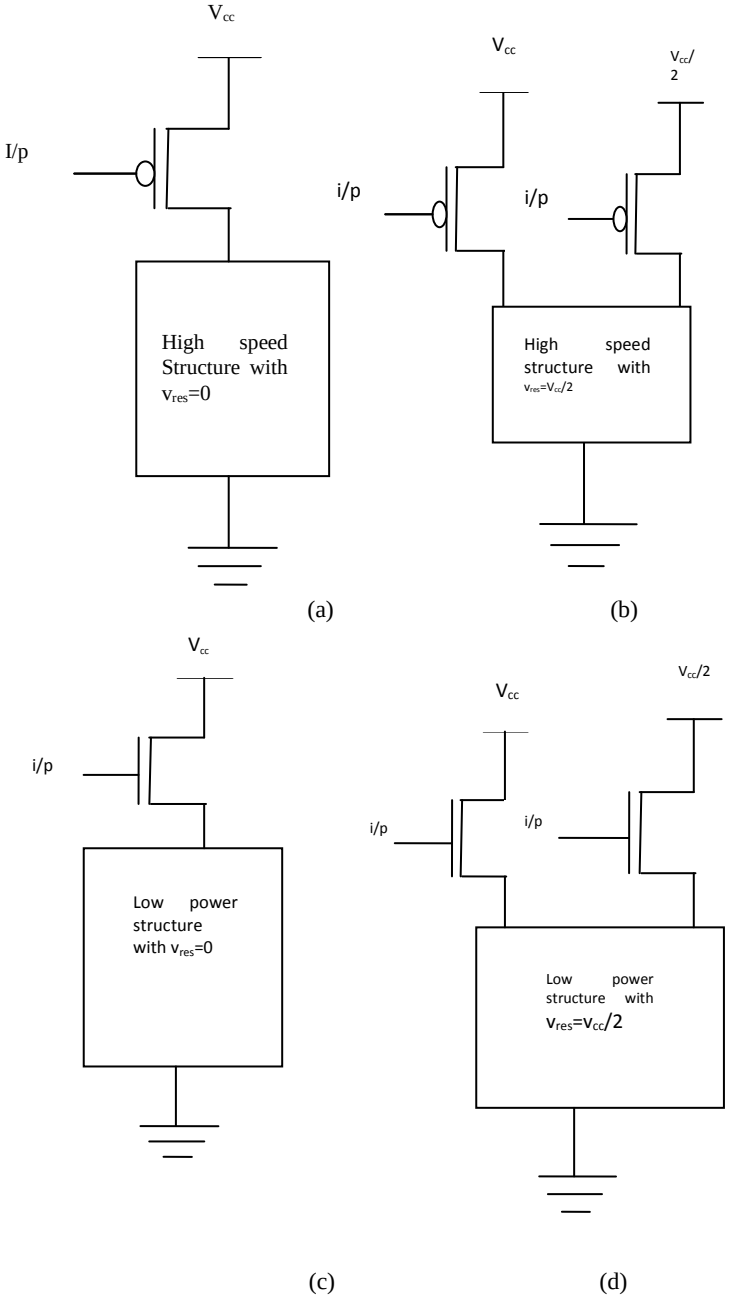

Fig.2. Modified FTL structures. (a) HS0: high-speed structure with V_{res} = 0.(b) HS06: high-speed structure with V_{res} = V_{cc} /2. (c) LP0: low-power structure with V_{res} = 0. (d) LP06: low-power structure with V_{res} = V_{cc} /2.

4. Simulation results and comparison

In this paper, the circuits are simulated in Cadence(R) Virtuoso(R) 90nm CMOS technology model library. Power supply V_{DD} is constant for all simulations and is equal to 0.9 V. Circuits are simulated in spectre simulator. To compare the proposed structure against the existing FTL structure in, the behavior of an 8-bit ripple carry adder is simulated. A full adder is designed by using basic sum and carry cell.

The values of dynamic power consumption, propagation delay time (Tp) and power delay product (PDP) of existing FTL structure are shown in Table I.

Table I: SIMULATION RESULTS FOR POWER, DELAY AND POWER DELAY PRODUCT FOR AN 8-BIT RIPPLE CARRY ADDER DESIGNED BY EXISTING FTL

Method	Total Power (µw)	Delay (n sec)	Power* Delay (µw sec)
CMOS	14.3780	49.76539	0.7155306
HS0	385.2689	21.96818	8.4636585
HS06	454.7078	15.22987	6.9129626
LP0	8.56791	27.81077	0.2382802
LP06	10.87623	44.87018	0.4880185

The values of dynamic power consumption, propagation delay time (Tp), and power delay product (PDP) of modified FTL structure are shown in Table II.

Table II: SIMULATION RESULTS FOR POWER, DELAY AND POWER DELAY PRODUCT FOR AN 8-BIT RIPPLE CARRY ADDER DESIGNED BY MODIFIED FTL

Method	Total. Power (µw)	Delay (n sec)	Power* Delay (µw sec)
CMOS	14.3780	49.76539	0.7155306
HS0	76.92036	24.24453	1.864898
HS06	82.23047	18.688810	1.536789
LP0	3.225122	16.30336	0.052580
LP06	3.75182	30.837288	0.1156961

With respect to the existing FTL structure the proposed FTL structure provides 55% reduction in dynamic power and achieves a speed up to 45% .

5. CONCLUSIONS

This paper proposes a novel low power dynamic circuit. The simulation for an 8-bit ripple carry adder is carried out in this work. The proposed circuit when compared with the existing FTL scheme has set 55% reduction in dynamic power consumption and attains a speed up to 45%. The proposed modified circuits can be used for design of various low-power or high performance logic circuits as per obligation.

6. ACKNOWLEDGMENTS

The CADENCE TOOLS were procured for this project under Research Promotion Scheme (RPS) from AICTE. We express our gratitude to AICTE for the RPS funding

7. REFERENCES

[1] S. M. Kang, Y. Leblebici, CMOS Digital Integrated Circuits: Analysis & Design, TATA McGraw- Hill Publication, 3e, 2003.

[2] J.M. Rabaey, A. Chandrakasan, B. Nikolic, Digital Integrated Circuits: A Design perspective 2e Prentice-Hall, Upper saddle River, NJ, 2002.

[3] R.K. Krishnamurthy, S. Hsu, M. Anders, B. Bloechel, B. Chatterjee, M. Sachdev, S. Borkar, "Dual Supply voltage clocking for 5GHz 130nm integer execution core," proceedings of IEEE VLSI Circuits Symposium, Honolulu, pp. 128-129, June 2002.

[4] S. vangal, Y. Hoskote, D. Somasekhar, V. Erraguntla, J. Howard, G.Ruhl,V.Veeramachaneni, D. Finan, S. Mathew, and N. Borkar, "A 5-GHz floating point multiply-accumulator in 90-nm dual VT CMOS," in Proc. IEEE Int. Solid-State Circuits Conf., San Francisco, CA, pp. 334–335, Feb.2003.

[5] V. Navarro-Botello, J. A. Montiel-Nelson, and S. Nooshabadi, "Analysis of high performance fast feedthrough logic families in CMOS," IEEE Trans. Cir. & syst. II, vol. 54, no. 6, pp. 489-493,Jun.2007.

[6] J. L. Rossello, C. de Benito, and J. Segura, "A compact gate-level energy and delay model of dynamic CMOS gates," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 52, no. 10, pp. 685–689, Oct. 2005.

[7] S. Nooshabadi and J. A. Montiel-Nelson, "Fast feedthrough logic: A high-performance logic family for GaAs," IEEE Trans. Circuits Syst.I, Reg. Papers, vol. 51, no. 11, pp. 2189–2203, Nov. 2004.

[8] K. Navi, V. Foroutan, M. Rahimi Azghadi, M. Maeen, M. Ebrahimpour, M. Kaveh, O.Kavehei, "A Novel low power full-adder cell with new technique in designing logical gates based on static CMOS Inverter," ELSEVIER Microelectronics Journal, Vol.40, (2009), 1441–1448.

[9] V. Navarro-Botello, J. A. Montiel-Nelson, and S. Nooshabadi, "Low power arithmetic circuits in feedthrough dynamic CMOS logic," in Proc. 49th IEEE Int. Midwest Symp. Circuits, Syst. (MWSCAS'06), San Juan, Puerto Rico, August 2006.

[10] V. Navarro-Botello, J. A. Montiel-Nelson, and S. Nooshabadi, "Fast Adder Design in Dynamic Logic" in IEEE Trans. Circuits Syst. 2007.