Analysis of Leakage Power Reduction Techniques for Low Power VLSI Design

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ABSTRACT
Power dissipation has become one of the major concerns of VLSI circuit design with the rapid launching of battery operated applications. In high performance designs, the leakage component of power consumption is comparable to the switching component. This percentage will increase with technology scaling unless effective techniques are introduced to bring leakage under control. In this paper, an 8X8 multiplier is designed using different leakage power reduction techniques like MTCMOS, DUAL-V_t and LECTOR. All the above mentioned techniques are simulated using Cadence virtuoso tool in 90nm technology.

Keywords
8X8 multiplier, MTCMOS, DUAL-V_t, LECTOR, Proposed methods

1. INTRODUCTION
The rapid increase in semiconductor technology led the feature sizes to be shrinking by using deep-submicron processes. System on a chip (SoC) is an integrated circuit that integrates complex functions on a single chip. In the growing market of mobile hand-held devices used all over the world today, the battery-powered electronic system forms the backbone. To maximize the battery life, the tremendous computational capacity of portable devices such as notebook computers, personal communication devices (mobile phones, pocket PCs, PDAs), hearing aids and implantable pacemakers has to be realized with very low power requirements. With miniaturization and the growing trend towards wireless communication, power dissipation has become a very critical design metric. The longer the battery lasts, the better is the device.

With the advancement in technology, static power dominates dynamic power. Leakage currents are especially important in burst mode type integrated circuits where most of the time the system is in an idle, or sleep mode. No computation takes place during sleep mode [1]. For example, a cell phone will be in the standby mode for most of the time where the processor is in idle state. With the large leakage currents during the idle mode power will be continuously drained with no useful work being done.

Many techniques have been proposed [2] to minimize these leakage currents in nanometer technology. Excessive power dissipation in portable devices causes overheating, reduces chip life, functionality and degrades performance. Minimizing power consumption is therefore important and necessary, both for increasing levels of integration and to improve reliability, feasibility and cost.

2. 8 BIT CARRY-SAVE MULTIPLIER
The basic principle involved in multiplication is the evaluation of partial products and accumulation of shifted partial products. In order to perform this operation, numbers of successive addition operations are required. Therefore one of the major components required to design a multiplier is Adder. Variety of adders can be used like Ripple Carry, Carry Look Ahead, Carry Select, Carry Skip and Carry Save. A parallel multiplier is for unsigned operands. It is composed of 2-input AND gates for producing the partial products, a series of carry save adders for adding them and a ripple-carry adder for producing the final product. The multiplier architecture with CSA gives better performance in terms of area, speed and power consumption as compared to the architecture with RCA. Basically, sum of three or more n-bit binary numbers can be computed using this carry save adder. Carry save adder is same as a full adder.

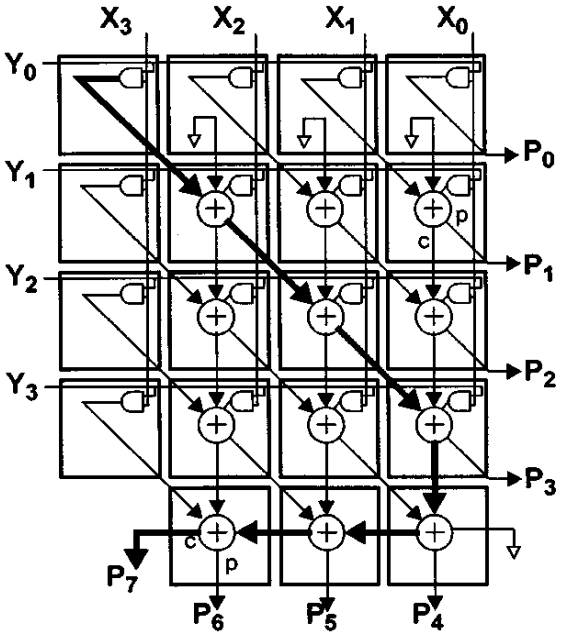

Fig 1: General architecture of 4X4 Carry-save multiplier[1]

Carry unit consists of series of full adders, each of which computes single sum and carry bit based on the corresponding bits of the two input numbers.

The final addition is then computed as:

1. Shifting the carry sequence C left by one place.

2. Placing a 0 to the front (MSB) of the partial sum sequence S.

3. Finally, a ripple carry adder is used to add these two together and computing the resulting sum.

Because of size limitations, a 4X4 version with a critical path highlighted [3] is shown in above Fig 1.

3. LEAKAGE REDUCTION TECHNIQUES

3.1 MTCMOS

The low-power and high performance design requirements of modern VLSI technology can be achieved by using MTCMOS technology. Low, normal and high threshold voltage transistors are used to design a CMOS circuit in this technique. With the scaling of CMOS technology, Supply and threshold voltages are reduced. Sub threshold leakage current increases exponentially with lowering of threshold voltage.

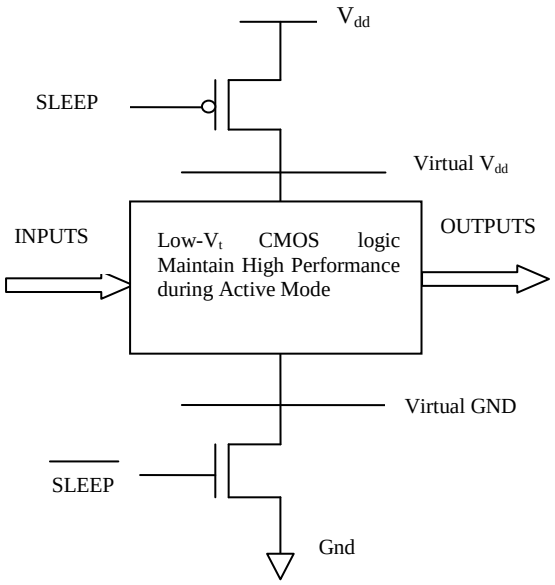

Fig 2: General MTCMOS circuit architecture

Multi-threshold CMOS (MTCMOS) is a design technique in which high threshold sleep transistors are connected between the logic circuit and power or ground, thus creating a virtual supply rail or virtual ground rail, respectively. The low-threshold voltage transistors which have high performance are used to reduce the propagation delay time in the critical path. The high-threshold voltage transistors which have less power consumption are used to reduce the power consumption in the shortest path [4],[5].

Fig.2 shows MTCMOS circuit technology which satisfies both the requirements of lowering the threshold voltage to obtain high speed and reducing standby current to have low power. The two main features of this technique are employing two different threshold voltages on a single circuit and having two operational modes active & sleep for efficient power management.

3.2 DUAL-V_t

Dual threshold voltage technique also uses two threshold voltages as in the case of MTCMOS. Here, high threshold voltage (HTV) is assigned to transistors of some gates in the non-critical paths while specifying the low-threshold voltage for the gates in the critical path. In this technique, no additional transistors are required as in the case of multi-threshold voltage technique. Reduction of static power is achieved while maintaining the same performance as single threshold voltage circuit [6], [7]. Care should be taken while designing, is that if all the transistors in the non-critical paths are assigned with HVT, non-critical path may become a new critical path with a larger path delay than the original one, deteriorating the speed of the circuit.

3.3 LEAKAGE CONTROL TRANSISTOR (LECTOR) Technique

The effective stacking of transistors in the path from supply voltage to ground is the basic idea behind the LECTOR technique for the leakage power reduction. This states that "a state is far less leaky with more than one OFF transistor in a path from supply voltage to ground compared to a state with only one OFF transistor in the path"

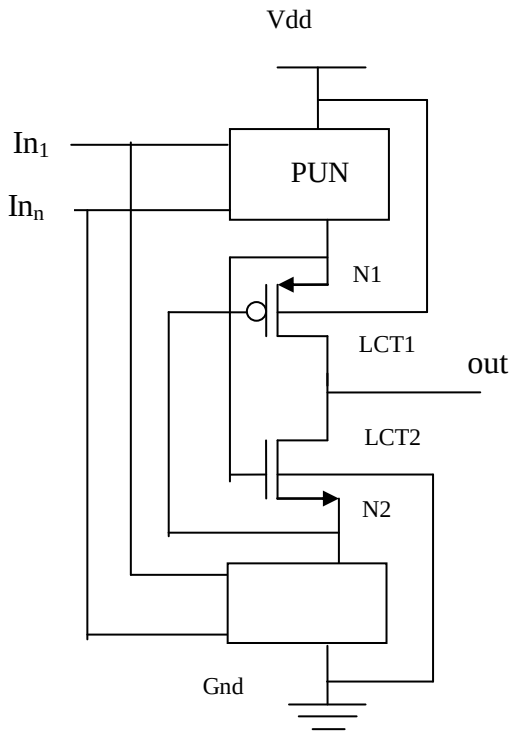

Fig 3: LECTOR CMOS GATE

The LECTOR implementation involves the addition of two LCTS for each gate between the supply and ground path [8]. The general architecture of the LECTOR technique is shown in Fig.3.

4. PROPOSED METHODS

4.1 PROPOSED METHOD1

This is a modified structure of MTCMOS technique. In this structure, the NMOS HVT sleep transistor is arranged as a stack of two transistors with width twice that of original one. A state is far less leaky with more than one OFF transistor compared to a state with only one OFF transistor in the path. This modified method reduces the leakage power to a great extent compared to that of existing.

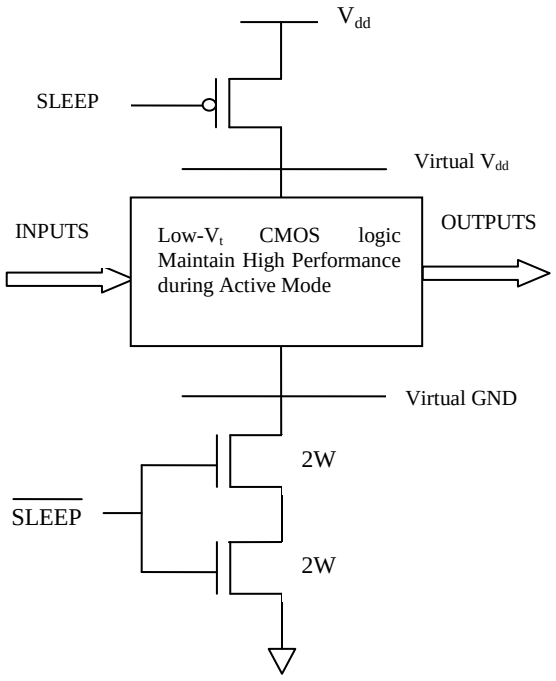

Fig 4: Logic diagram of proposed method1

4.2 PROPOSED METHOD2

It is an improvised structure of existing dual-Vt technique. An NMOS transistor is kept between ground and logic circuit.

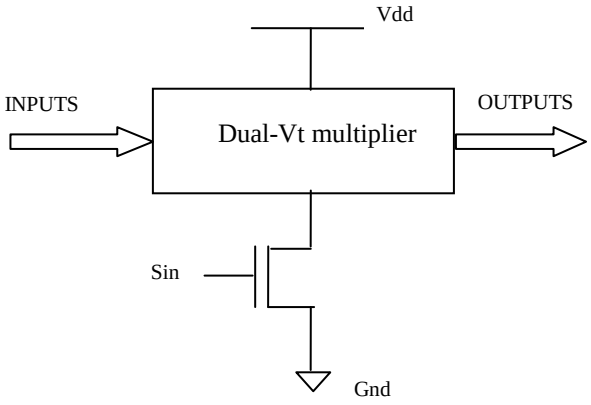

Fig 5: Logic diagram of proposed method2

In active mode, NMOS will be kept ON allowing the circuit to operate normally. In inactive mode NMOS will be kept OFF which provides high resistance path between power supply and ground. The NMOS is kept ON/OFF by means of controlling input Sin.

4.3 PROPOSED METHOD 3

In the proposed design, the critical path blocks in an 8 bit carry-save multiplier are replaced with LCT blocks and other non-critical path blocks are assigned with high threshold voltage. A PMOS transistor is kept over the developed logic which intern cut-off the power supply to the logic block in inactive mode.

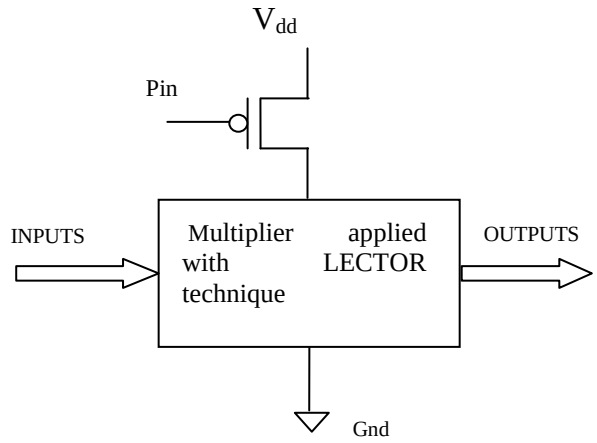

Fig 6: Logic diagram of proposed method 3

5. EXPERIMENTAL ANALYSIS

In this paper an 8X8 multiplier is designed using leakage power reduction techniques like MTCMOS, DUAL-Vt, LECTOR and proposed methods. These designs are simulated using Cadence virtuoso tool in 90nm technology. Table.1 shows the simulation results of all the above techniques in terms of average power, Delay and static power.

Figure [7], [8] and [9] represents the comparison of above techniques in terms of average power, delay and static power. From the simulation results, proposed methods give 99.99%, 99.02% and 99.98% of reduction in static power respectively.

Table1. Simulation results of an 8X8 multiplier

Method	Average power (µw)	Delay (ps)	Static power(w)
Basic multiplier	62.75	91.84	3.3263 e-6
Multi-threshold	28.98	274.76	3.7387 e-11
Dual-threshold	20.71	119.80	7.1452e-7
LECTOR	28.27	130.85	6.3806e-6
Proposed method1	26.89	346.94	8.4968e-12
Proposed method2	19.84	145.15	3.2453e-8
Proposed method3	16.51	137.50	4.4948e-10

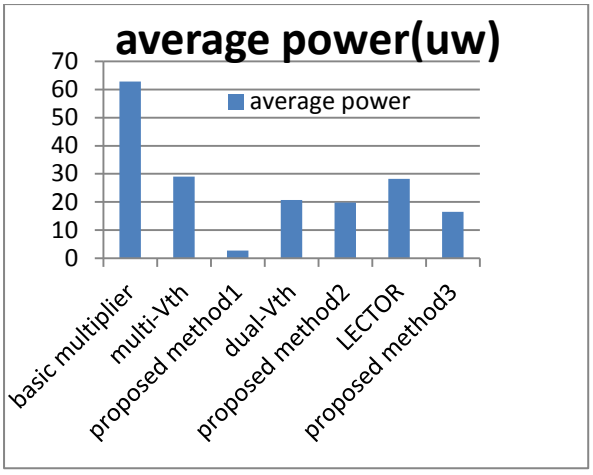

Fig 7: comparing average power of above techniques

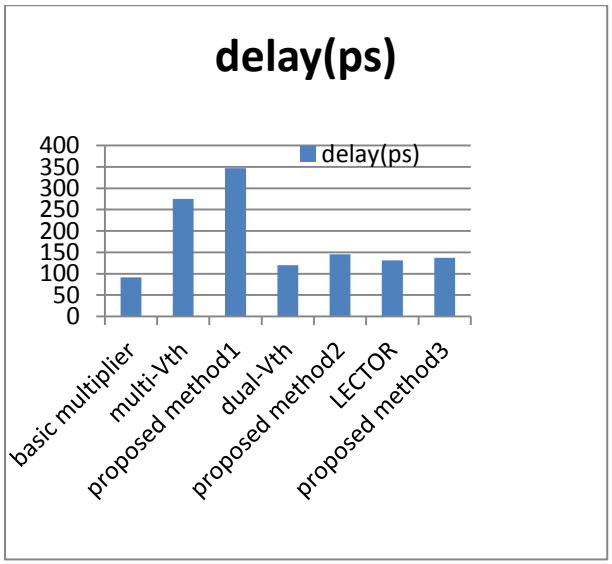

Fig 8: comparing average power of above techniques

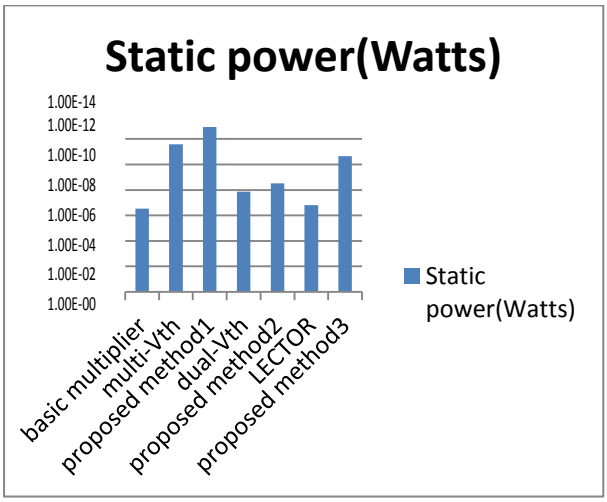

Fig 9: comparing static power of above techniques

6. CONCLUSIONS

In this paper multiplier is designed with different leakage power reduction techniques like Multi-V_t, Dual-V_t, LECTOR and proposed methods. Proposed method1 is an effective circuit level technique that enhances the performance and provides low design methodologies by using both low and high threshold voltage transistors. From Simulation results it is concluded that proposed method1 effectively reduces leakage power to an extent of 99%.

7. ACKNOWLEDGMENTS

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