Single Active Element based Current-Mode All-Pass Filter

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ABSTRACT
In this paper, a current-mode all-pass filter employing single multi-output dual-X second-generation current conveyor, a grounded resistor and a grounded capacitor is proposed. The circuit is as good as ideal for current-mode cascading by possessing low input and high output impedances. The use of grounded passive components makes the circuit, ideal for IC implementation. The effect of non-idealities and parasitics associated with the real MO-DXCCII implementation is also considered. The theoretical results are validated through PSPICE simulation program using 0.35µm CMOS process parameters.

Keywords
Active filters, current conveyor, all-pass filter, analog signal processing.

1. INTRODUCTION
First order all-pass filter (APF), also called as a phase shifter is a simple and useful analog building block for many analog signal processing applications. The few important applications of interest are in delay equalization, in communication and instrumentation system, etc. [1-3]. Recently, the design of first order current-mode all-pass filter (CMAPF) is focused on the use of minimal number of components i.e. one active element and two passive components (minimum for first order active RC realization).

Numerous first order current-mode APFs employing different types of current-mode active elements such as second generation current conveyor (CCII) [5-6, 8-9, 11, 15-16, 18, 20, 27], four terminal floating nullor (FTFN) [7], third generation current conveyor (CCIII) [12, 17], Current operational amplifier (COA) [13], differential voltage current conveyor (DVCC) [14], current differencing buffered amplifier (CDBA) [10], dual-X second-generation current conveyor (DXCCII) [4, 19, 26] are available in the literature. Some of the current-mode all-pass filter circuits do enjoy the feature(s) of grounded components, minimum components, single active element, low-input and high-output impedances.

In this paper a novel first order current-mode all-pass filter is presented. The proposed circuit employs single active element and two grounded passive components. It also possesses low-input and high-output impedance feature with no element matching restriction. The proposed circuit is based on multi-output dual-X second-generation current conveyor (MO-DXCCII) [21]. It is a useful and versatile current-mode active element for analog signal processing applications [22-24, 28-29]. The proposed circuit is validated through PSPICE simulation using TSMC 0.35µm CMOS process parameters.

2. CIRCUIT DESCRIPTION
A MO-DXCCII is characterized by the following port relationship:

$$\begin{bmatrix} I_Y \\ V_{X+} \\ V_{X-} \\ I_{Z1+} \\ I_{Z2+} \\ I_{Z1-} \\ I_{Z2-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{X+} \\ I_{X-} \end{bmatrix} \tag{1}$$

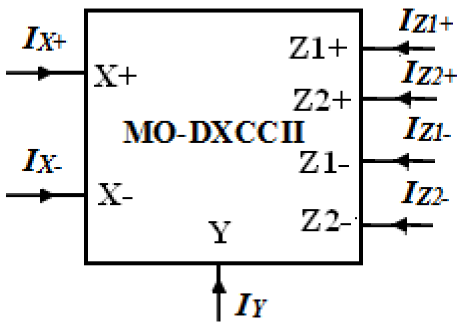
The symbol and CMOS implementation of MO-DXCCII are shown in Fig. 1. The proposed CMAPF using single MO-DXCCII and two grounded passive components is shown in Fig. 2. The circuit is characterized by the following transfer function

$$\frac{I_{OUT}}{I_{IN}} = \frac{sCR-1}{sCR+1} \tag{2}$$

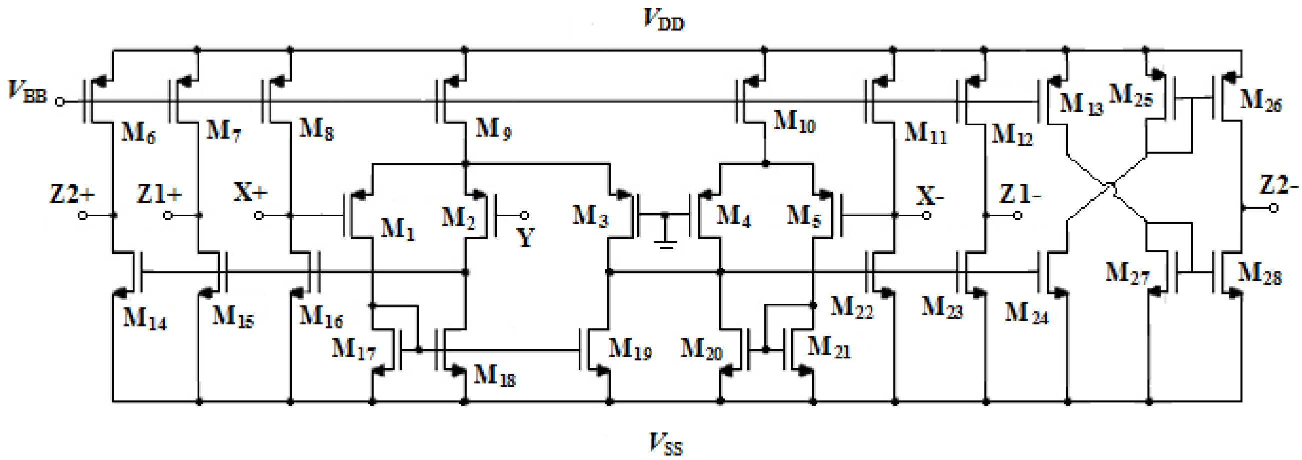
The frequency dependent phase response (Φ) of the proposed circuit is given as

$$\phi(\omega) = 180^0 - 2\tan^{-1}(\omega CR) \tag{3}$$

It is evident from equation (3) that the circuit of Fig. 2 realizes first order all-pass filter with only single active element and two grounded passive components without any matching constraints. The proposed circuit possesses low input and high output impedance, since the input current is applied to the X-terminal and the output current is taken from the Z terminal, which makes it suitable for cascading without the need of additional circuit of current buffer.



(a)



(b)

Fig 1: (a) Symbol, and (b) CMOS Implementation of MO-DXCCII.

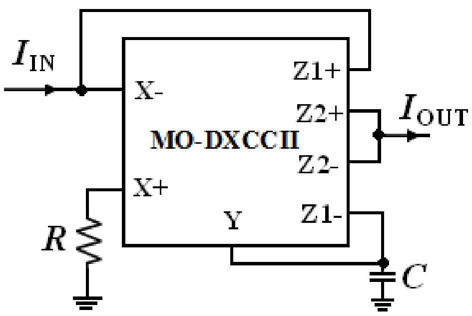


Fig 2: Current-mode all-pass filter

It is worth mentioning that by interchanging the resistor and the capacitor in the Fig. 2 an additional all-pass filter circuit can be obtained. However the circuit would employ a grounded capacitor at the X terminal of MO-DXCCII, which does pose a high frequency limitation. It is a well known fact that the use of capacitor at the X terminal of the current conveyor circuit would pose a high frequency limitation [25].

3. NON-IDEAL ANALYSIS

Considering the non-idealities of the MO-DXCCII into account, the port relationships of the terminal voltages and currents can be written as

$$\begin{bmatrix} I_Y \\ V_{X+} \\ V_{X-} \\ I_{Z1+} \\ I_{Z2+} \\ I_{Z1-} \\ I_{Z2-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta_1 & 0 & 0 \\ -\beta_2 & 0 & 0 \\ 0 & \alpha_1 & 0 \\ 0 & \alpha_2 & 0 \\ 0 & 0 & \alpha_3 \\ 0 & 0 & -\alpha_4 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{X+} \\ I_{X-} \end{bmatrix} \tag{4}$$

Here, α_1 and α_2 are the current transfer gains (deviate from unity by the current tracking errors) from X+ terminal to Z1+ and Z2+ terminals respectively, α_3 and α_4 are the current transfer gains from X- terminal to Z1- and Z2- terminals, respectively, and β_1 and β_2 are the voltage transfer gains (deviate from unity by the voltage tracking errors) from Y input terminal to X+ and X- terminals, respectively. However, these transfer gains remain close to unity upto a very high frequency range (i.e. in GHz); the actual value depends upon the technology and the devices used in implementing the active element [25].

Taking the tracking errors of the non-ideal MO-DXCCII into account, the proposed circuit is reanalyzed and the modified transfer function is found to be as

$$\frac{I_{OUT}}{I_{IN}} = \alpha_3\alpha_4\left[\frac{sCR\alpha_4 - \alpha_2\beta_1}{sCR + \alpha_1\alpha_3\beta_1}\right] \tag{5}$$

From equations (5), it is to be noted that the non-idealities do affect the filter gain and the pole frequency. The active and passive sensitivities of the proposed circuit with respect to pole frequency (ω_o) and gain (H) are as follows

$$S_{C,R}^{\omega_o} = -1, S_{\alpha_1,\alpha_3,\beta_1}^{\omega_o} = 1, S_{\alpha_2,\alpha_4,\beta_2}^{\omega_o} = 0, S_{C,R,\alpha_1,\alpha_2,\beta_1,\beta_2}^{H} = 0, S_{\alpha_3,\alpha_4}^{H} = 1 \quad (6)$$

Equation (6) shows that the sensitivities are within or equal to unity in magnitude, thus ensuring good active and passive sensitivity performance.

4. PARASITIC EFFECTS

Next study is carried out on the effects of various parasitics of the MO-DXCCII employed in the proposed circuit. These are the Y and Z terminals parasitic capacitances and the X-terminal resistance. For the circuit of Fig. 2, the Y and Z1-terminal capacitances (C_Y and C_{Z1-}) appear in shunt with external C and the X+ terminal resistance (R_{X+}) appears in series with external *R*, thus the modified transfer function is

$$\frac{I_{OUT}}{I_{IN}} = \frac{s - \dfrac{1}{(C + C_Y + C_{Z1-})(R + R_{X+})}}{s + \dfrac{1}{(C + C_Y + C_{Z1-})(R + R_{X+})}} \quad (7)$$

From equation (7), it is to be further observed that most of the parasitic capacitances and resistances get merged with the external capacitor and resistor. Such a merger will cause a slight offset in circuit parameters, which can be corrected by pre-distorting the passive element values used in the circuit.

5. SIMULATION RESULTS

The proposed circuit in Fig. 2 was simulated using the PSPICE simulation program with CMOS implementation of MO-DXCCII [21] using TSMC 0.35 μm process parameters as listed in Table 1. The supply voltages used were ± 1.8 V and V_{BB} = -0.5 V and the aspect ratios of NMOS and PMOS transistors are listed in Table 2. The proposed circuit was designed for a theoretical pole frequency of 1.59 MHz. The designed values used were *C* = 100pF and *R* = 1 KΩ. The phase and gain plots are shown in Fig. 3, which shows a pole frequency of 1.57 MHz, which is close to the designed value. The phase is found to be vary from 180^0 to 0^0.

Table 1. TSMC 0.35 μm CMOS process parameters.

NMOS:
LEVEL=3 TOX=7.9E-9 NSUB=1E17 GAMMA=0.5827871 PHI=0.7 VTO=0.5445549 DELTA=0 UO=436.256147 ETA=0 THETA=0.1749684 KP=2.055786E-4 VMAX=8.309444E4 KAPPA=0.2574081 RSH=0.0559398 NFS=1E12 TPG=1 XJ=3E-7 LD=3.162278E-11 WD=7.04672E-8 CGDO=2.82E-10 CGSO=2.82E-10 CGBO=1E-10 CJ=1E-3 PB=0.9758533 MJ=0.3448504 CJSW=3.777852E-10 MJSW=0.3508721
PMOS:
LEVEL =3 TOX = 7.9E-9 NSUB=1E17 GAMMA=0.4083894 PHI=0.7 VTO=-0.7140674 DELTA=0 UO=212.2319801 ETA=9.999762E-4 THETA=0.2020774 KP=6.733755E-5 VMAX=1.181551E5 KAPPA=1.5 RSH=30.0712458 NFS=1E12 TPG=-1 XJ=2E-7 LD=5.000001E-13 WD=1.249872E-7 CGDO=3.09E-10 CGSO=3.09E-10 CGBO=1E-10 CJ=1.419508E-3 PB=0.8152753 MJ=0.5 CJSW=4.813504E-10 MJSW=0.5

Table 2. Transistor aspect ratios

Transistors	W(μm)	L(μm)
M_1-M_2	1.4	0.7
M_3-M_5	2.8	0.7
M_{17}-M_{18}	2.4	0.7
M_{19}-M_{21}	4.8	0.7
M_6-M_{16}, M_{22}-M_{28}	9.6	0.7

Next, the circuit may use as a phase shifter introducing a 90^0 shift to a sinusoidal signal of pole frequency. The input and 90^0 phase shifted output waveforms are shown in Fig. 4, which verify the circuit as a phase shifter. In addition, the Fourier spectrums of the input and output currents, showing high selectivity for the applied input current are shown in Fig. 5. The total harmonic distortion (THD) variation with respect to the amplitude of the applied sinusoidal input current at 1.59 MHz is shown in Fig. 6. It can be seen that the THD value of the filter remains below 3% for the input current up to 1mA (peak to peak). Simulation results are quite agreed with the theoretical results.

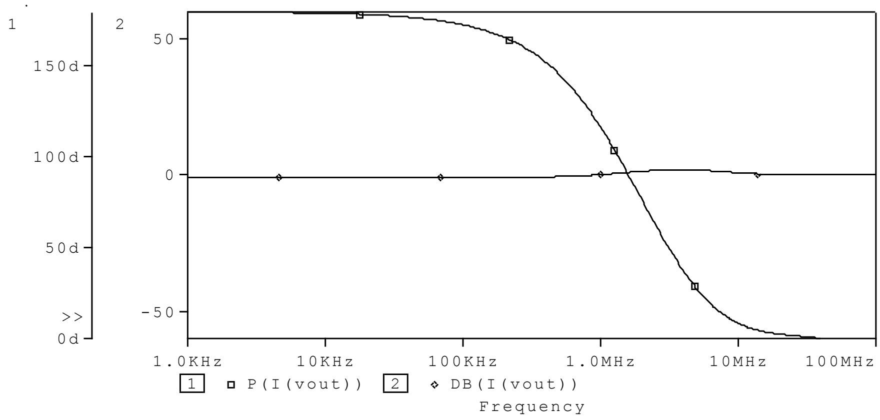


Fig 3: Phase and gain plot for Circuit of Fig. 2

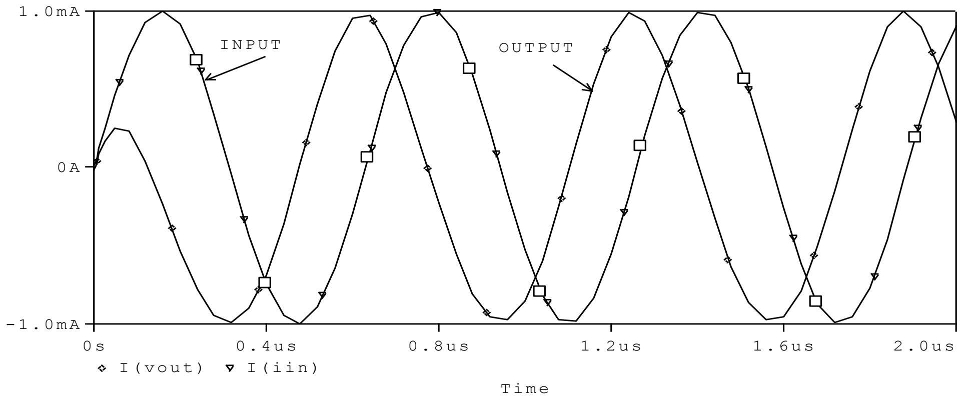


Fig 4: Input and 90^0 phase shifted output at 1.59MHz.

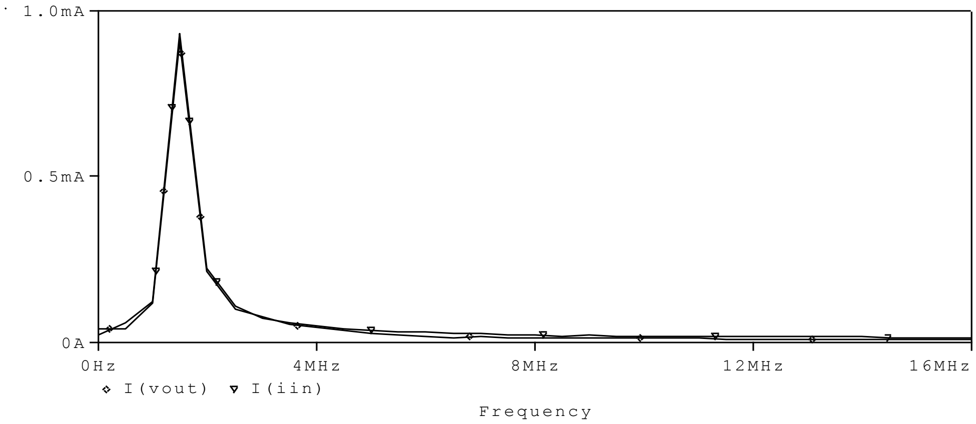


Fig 5: Fourier spectrum of the input and output signal at 1.59MHz

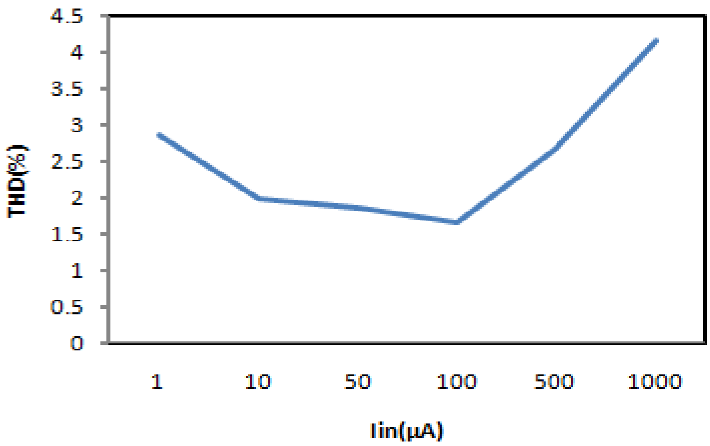


Fig 6: THD variation at output with signal amplitude at 1.59MHz

6. CONCLUSION

This paper presented a first order current-mode all-pass filter suitable for cascading, employing minimum number of active and passive components (one MO-DXCCII, one grounded resistor and one grounded capacitor). The circuit enjoys low input and high output impedance feature, which is a desirable feature for the current mode cascading. Beside this, the circuit employs grounded passive components, which are suited for IC implementation. The proposed circuit requires no matching constraints, possesses low active and passive sensitivities. The proposed circuit is validated by attractive simulation results.

7. REFERENCES

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