Three New Investigations of Aggressive Packet Combining to Get High Throughput

Swarnendu K Chakraborty
Department of CSE
NIT Arunachal Pradesh, India

Rajat S Goswami
Department of CSE
NIT Arunachal Pradesh, India

Abhinandan Bhunia
Microsoft Corporations, USA

Chandan T Bhunia
Director
NIT Arunachal Pradesh, India

ABSTRACT
Aggressive Packet Combining (APC) scheme is well established in literature for receiving correct packet in high error prone wireless link. Several modifications were earlier studied elsewhere for improving throughput and decreasing latency. In APC three copies of a packet are transmitted and receiver does bit wise majority decision to get correct copy. Main research challenge of the APC is if two or more copies of the packet become erroneous at a particular bit location(s) the operation of the majority logic fails to correct the error. To address the above drawback of the APC, three new modifications of APC are proposed in this paper. The proposed techniques are found to provide better throughput & high error correction probability.

Keywords
Packet Combining Scheme, Conventional Aggressive Packet Combining Scheme (CAPC), Throughput, Bit error rate, three paths, XOR, half bit exchange.

1. INTRODUCTION
Reliable transport of data from a sender to a receiver is a research challenge. Basic technique for the same is either BEC (backward error correction) or FEC (forward error correction) [1-5]. Many different studies [3-5, 8, 15] have conclusively established that BEC is more appropriate for wired transport where as FEC for wireless transport. Wireless is of high bit error rate that calls for application of FEC in order to avoid delay in transportation. Leung [7] proposed an idea of Aggressive Packet Combining scheme (APC) for error control in wireless networks with the basic objective of fast error control in relatively higher noisy wireless networks. In order to combat errors in computer/ data communication networks, ARQ (Automatic Repeat Request) techniques [1-5] with various modifications as applicable to in various communication environments are used. APC is well established and studied elsewhere [3-10].Several modifications of APC are also reported elsewhere [2-13]. The modifications are due to increasing throughput, tackling various error syndromes and enhancing fast correction. In APC and/ or modified APCs, two or more copies of the packets are transmitted. Copies received by the receiver either error free or erroneous are used in receiver to correct errors by applying Packet Combining schemes differently in different situations. However in original APC, if an error occurs at same locations of erroneous packets, the application of the majority logic as in original APC fails to correct the error. To address the stated problem of APC we propose two new protocols of APC. Analytical results establish that the proposed new schemes are superior to original APC.

2. REVIEW OF PACKET COMBING SCHEME
Chakrabotry [11] suggested a very simple and elegant technique known as packet combining scheme (PC) where the receiver will correct limited error, one or two bit error, from the received erroneous copies. Assume an original packet "10101010" is transmitted between a sender and a receiver. The packet erroneously received by the receiver is "00101010". The receiver requests for retransmission of the packet and keeps the copy that has been received erroneously as well. The transmitter retransmits the packet, but again the packet is received by the receiver erroneously as "11101010". Chakraborty suggested that the receiver can correct the error by using two erroneous copies. After making a bit wise XOR operation between erroneous copies, the receiver can locate the error position. The operation can be identified by an example given below:

First erroneous copy = 00101010

Second erroneous copy = 11101010

XOR 11000000

The error locations are identified as first and/or second bit from left. Chakraborty suggested that the receiver can apply the brute method to correct error by changing received "1" to "0" or vice versa on the received copies followed by the application of error decoding method in use. In the example the average number of brute application will be ½ and in general 2^{n-1} if n bits are found in error. Several modifications of PC have been studied elsewhere [12-13] by Bhunia.

3. REVIEW OF CONVENTIONAL APC
Aggressive packet combining scheme is a modification of MjPc (Majority Packet Combining) [14].To illustrate APC it is assumed that an original packet 10101010 is transmitted between a sender and a receiver. In Aggressive Packet combining Scheme (APC) the three copies of packet are sent for each packet between a source and a destination. The majority logic is applied bit to bit on three copies of packet. In table: (1) we have shown different possibilities of APC. In Case (1) there is no error in transmitted three copies. In Case (2) receiver receives two copies of correct packet and one copy with an error, so the correction is possible by majority logic. In Case (3) and Case (4) errors are present in two or more copies in which case correction is not possible.

Table: 1: Different cases of Aggressive Packet Combining Scheme

Case 1	Case 2	Case 3	Case 4
Copy-1= 10101010 Copy -2= 10101010 Copy-3= 10101010	Copy-1= 00101010 Copy -2= 10101010 Copy-3= 10101010	Copy-1= 00101010 Copy -2= 00101010 Copy-3= 10101010	Copy-1= 00101010 Copy -2= 00101010 Copy-3= 00101010
Correction Probability is $(1-P^3)$	Correction Probability is $(1-P^2)$ P	Correction Probability is $(1-P)$ P^2	Correction Probability is (P^3)
Correction not required.	Correction possible	Correction not possible	Correction not possible

4. NEW BASIC IDEA

Scheme 1: In the original APC, three copies of a packet are transmitted sequentially. We assume these three copies are CP1, CP2 and CP3. As per our protocol we will have to transmit CP1 normally and being received by the receiver erroneously with error say in 1st bit location. CP2 will be generated as: CP2 = previously received correct copy (a copy is retained by transmitter) $\oplus$ present copy to be transmits and generated CP2 is then sent. CP3 will be generated as: shifting of CP2 left with n/2 times where n is the packet size. For both cases in CP2 and CP3 the receiver will apply reverse process. Above protocol explained thoroughly with different examples;

I) suppose original packet is "00010011" and previous packet is "10101010". As per proposed scheme CP1will have to transmit as it is and being received by the receiver erroneously in 1st bit location "**1**0010011". CP2 will be transmitted after XORed with previous packet (00010011 XOR 10101010 = 10111001), here we are transmitting "10111001" being received by the receiver as without error and receiver will do reverse process to get "00010011. After that we will be transmitted CP3 as per CP2 but after half bit exchanged form like instead of "10111001" we will have to send "10011011" and received by the receiver erroneously in 1st bit as " **0**0011011". Receiver will do reverse to get back "0001**1**011". So three copies at receiver side are;

CP1------- 10010011
CP2------- 00010011
CP3------- 00011011

00010011, after majority logic we are able to get back original copy by this proposed scheme but in normal APC this won't be possible because we have got error in more than one in same bit location.

II) Suppose original packet is "00110101" and previous packet is "00010011", as per proposed scheme;

Sender side: Receiver side:

CP1 (00110101) CP1 (**1**0110101)

00110101
00010011

00100110
CP2 (00100110) CP2 (00100110)

After XOR (00110101)

CP3 (01100010) CP3 (**1**1100011)

After

Half exchanged CP3 (0011**1**110)

CP1 (**1**0110101)

CP2 (00110101)

CP3 (0011**1**110)

00110101, original packet after majority logic.

III) Suppose original packet is "11010111" and previous packet is "00110101", as per proposed scheme;

Sender side: Receiver side:

CP1 (11010111) CP1 (**0**1010111)

11010111

00110101

11100010

CP2 (11100010) CP2 (11100010)

After XOR (11010111)

CP3 (00101110) CP3 (10101110)

After

Half exchanged CP3 (1101**1**111)

CP1 (**0**1010111)

CP2 (11010111)

CP3 (1101**1**111)

11010111, original packet after majority logic.

Scheme 2: In the conventional APC, three copies of a packet are transmitted sequentially in a single path, here we are proposing to transmit three copies of a packet in three different path or two copies in a single path and one copy in another path. Under this new scheme probability of error (E) in packet are given below;

Case 1: Three copies each of "**n**" bits in a single path:

$E1 = 1 - (1 - \alpha)^{3n}$ …… (i) (e1)
(Normal APC)

Case 2: Two copies each of "**n**" bits in a single path and another copy of "n" bits in another path:

$2(E2)^2 / 2(E3)^2 = 1 - (1- \alpha)^{2n}$ …… (ii) (e2)

$(E2)^1 / (E3)^1 = 1 - (1- \alpha)^{n}$ …… (iii)

Case 3: Single copy each of "**n**" bits is in a single individual path:

$E31 = 1 - (1- \alpha)^{n}$ …… (iv) (e3)

$$E32 = 1 - (1- \alpha)^{n} \ldots\ldots\ldots (v)$$

$$E33 = 1 - (1- \alpha)^{n} \ldots\ldots\ldots (vi)$$

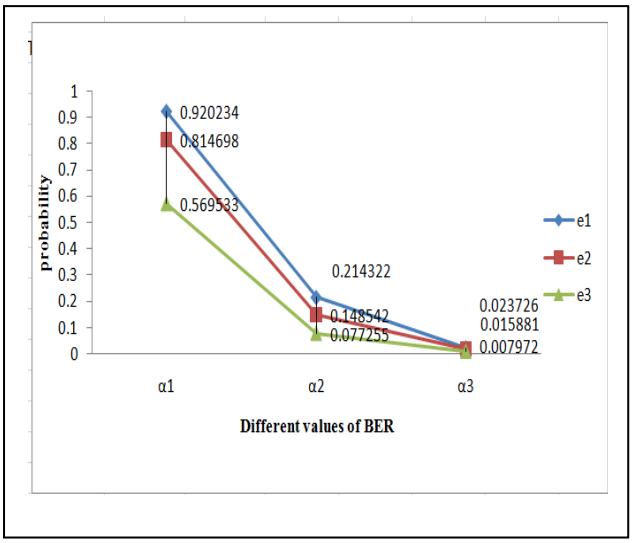

Fig (1): Probability of error in packet comparison for different values of BER (α).

Scheme 3: In the original APC, three copies of a packet are transmitted sequentially. One modification of APC(MAPC) namely Bitwise repetition [16] , under that scheme instead of sending three copies of a packet one after another from the source to the receiver like conventional APC, we are repeating each bit location three times one after another and sending from the source to the receiver. At receiver side receiver applies majority logic with every successive three bits to find out the correct packet. Say an original packet is:"11011101" and we are sending this packet under proposed scheme like; 111111000111111111000111 from the source to the receiver. At the time of transmission in channel due to error data stream is changed, new data stream will be;

110111000111111111010111 at receiver end receiver will try to correct the packet by applying majority logic with three successive bits. (Error location is marked in boldface).

110 – 1, 111—1, 000 – 0, 111—1, 111—1, 111—1, 010—0, 111—1, so ultimate corrected packet will be "11011101". Numerically it has been proved that conventional APC is good for Burst Error (BE) and modified APC (Bitwise repetition) is good for Random Error (RE). So we are proposing a new scheme which will be an adaptive technique to control. As per our new technique initially sender sends packets under bitwise repetition (modified APC) until its gets a negative acknowledgement from the receiver. When sender gets negative acknowledgement from the receiver, sender switch to conventional APC for transmission of packets until it gets negative acknowledgement. System will switch its transmission under these two schemes with every negative acknowledgement.

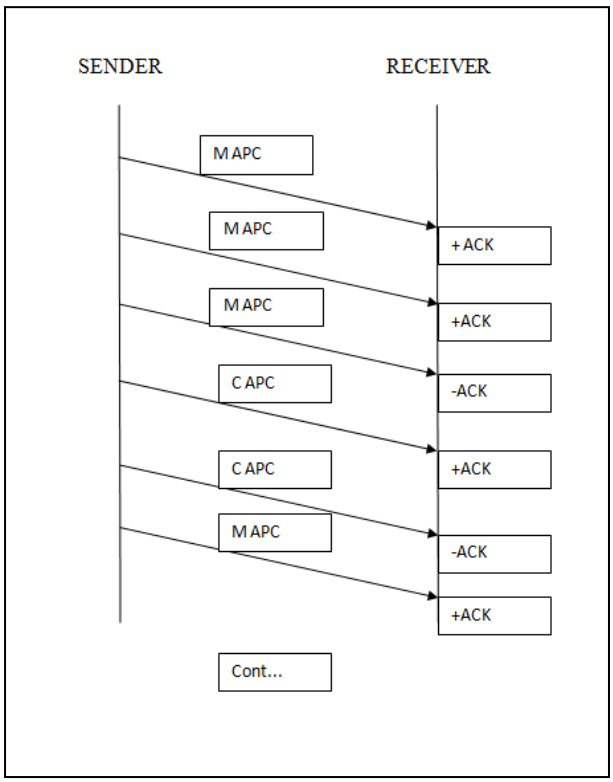

Fig (2): operation of scheme 3.

5. ANALYSIS

As per analysis and examples cited, scheme 1 offers better correction capability over conventional APC. The fig (1) conclusively establishes that APC implement in 2 paths/ 3 paths is more reliable than normal APC. In scheme 3, a protocol is proposed to tackle both random and burst error in the link that normal APC does not do.

6. CONCLUSIONS

In this paper, three new schemes of APC are proposed & studied. These schemes provide better correction capability. Numerical studies duly establish the superiority of proposed techniques over normal APC. Simulation study will be made in future research.

7. REFERENCES

[1] C T Bhunia, A Few Modified ARQ Techniques, Proceedings of the International Conference on Communications, Computers & Devices, ICCCD-2000, 14-16, Decedmber'2000, IIT, Kharagpur, India, Vol.II, pp. 705-708.

[2] C T Bhunia, ARQ Techniques: Review and Modifications, Journal IETE Technical Review, Sept-Oct'2001 Vol18, No 5, pp 381-401

[3] R J Beniece and A H Frey Jr, An analysis of retransmission schemes, IEEE Trans CommTech, COM-12, pp 135-145, Dec 1964.

[4] S Lin, D Costello Jr and M J Miller, Automatic repeat request error control schemes, IEEE Comm Mag, 22, pp 5-17, Dec '1984.

[5] A R K Sastry, Improving Automatic Repeat Request (ARQ) Performance on Satellite Channels Under High

Error Rate Conditions, IEEE Trans Comm, April'77, pp 436-439.

[6] C T Bhunia Modified Aggressive Packet Combining Scheme, Pre-print, ICTP, Italy, IC/2010/037, pp. 1-10.

[7] Yiu-Wing LEUNG, Aggressive Packet Combining for Error Control in Wireless Networks, trans. Comm Vol. E83, No 2Feb'2000, pp38-385

[8] Don Towsley, The Shutter Go Back-N ARQ Protocol, IEEE Trans Comm, Vol 27, No 6, June'79, pp 869-875.

[9] N D Birrell, Pre-emptive retransmission for communication over noisy channels, IEE Proc Part F, Vol 128, 1981, pp 393-400.

[10] H Bruneel and M Moeneclacey, On the throughput performance of some continuous ARQ strategies with repeated transmissions, IEEE Trans Comm, Vol COM m34, 1986, pp 244-249.

[11] Shyam S. Chakraborty et al, An ARQ Scheme with Packet Combining, IEEE Comm Letters, Vol 2, No 7, July'95, pp 200-202.

[12] C T Bhunia, Modified Packet Combining Scheme using Error Forecasting Decoding to combat error in network, Proc. ICITA'05(Proc. IEEE Computer Soc.), Sydney, Vol, 2, 4-7, July'2005, pp 641-646

[13] C T Bhunia, Packet Reversed Packet Combining Scheme, Proc. IEEE Computer Soc, CIT'07, Aizu University, Japan, pp. 447-451

[14] S B Wicker, Adaptive rate error control through the use of diverse combining and majority logic decoding in hybrid ARQ protocol, IEEE Trans Comm., Vol.39. No. 3, March'1991, pp 380-385.

[15] Joel M Morries, On another Go-Back –N ARQ Techniques For High Error Rate Conditions, IEEE Trans Comm, Vol 26, No 1, Jan'78, pp 186-189.

[16] Swarnendu K Chakraborty, Rajat S Goswami, Abhinandan Bhunia, C T Bhunia, "Studies of several new modifications of Aggressive Packet Combining to achieve higher throughput, based on correction capability of disjoint error vectors", communicated to Journal of the Institution of Engineers (India): Series B.