Comparative Analysis of Low Power Sequential Elements

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ABSTRACT
Main constraint for any VLSI system is power, speed and area but power consumption is major hurdle for system performance. In this paper a series of improved power efficient sequential elements (flip-flops) are presented. Such as conditional data mapping flip-flop (CDMFF), clocked pair shared flip-flop (CPSFF) and new proposed flip-flop in which dual edge triggered technique is used. In conditional data mapping methodology the less power consumption achieved by mapping the inputs in such way that eliminates the unnecessary transitions. But CPSFF the clock load is minimized it leads to power saving. In new propose technique clock frequency could reduce by half then the power dissipation due to clock transitions can be reduced by half it leads to power efficient model flip-flop.

Keywords
Data mapping, Clock load, CPSFF, Flip-flop, Power, Edge-triggered.

1. INTRODUCTION
Power consumption is depends on several factors, the total power is sum of dynamic, short circuit and leakage power dissipation. Dynamic power dissipation is function of frequency, supply voltage, data activity.

Based on these parameters, there are several ways to reduce power consumption.

1) Using low swing voltage on the clock distribution network can minimize the clocking power consumption due to power is quadratic function of voltage.

2) Reducing clock load: Huge amount of on chip power is consumed by clocking system the effective way to achieve low power design for clocking system is to minimize the clock load by reducing number of clocked transistors.

3) Using dual edge triggering methodology in this technique the data is sampled for both edges of clock signal i.e. using half frequency on clock distribution network leads to save approximately half of the power consumption on clock distribution network.

Using dual edge triggering, data latching or sampling is used at both the rising and falling edges, usually allows the clock routing network to consume less power. For example, for a system with through put of one operation per cycle and a clock frequency, dual edge triggering results in two operations being executed in one cycle; if we use half the frequency, we can maintain the same throughput of the original system. With half the frequency, the clock switching activity is reduced by half, which leads to considerable power savings in the clock routing network.

2. CONDITIONAL DATA MAPPING METHODOLOGY:
In data mapping methodology in which reduce their dynamic power dissipation by mapping their inputs to a configuration that eliminates redundant internal transitions. Conditional data mapping methodology explained as below.

Table 1: S-R Flip-flop with differential Inputs

S	R	Q	QB	Dynamic power
0	0	Qn-1	QBn-1	Very low
0	1	0	1	High
1	0	1	0	High
1	1	….	….	……

Consider S-R flip-flop which having properties as Table 1. At (0,0) input, the flip-flop does not perform any pull-up or pull-down transition when triggered a clock signal, and its outputs (Q,QB) retain their previous states, respectively. This accounts for no dynamic power dissipation at its internal nodes. Whenever redundant event is recognized the flip-flop map its input into (0, 0) state where dynamic power dissipation is very low. Unnecessary event means where the output is unchanged when subsequent clock signal is triggered.

2.1 Conditional Data Mapping Flip-Flop:

Conditional data mapping flip-flop (CDMFF,Fig.1) used seven clocked transistors, resulting in about 50% reduction in the number of clocked transistors, hence CDMFF used less power than Conditional capture flip-flop(CCFF) and CDFF (previous low power flip-flops).

The flip-flop is driven by clock CLK and delayed complementary clock CLKB, which produce a short transparency period when both CLK and CLKB are HIGH. Before the transparency period, node X is precharged to HIGH. Suppose Q (previous output) is LOW and D is HIGH. This makes output of AND gate become HIGH. When the flip-flop turning in to the transparency period, X is pulled down to LOW through N1, N3 and N5, and N4 is open. Node X is low this switches on P3, pulling Q up to HIGH. After the

transparency period, X is precharged to HIGH.

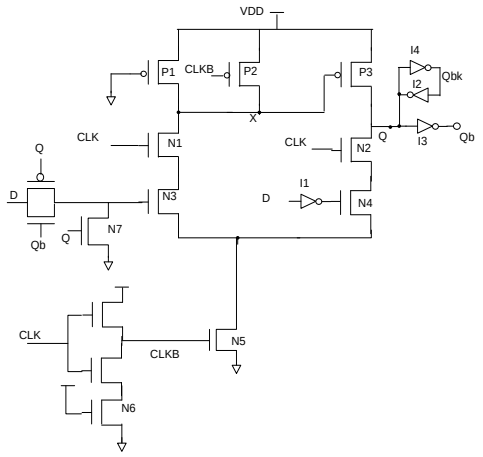

Figure 1: Conditional Data Mapping Flip-flop.

When the flip-flop is turning in to the transparency period again, no internal transition exists, and (Q,QB) retain their previous states as HIGH and LOW, respectively, since all pull-up and pull-down paths are deactivated due to both AND gate output and Y being LOW. Therefore, no dynamic power dissipates at this redundant event. Suppose Q (previous output) is HIGH and D is LOW. This makes output of AND gate becomes LOW. When the flip-flop turning in to the transparency period, Q (HIGH) is pulled down to LOW through N1, N2 and N5, and N4 is ON. Output Q become LOW. A delay cell is used for producing CLKB from CLK. A pass-gate version of AND gates used to construct the data mapper, for decreasing the latency of the data path. The inverter at nodes are used to maximize the noise immunity of precharge nodes by making them fully static.

However, there is redundant clocking capacitance in CDMFF. When data remains LOW or HIGH, the precharging transistors, P1 and P2, keep switching without any useful computation, resulting in redundant clocking. It is necessary to reduce redundant power consumption here. Further, When clock signal CLK transits from LOW to HIGH, CLKB will stay 1 for a short while which produces an implicit pulse window for evaluation. During that window, bothP1, P2 are off. In addition, if transits from low to high, the pull down network will be disconnected by N3 using data mapping scheme, If D is 0, the pull down network is disconnected from GND also. Hence internal node is not connected with Vdd or GND during most pulse windows, it is essentially floating periodically. If a nearby noise discharges the node X, due to this PMOS transistor P3 will be partially on, and an unwanted glitch will appear on output node.

3. CLOCKED PAIR SHARED IMPLICIT PULSED FLIP-FLOP:

Clocked Pair Shared flip-flop (CPSFF, Fig.2) use less clocked transistor than CDMFF and to overcome the floating problem in CDMFF. In the clocked-pair-shared flip-flop, clocked pair (N3,N4) is shared by first and second stage. An always on pMOS, P1, is used to charge the internal node rather than using the two clocked precharging transistors in CDMFF. Comparing with CDMFF, a total of three clocked transistors are reduced.

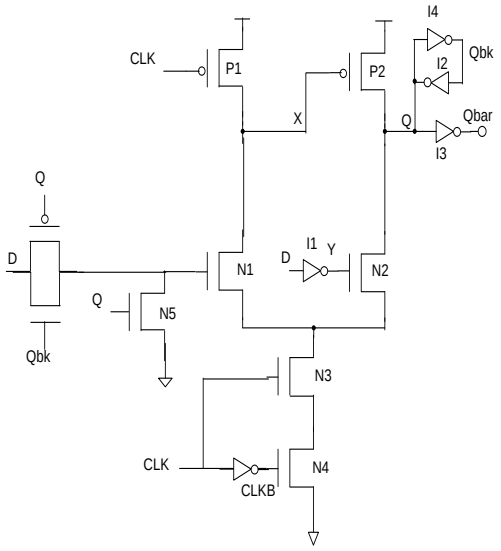

Figure 2: Clocked Pair Shared Flip-flop

Internal node X is connected to Vdd by an always on P1, so node X is not floating, resulting in enhancement of noise robustness of node X. This resolves the floating point problem in CDMFF. When input D stays HIGH,Q=1 ,N5 is on, N1 will off to avoid the redundant switching activity at node X as well as any short circuit current. P MOS P2 should pull Q up when D transits to HIGH. The second nMOS branch (N2) is responsible for pulling down the output of Q if D=0 and Y=1 when the clock pulse arrives. pMOS in I1 should turn on nMOS N2 when D=0.

4. PROSPOSED DUAL EDGE TRIGGERD FLIP-FLOP:

Using dual-edge triggering, Data latching or sampling is is used at both the rising and falling edges, usually allows the clock routing network to consume less power. For example, for a system with at throughput of one operation per cycle and a clock frequency, double-edge triggering results in two operations being executed in one cycle, if we use half the frequency, we can maintain the same throughput of the original system. With half the frequency, the clock switching activity is reduced by half, which leads to considerable power savings in the clock routing network.

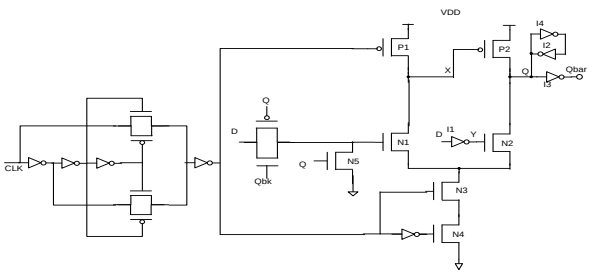

Figure 3: Proposed dual edge triggered flip-flop

Dual edge triggered flip-flop design is used to reduce leakage current, and use more clocked transistors then CSPFF should not increase too much load ,and it can receive input signal at two levels of the clock dual edge triggered flip-flop has ideal logic functionality, simple structure lower delay time, and higher maximum data rate compared to other existing flip-flops.

5. SIMULATION RESULTS:

The simulation results were obtained from HSPICE simulations in 0.18-µm CMOS technology at room temperature. VDD is 1.8V. The setup used in our simulations is shown in Fig. An inverter is placed after output, providing protection from direct noise coupling. The value of the capacitance load at node Qb is 21fF, which is selected to simulate a fan out of 14 minimum sized inverters (FO14). Assuming uniform data distribution, a clock frequency of 250MHz is used.

Table 2. Power consumption comparisons

	CDMFF	CPSFF	PROPO-ED FF
Number of transistor	22	19	24
Clock Incorporated	Single edge triggered	Single edge triggered	Double edge triggered
D-Q Delay(ps)	59	62	61
Power(100%actilvity) [µW]	70.93	53	31.11
Power(50%actilvity) [µW]	39.86	27.74	17.17
Power(25% activity) [µW]	23.11	17.13	10.68
Power(0% D high) [µW]	12.66	9.76	7.11
Power(0% D low) [µW]	13.71	10.11	8.17

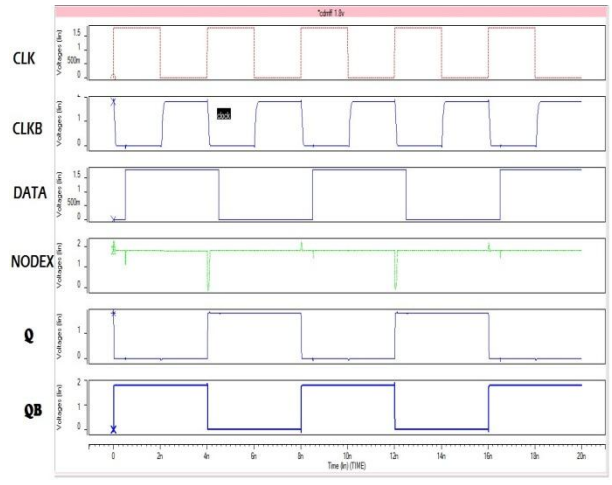

Figure 4: Simulation wave forms of Conditional Data Mapping Flip-flop

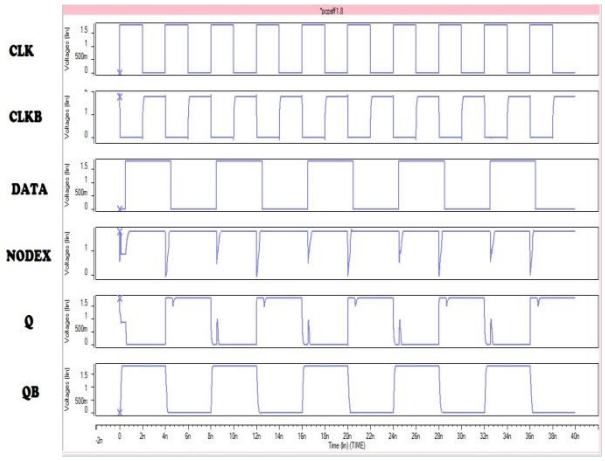

Figure 5: Simulation results of Clocked Pair Shared Flip-flop

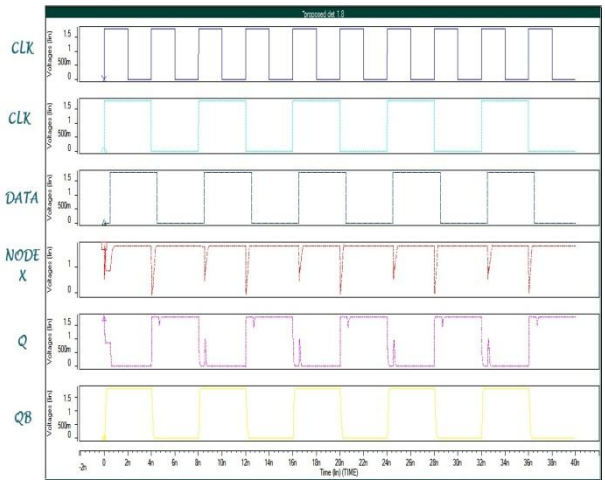

Figure 6: Simulation wave forms of proposed dual edge Triggered Flip Flop

Figure 4 shows the simulation wave forms of CDMFF design and figure 5 shows simulation wave forms of CPSFF design figure 6 shows the simulation wave forms of proposed dual edge triggered flip-flop.

To test elaborated the power consumption behavior of the flip-flop designs five test patterns each exhibits different data switching probability are applied. Five of them are deterministic patterns with 0% (all-zero or all-one), 25%, 50%, and 100% data transition probabilities, respectively. The power consumption results are summarized in Table 2.

While comparing three design models of flip-flops CPSFF, Proposed dual edge triggered flip-flop achieves the good performance. Using CPSFF approximately 24% of power consumption reduction is achieved; in proposed model approximately 40% power reduction is achieved when compared with CPSFF design.

6. CONCLUSION

In this paper, three varieties of design techniques for low power clocking system reviewed. CDMFF mapping methodology used to map inputs to eliminate redundant transitions. In CPSFF clock load is minimized. CPSFF achieves the 23% reduction in power consumption. In

proposed dual edge triggered flip-flop even the clock load increased the overall power dissipation is reduced. By reducing the power consumption in sequential elements the overall power consumption in circuits decreased drastically.

7. REFERENCES

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