Energy Efficient Design of Static Asymmetric Low Swing On-Chip Interconnect Circuits

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ABSTRACT
In this paper, an energy efficient design of asymmetric high performance low swing CMOS driver receiver pair for driving global on-chip interconnects is proposed. The design is implemented on 90nm CMOS technology using HSPICE. The proposed CMOS driver receiver pair reduces the power by 35.45% as compared to the static driver with conventional level converter (CLC). The design is also compared with the asymmetric source follower driver with level converter (ASDLC), which results in high performance and low power consumption with reduced circuit complexity.

General Terms
High performance, low power, circuit complexity, CMOS technology, driver, receiver, interconnect

Keywords
Low swing, CMOS driver receiver pair, level converter, asymmetric source follower driver, global on-chip interconnects.

1. INTRODUCTION
The power consumption of an integrated circuit mostly depends on the interconnecting wires and the associated driver and receiver circuits. Long global interconnect wires such as buses, clocking, and timing signals constitute the major source of delay and power consumption [1]. For gate array and cell based designs, the power consumed by the clock signals and wires can be up to 50% of the total on-chip power consumption. The impact of interconnect wires is even more significant for reconfigurable circuits. Measured over a wide range of applications, more than 90% of the power dissipation of traditional FPGA devices have been reported to be due to the interconnect [2]. Most effective technique to achieve power reduction and energy-delay efficiency is to reduce the voltage swing of the signal on the wire. But noise margin is a compromise for reducing the voltage swing.

In this paper, different low swing signaling schemes are presented and compared in terms of power, delay and power delay product. In section 2, the basic test bench architecture and various performance metrics is described. In section 3, the conventional low swing asymmetric signaling schemes are discussed and in section 4, the proposed design is illustrated.

2. TESTBENCH ARCHITECTURE AND PERFORMACE METRICS
For fair comparison of various interconnect schemes, a common test bed is required. Fig. 1 (a) shows the block diagram of our benchmark interconnect circuit. The driver converts a full-swing input signal into a low swing interconnect signal, which is reverted back to a full swing output by a receiver circuit. The interconnect line is of a length 10mm, modeled by a distributed RC interconnect model with an extra load capacitance.

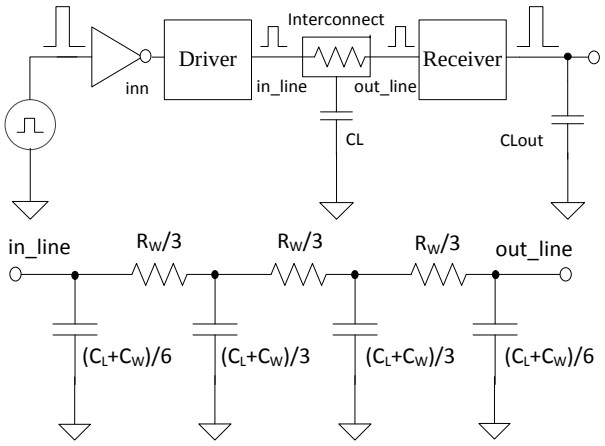

Fig. 1: (a) Benchmark Test Architecture (b) RC Interconnect Model

For all the circuits presented in this paper, we consider the following performance metrics.

2.1 Energy
The energy consumed by the driver, interconnect and receiver are separately analyzed and optimized individually for optimum energy consumption. The various low swing signaling schemes presented in this paper are compared with their energy consumption with respect to the variation in the length of the interconnect wire. The static drivers are preferred because they will result in lower switching activity [1]. The data switching activity is also a factor to be considered for comparing the schemes of different types. The supply voltage of the static driver should be as low as possible.

2.2 Reliability
Three main sources of reliability degradation have to be considered: process variation, crosstalk noise and power supply noise [2]. Static drivers are used to avoid floating interconnect, especially for long interconnect wires. To reduce the power supply noise, the receiver must have small input offset, high common mode noise rejection and good sensitivity.

2.3 Complexity
The number of extra power supplies used on-chip should be kept minimum. And only single ended signaling schemes will be considered so as to reduce the area overhead.

3. CONVENTIONAL DESIGNS

3.1 Static Driver with Conventional Level Converter

The circuit diagram of static driver with conventional level converter (SD-CLC) is shown in fig. 2 [1]. The static driver uses an extra power supply with lower voltage Vddl to drive the interconnect line from zero to Vddl. The receiver is a traditional level converter which is actually a differential amplifier, with an inverter to generate a complementary input signal. The circuits achieves a power saving on the interconnect line which is proportional to $Vddl^2$. This scheme works for low Vddl, as long as the value of Vddl is higher than threshold voltage Vt of the transistors. But Vddl should be large enough to have a reasonable noise margin. With Vddh=2V, the vddl value for minimum power-delay product is 1.1V, which reduces the power to 40% of that of full swing circuit. The area occupied on the chip is very small, since both the driver and receiver are very simple. The size of the PMOS devices of the driver should be large to compensate the loss of the current drive capability due to lower supply voltage. The complexity of the design is the extra power supply in both the driver and receiver circuits.

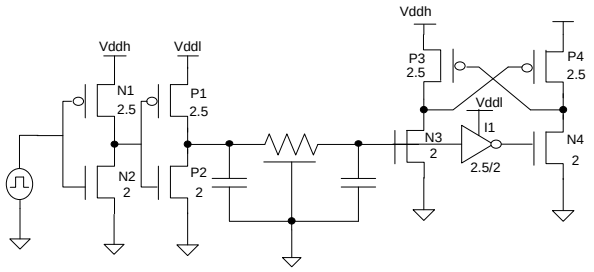

Fig. 2: Static driver with conventional level converter [1]

3.2 Asymmetric Source Follower with Voltage Sense Translator

The circuit diagram of asymmetric source follower driver with level converter (asf-lc) scheme is shown in fig. 3 [1]. The static driver uses an extra power supply of Vrefl to drive the interconnect line with a swing from Vrefl to Vdd-Vtn. The internal supply voltage Vrefl is set below Vtn of N5. The receiver is actually an asymmetric level Assume that the voltage at the end of wire goes from low to high: Vtn to Vdd-Vtn. Initially, node A and B sit at Vtn and ground, respectively. During the transition period both A and B nodes rise to Vdd-Vtn, and N5 is turned on and output goes low. The feedback transistor P1 pulls A further upto Vdd and that makes P2 to cutoff completely, and output is constant.

In the case of high to low transition, N5 turns off after A and B are discharged to a voltage which is less than Vt of transistor N5 and P2 pulls out up to Vdd.

The energy savings ratio of the interconnect is obtained as follows

$$\frac{E_{new}}{E_{full}} = \frac{V_{dd} - V_{tn} - V_{refl}}{V_{dd}}$$

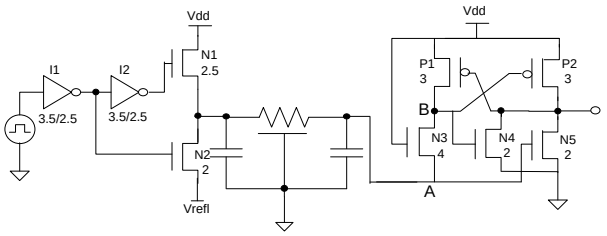

Fig. 3: Asymmetric Source Follower with Voltage Sense Translator [1]

3.3 High Offset Asymmetric Low Swing Voltage Scheme

The circuit diagram of high offset asymmetric low swing voltage scheme is as shown in the fig. 4 [5]. The input to the receiver comes from the driver circuit via the interconnect network. Input swings between the low and high limits of zero and Vdd-2Vtn. The pass transistor N3 isolates the internal node A, from the previous stage. Without the pass transistor, the lower potential from the previous stage causes the current to flow from Vddh through P1 back to the transmitter side. With node A isolated, the feedback transistor P2 can pull up the gate of P1 above the high swing voltage level at the input.

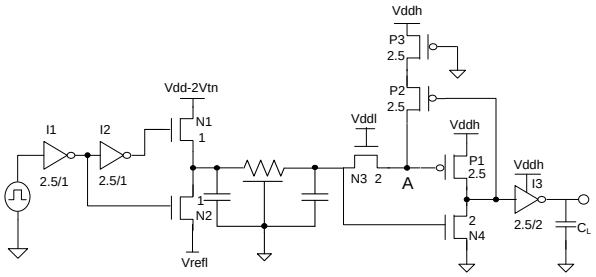

Fig. 4: High Offset Asymmetric Low Swing Voltage Scheme [5]

4. PROPOSED DESIGN

The circuit diagram of the proposed design is shown in fig. 5. The disadvantage of the high offset asymmetric low swing voltage scheme in fig. 4 is that it consumes significant static power due to the network formed by the transistors P1, N4 and inverter I3. But the elimination of these elements is not possible due to its operation failure. So, the feedback path is eliminated to reduce the power consumption and the output of the level converter is driven directly by the transistors P1 and inverter I3 towards high Vddh.

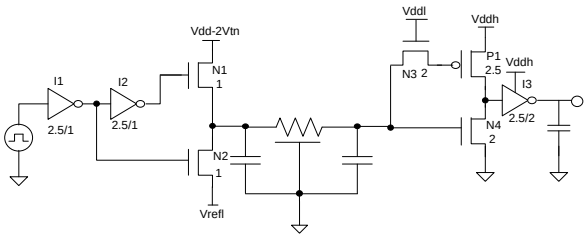

Fig. 5: Modified High Offset Asymmetric Low Swing Signaling Scheme

5. SIMULATION RESULTS

Fig. 6 shows the simulated waveforms of the proposed design. For the simulation of all the schemes discussed in the paper, we used the test bench architecture shown in fig. 1 (a). In all the schemes, Vdd is set to 1V and the load capacitance C_L is

kept 2fF. From the simulation results, power, delay and power delay product were computed and are shown in table I.

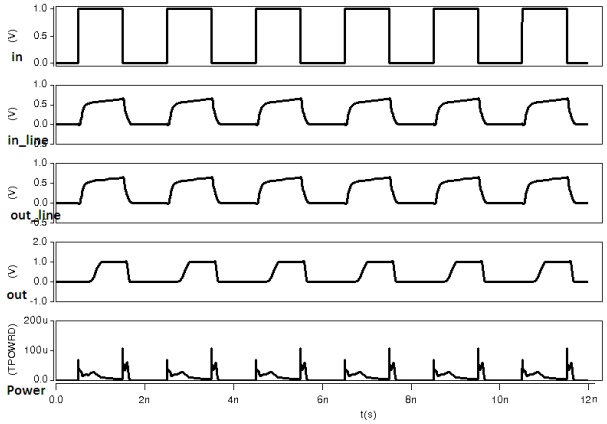

Fig. 6: Simulation Waveforms of the Proposed Design.

Table I
Comparison of various Schemes for 10mm length of interconnect

Schemes	Power (uW)	Delay (ns)	Power Delay Product (pJ)
SD-CLC [1]	17.77	0.31	5.508
ASF-VST [1]	28.6	0.42	12.012
HOA-LS [5]	13.51	0.385	5.201
Proposed	11.47	0.574	6.583

6. CONCLUSIONS

The existing low swing interconnect interface circuit schemes show a wide variety of problems in efficiency, performance and robustness. A novel modified circuit is proposed to address some of these problems. The proposed design has improved in its power consumption saving as compared to the conventional level converter and voltage sense translator. The proposed scheme reduced the power by 35.45% over the conventional level converter.

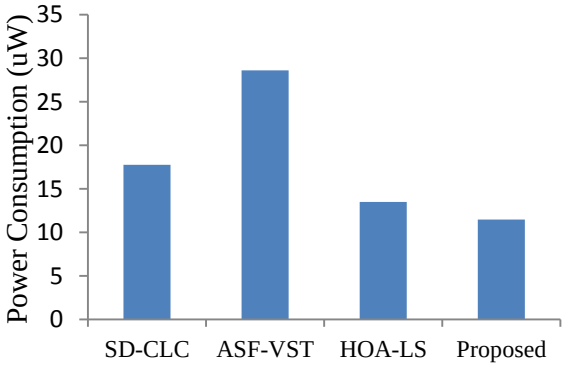

Fig. 7: Power Consumption of various schemes

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