Low Power Pulsed Flip-Flop using Self Driven Pass Transistor Logic

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ABSTRACT
In this paper, a low power implicit type pulsed flip-flop (PFF) using self-driven pass transistor logic is presented. The pulse generation logic comprising of two transistor AND gate is used in the critical path of the design for improved speed and reduced complexity. The pass transistor logic driven by generated clock pulse is used directly to drive the output of the flip-flop. The proposed design is compared with the conventional implicit type data close to output (ip-DCO) flip-flop. As compared to the conventional pulse triggered flip-flop, the proposed pulsed flip-flop (PFF) design features best speed, power and power-delay-product performance. The proposed technique is implemented using HSPICE CMOS 90nm technology. The average power consumption for 50% switching activity is reduced by 12.75% as compared to conventional ip-DCO.

Keywords
Low power, pulsed flip-flop, pass transistor logic, critical path, power-delay-product

1. INTRODUCTION
Flip-flops (FFs) are the fundamental building blocks of any sequential circuit design. In particular, digital designs nowadays often adopt pipelining techniques for high throughput, which increases the use of number of FFs. It is also estimated that in many integrated systems, the power consumption of the clock system, consisting of clock distribution networks and storage elements(FFs and latches), is about 50% of the total system power [1]. In clock system, power is mostly consumed by flip-flops. If the power consumed by the flip-flops is reducing then there will be a deep impact on the total power consumption of the clock system.

Pulse triggered flip-flop (PTFF) is considered as an alternative for the conventional transmission gate (TG) based or master-slave based edge triggered flip-flops [2][3]. A PTFF consists of a pulse generator and a latch. If the width of the triggered pulses is narrow then the latch acts like an edge triggered flip-flop. Since only one latch is used, the PTFF is simpler in complexity as compared to the conventional master-slave flip-flop. This leads to higher data rate for high speed operation.

Based on the method of pulse generation employed in the design, the PTFFs are of two types: implicit type and explicit type [4]. In an implicit type, the pulse generation is built-in logic of the latch structure. In an explicit type, the pulse generation and latch are separate. Implicit type pulse generation is considered as more power efficient than explicit type pulse generation. This is because; the former merely controls the discharging path while the later generates the pulse train.

In this paper, a novel low power implicit type PTFF design featuring self-driven pass transistor logic is presented. The proposed scheme includes implicit type pulse generation and the use of additional pass transistor controlled by the clock pulse to directly drive the output Q. This design gives rise to competitive power and PDP performance against conventional PTFF designs.

2. PROPOSED LOW POWER PULSED FLIP-FLOP

2.1 Conventional Pulse Triggered Flip-Flop Designs
The conventional implicit type pulse triggered flip-flops, which are used as the reference designs for performance comparisons, are reviewed first. As shown in Fig. 1[4], the implicit data closed to output (ip-DCO) type PTFF consists of an implicit pulse generator based on AND logic and a semi-structured latch design. Two practical problems arise in this design. First, during the positive edge of the clock, two nMOS transistors N2 and N3 are switched on. As long as the input data remains high, node X will be discharged on every positive edge of the clock. This leads to a large amount of switching power. The other problem is that node X controls two large MOS transistors (P2 and N5). The large capacitive load at node X causes speed and power performance degradation.

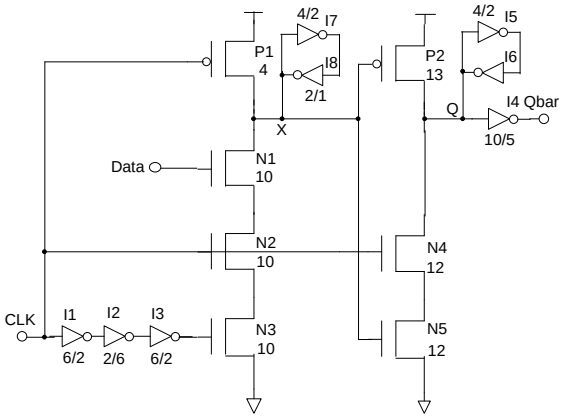

Fig 1: Conventional PTFF ip-DCO [4]

Fig. 2 shows a conditional pulse enhancement based PTFF (CPE-PTFF) [5], which adopts two measures to overcome the difficulties encountered with the existing PTFF designs. The

first one is reduction in the number of nMOS transistors stacked in the discharging path. The other one is a mechanism to support conditional enhancement of the pull down strength when input data is high.

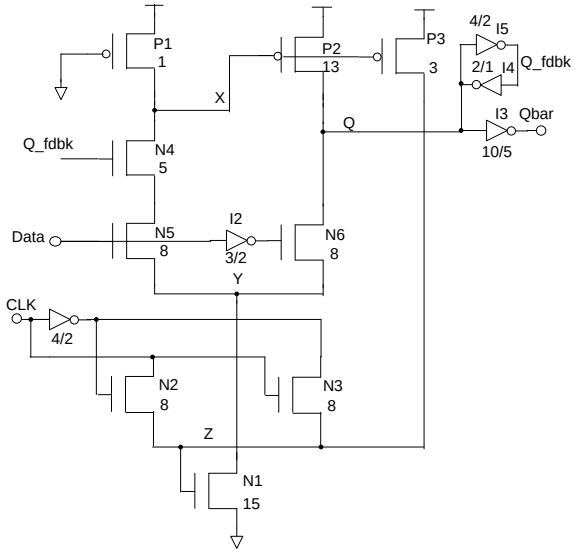

Fig 2: Conditional Pulse Enhancement Based PTFF (CPE-PTFF) [5]

2.2 Proposed Pulsed Flip-Flop Design

The proposed low power pulsed flip-flop using self driven pass transistor logic scheme is shown in Fig. 3. It consists of a latch structure and pulse generation logic. A weak pull-up pMOS transistor P1 with gate connected to ground is used in the first stage of true-single-phase-clocked latch (TSPC) [6]. This gives rise to a psuedo-nMOS logic style design. This approach reduces the load capacitance at node X. The transistors N2 and N3 forms the pass transistor logic (PTL) based two input AND gate which is used to generate pulse train. A pass transistor N6 controlled by the pulse clock is included so that the input data can drive the output node Q of the TSPC latch directly (self-driven). With this, the level of node Q can be quickly pulled up to reduce the data transition delay. This newly employed pass transistor provides a discharging path. The function of this pass transistor is twofold, i.e., driving to node Q during 0 to 1 transition and discharging node Q during 1 to 0 transitions.

The principle of operation of proposed FF design is explained as follows. If no data transition occurs and when clock pulse arrives, i.e., the input and output nodes are at the same level, no current passes through the pass transistor N6. At the same time, assuming input data and Q_fdbk are at complementary levels, the pull-down path of node X is off.

If data transition from 0 to 1 occurs, node X is discharged to turn on transistor P2, which pulls the node Q high. With the pass transistor logic N6, the delay can be greatly reduced. When data transition from 1 to 0 occurs, transistor is turned on by the clock pulse and node Q is discharged through the pass transistor N6. Now the pass transistor N6 is turned only for a short duration. In addition, a keeper logic is placed at node Q to lift the state of the discharging path once the Q_fdbk is inverted.

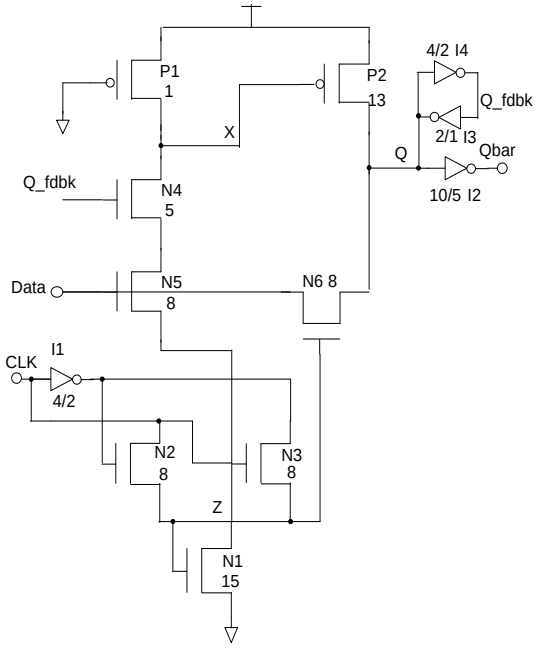

Fig 3: Proposed Low Power Pulsed Flip-Flop

3. PERFORMANCE ANALYSIS

For testing the performance of the proposed design and for fair comparison with the existing PTFFs, the 'reset' function has been incorporated. Because of the architectural complexity, the methods explained earlier cannot be used for 'reset' in conventional PTFFs. Now, we use a NOR based reset circuit shown in fig. 4 for reset logic in the conventional pulse enhancement based PTFF and proposed pulsed flip-flop design. And also the performance of both the flip-flop designs was compared.

The NOR logic based reset circuit acts as cross coupled inverter pair and is replaced with the keeper logic (inverter loop I4 and I5 in fig. 2 and inverter loop I3 and I4 in fig. 3) in the circuit. In the NOR based reset circuit, when rst_n is high, and on a negative edge of rst_n, N1, pulls IN low to achieve the required reset operation. The size of the transistor N1 in the reset circuit is kept large to avoid any power consumption.

In order to improve the performance of the proposed design, a 4-bit ring counter has been designed and tested. The 4-bit ring counter design is shown in fig. 5.

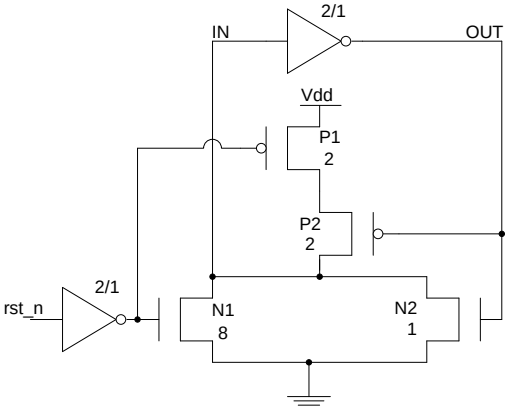

Fig 4: NOR logic based reset circuit

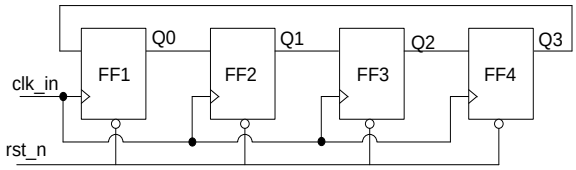

Fig 5: 4– bit Ring Counter

4. SIMULATION RESULTS

The proposed pulsed flip-flop design is compared with the conventional pulse triggered flip-flops to obtain their performance metrics. These designs include the two implicit type PTFF designs shown in Fig. 1 (ip-DCO [4]), Fig. 2 (CPE-PTFF [5]). The proposed flip-flop is implemented in 90nm CMOS technology at room temperature using HiSIM level 68 model HSPICE. The operating condition used in simulations is 500MHz/1.0V.

Fig. 6 shows the simulation testbench model. Considering the loading effect of the flip-flop to the previous stage and the clock tree, the power consumption of the clock and data buffers are also included. The output of the flip-flop is loaded with a 20 fF capacitor. An extra capacitance of 3 fF is also placed after the clock buffer. To illustrate the performance of the present work, Fig. 7 shows the simulation waveforms of the proposed low leakage PTFF against conventional PTFFs. The power consumption results are summarized in Table I. Table I also summarizes some important performance metrics of the PFF designs. These include transistor count, set-up time, hold time, Data-to_Q delay, average power consumption and power delay product (PDP).

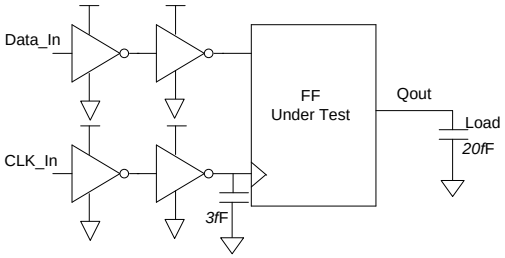

Fig 6: Simulation Test bench Model

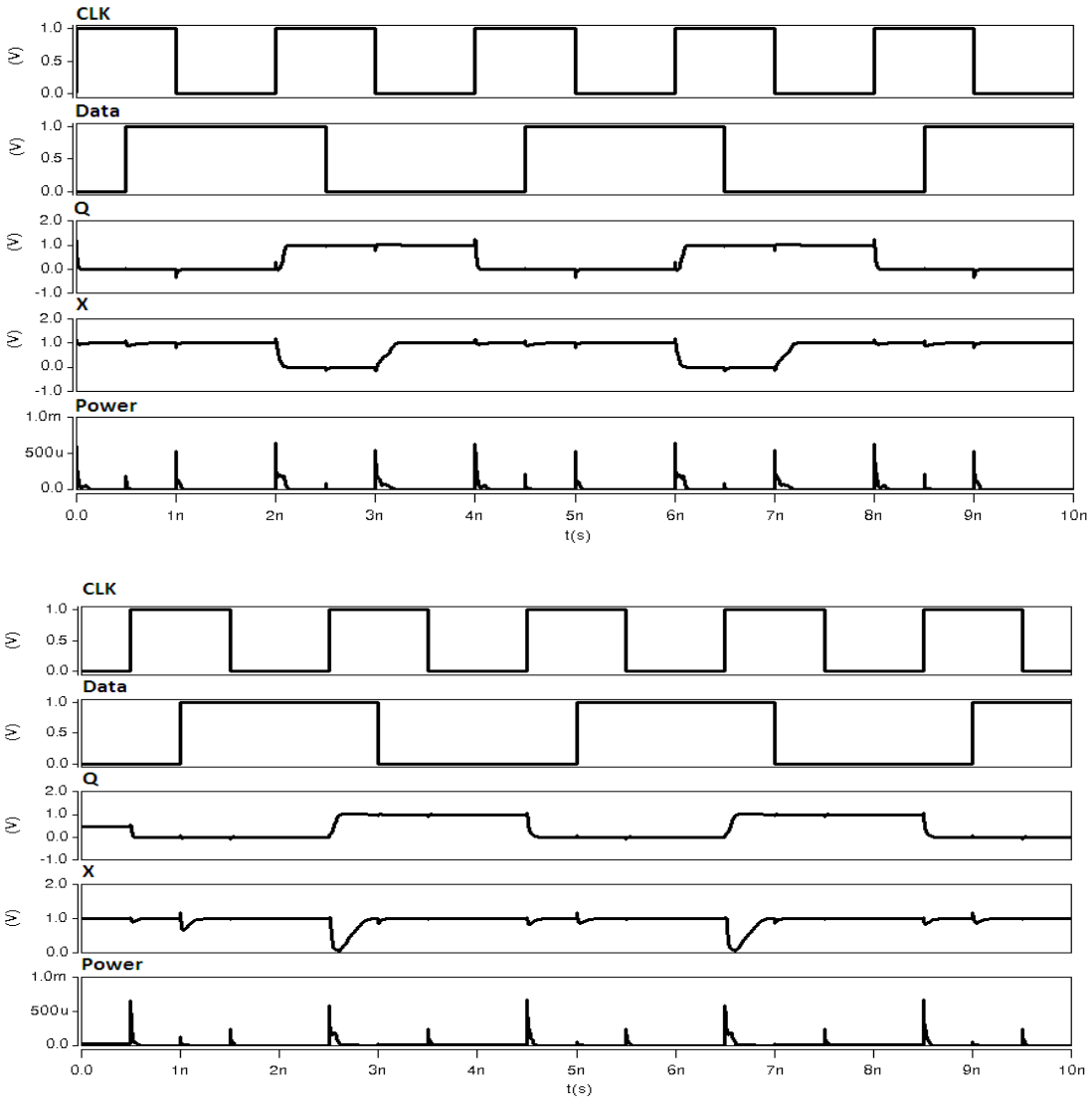

Fig 7: Simulation Waveforms of (a) ip-DCO (b) Proposed PFF Design

To get a more realistic performance, the overall power consumption for different input patterns is simulated. Consider five different data sequences to represent various input switching activities. The sequence of …010101… represents 100% switching activity, …00110011… represents 50% switching activity, and …00010001… represent 25% switching activity. Two other sequences, …11111… and …00000… are used to represent the switching activity of 0%. We compare the power consumption and power-delay-product for 50% switching activity with conventional pulse triggered flip-flop designs.

Fig. 7 shows the simulation waveforms for conventional ip-DCO flip-flop and proposed pulsed flip-flop. The waveforms represent the comparison of signals clock pulse (CLK), input data (Data), Output (Q), internal node (X) and power in microwatt. Fig. 8 shows the power consumption for different data switching activities of various flip-flops.

Table 1. Comparison of Various PTFF Designs

PTFF	ip-DCO	CPE-PTFF	Proposed PFF
Transistors	23	19	16
Setup Time(ns)	-50.01	-50.02	-2.6
Hold Time(ns)	1.5	1.5	1.6
Min. Data to Q Delay (ns)	1.12	0.963	0.52
Average Power (uW) 100% Activity	18.62	15.02	13.22
Average Power (uW) 50% Activity	13.48	13.0	11.76
Average Power (uW) 25% Activity	6.97	7.15	6.65
Average Power (uW) 0% Activity All One	7.68	6.97	6.36
Average Power (uW) 0% Activity All Zero	6.75	5.03	4.95
Power Delay Product (PDP) (fJ)	15.09	12.52	6.03

5. CONCLUSIONS

In this paper, a novel low power pulsed flip-flop using self-driven pas transistor logic scheme is proposed. The proposed design reduces the transistor count thereby the layout area can be considerably reduced. Simulation results indicate that the proposed design excels conventional designs in its performance metrics such as power, D to Q delay and power delay product. The power consumption for different data switching activities is compared and plotted. The average power consumption is reduced by 12.75% for 50% data switching activity. The proposed flip-flop gives a very good power-delay-product (PDP) with glitch free operation and is useful in high performance applications.

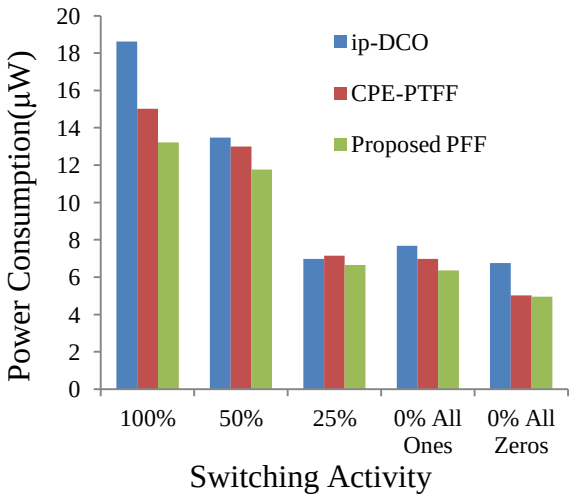

Fig. 8: Power Consumption Under Different Data Switching Activities

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