

# Design and Simulation of Output Queuing with the Middle stage Buffered (OQMB) Clos Packet Switching Network

S. Rajeshwari  
M.E (Applied Electronics)  
University college of Engineering Nagercoil  
Kanyakumari, Tamilnadu, India

R. Bharathi, Assistant professor  
University college of Engineering Nagercoil  
Kanyakumari, Tamilnadu, India

## ABSTRACT

Clos network, a family of multistage networks, are attractive alternative for constructing scalable packet switches because of its distributed and modular design. The Clos packet switching networks are the next step in scaling current crossbar switches to large number of ports. This paper presents the design and simulation of buffer less- buffered- buffered - Clos Packet switching network architecture. This paper proposes a novel the output queuing with the middle stage buffered (OQMB) Clos Packet switching architecture that does not need any schedulers. This architecture employs an ID matching with OQMB packet switching and desynchronize static round robin (DSRR) scheme to achieve Maximum throughput under any admissible traffic. Our queuing analysis demonstrates that only small size buffers are needed in the central stage. The only trade off for the proposed (OQMB) architecture is to employ small extra resequencing buffers. Input modules with desynchronize static round robin (DSRR) scheme connection scheme guarantees no cell contention in input stages. As a result, the OQMB architecture can achieve very high performance, and high throughput under any admissible traffic.

## General words

Output Queuing with the Middle stage Buffered (OQMB), Desynchronize Static Round Robin (DSRR), Input and Output Queuing (IOQ)

## Keywords

Input and Output Queuing with the Middle stage Buffered (IOQMB), Fully Buffered (FB), Very Large Scale Integration (VLSI).

## 1. INTRODUCTION

Clos network is a kind of multistage on chip permutation network. The Clos network architecture [1] was first proposed by C. Clos in the 1950s, for use in telecommunications networks. Clos networks are required, when the physical circuit switching needs exceed the capacity of the largest feasible single crossbar switch. We proposed to design and simulation of a Clos packet switching network to support collision free and guaranteed throughput. The combinatorial properties of this multi-stage interconnected network help to construct strict non-blocking circuit switches with fewer cross-points. Clos networks have three stages: the ingress stage, middle stage, and the egress stage. Each stage is made

up of a number of crossbar switches; often just called crossbars. This network has a rearrangeable property [11] that can realize all possible permutations between its input and outputs. The choice of the three stage Clos network with a modest number of middle stage switches is to minimize implementation cost, whereas it still enables a rearrangeable property for the network. The proposed Clos network employs an ID matching with OQMB packet switching and desynchronize static round robin (DSRR) scheme. The ID matching scheme offers a contention free routing from unauthorized users. It compares the user ID with the switch port ID, depending upon ID matching it will allow the segmented packets to further stages. The output queuing with the central stage buffered (OQMB) Clos packet switching network contains buffer less input stage with the buffered central stage and buffered output stage. A desynchronized static round-robin (DSRR) connection pattern is set in buffer less input stage switching modules and guarantees zero cell contention. This paper is organized as follows; section 2, explains related work of Clos packet switching network design. Section 3, explains a brief introduction of Clos packet switching network design is presented. Section 4 gives the simulation Results. In section 5, gives the conclusion.

## 2. RELATED WORK

Reviewing on chip permutation networks (supporting either full or partial permutation) with regard to their implementation shows that most of the networks employ a packet switching mechanism to deal with the conflict of permuted data [3]–[6]. Their implementations either use first input first output (FIFO) queues for the conflicting data [3] [5] [6] or time slot allocation in the overall system with the cost of more routing stages [5] or a complex routing with a deflection technique that avoids buffering of the conflicting data [4]. The choices of network design factors, i.e., topology, switching technique and the routing algorithm, have different impacts on the on chip implementation. Regarding the routing algorithm, the deflection routing [4] is not energy efficient due to the extra hops needed for deflected data transfer, compared to a minimal routing [2] [3] [5]. Moreover, the deflection makes packet latency less predictable; hence, it is hard to guarantee the latency and the in order delivery of data. Clos-network packet switch can be classified based on their buffer (memory) allocation schemes. For example, the simplest Clos-network fabric has no buffers at any stage.

Since the Switching is done purely in space for all three stages, this Architecture is normally named as buffer less architecture. Input and output queuing with the middle stage

buffered (IOQMB) architecture has buffered input and output stages and a buffer less central stage. Although there are other possible buffer allocation schemes a fully buffered architecture, most existing researches on Clos-network packet switch are on these two architectures. Their focus is to develop good scheduling algorithms for the architectures. In fact, the way of allocating the buffers is an important design consideration and it influences the switching performance. Buffer less architecture is favoured for hardware simplicity. However pure space switching in all three stages increases the cell contention probability. The throughput of buffer less with random dispatching may be as low as 39.7%. Input and output queuing with the buffer less central stage (IOQ) architecture tries to enhance the performance of buffer less by adding buffers to input and output stages. The buffers relieve the cell

contentions in these two stages, but IOQ tends to keep a buffer less central stage in fear of out-of-sequence problem. This leaves some unsolved contentions. The throughput of IOQ with random dispatching is increased but not satisfactory. The worst case throughput is 63% and is still not a satisfied result. Obviously, Fully Buffered (FB) architecture does not suffer any throughput degradation since all possible contentions are absorbed by buffers, but it is expensive to be implemented. It is worth asking whether there exists less complex architecture which performs as well as Fully Buffered (FB). Observing that the main effect of buffers is to resolve contentions, buffers can be removed if there is no contention at all. The proposed Clos network employs an ID matching with IOQMB packet switching and desynchronize static round robin (DSRR) scheme.

**Table 1 Comparison with other related on-chip permutation networks**

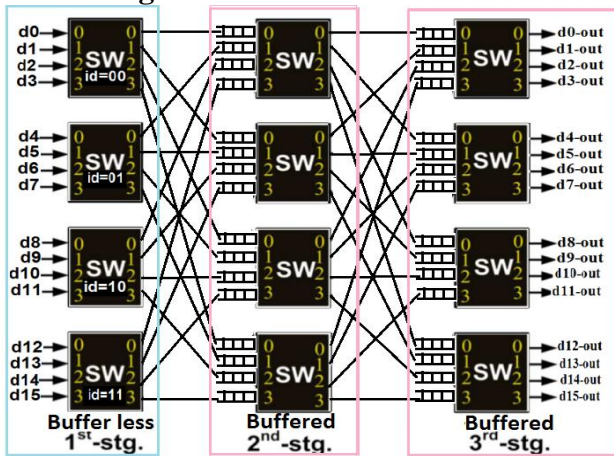
Design	Permutation and Switching	Number of inputs and outputs	Topology	Collision occurrence
[3]	Concurrent permutation & Packet switching	16×16	Mesh and torus	Data loss & in order delivery is difficult.
[4]	Concurrent permutation & Packet switching	16×16	De-Bruijn	Data loss & in order delivery is difficult.
[5]	Concurrent permutation & Packet switching	16×8	Butterfly & Benes 2N-N	Data loss & in order delivery is difficult.
[6]	Transpose permutation & Packet switching	16×16	Mesh and torus	Data loss & in order delivery is difficult.
[7]	Arbitrary permutation & Packet switching	16×16	Mesh and torus	Throughput degradation.
[8]	Application aware routing	16×16	Mesh and torus	Throughput degradation.
[15]	On chip permutation	16×16	3stage Clos	Collision occurs.
Proposed work	On chip permutation & Packet switching	16×16	3stage Clos	Collision free and highly efficient throughput under any admissible traffic.

### 3. CLOS PACKET SWITCHING NETWORK DESIGN

Clos network, a family of multistage networks, is applied to build scalable commercial multiprocessors with thousands of nodes in macro systems [7] [11]. A typical three stage Clos network is defined as  $C(n, m, p)$ , where  $n$  represents the number of inputs in each of  $p$  stage switches and  $m$  is the number of second stage switches. The proposed Clos network

employs an ID matching with IOQMB packet switching and desynchronize static round robin (DSRR) scheme.

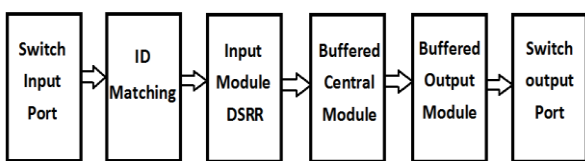
### 3.1 Clos packet switching network buffer less-buffered- buffered topology with port ID matching



**Fig 3.1: Clos packet switching network**

This paper proposed to use C (4, 4, 4) as a topology for the designed network (Fig.3.1). This network has a rearrangeable property [11] that can realize all possible permutations between its input and outputs. Fig 1 says that there are sixteen input ports are available in our clos network. These ports are connected to the corresponding switches depending upon the ID of the switches. The first switch is having the ID as 00, second switch is having the ID as 01, Third switch is having the ID as 10 and fourth switch is having the ID as 11. The proposed clos network employs an ID matching with OQMB packet switching and desynchronize static round robin (DSRR) scheme. A desynchronized static round-robin (DSRR) connection pattern is set in buffer less input stage switching modules and guarantees zero cell contention. OQMB architecture is proved to be of 100% throughput under any admissible traffic. It needs no scheduler and is practical to be implemented. In response to the out-of-sequence problem, queuing analysis is conducted for output queues of the central stage.

### 3.2 Proposed Block Diagram



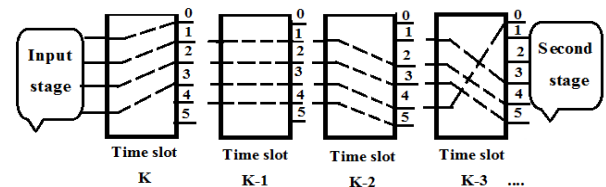
**Fig 3.2: Block Diagram**

Fig3.2. Shows that the ID matching section matches switch ID with the port ID and connect it to the output port. If it is not matching means it would not allow that so it makes the collision free one from un authorized users. Due to the clos network topology all possible combinations are available between inputs to output. The output queuing with the middle stage buffered OQMB packet switching architecture consists of a buffer less input stage, buffered middle and output stages. In packet switching, messages are broken into certain blocks called packets, and packets are transmitted independently using the store and forward scheme. The packets are passed to the first stage. Each packet contains the packet number, Source address and destination address. The buffer less input

stage forwards the packet to the second depending on the destination address using DSRR connection pattern. The buffered central stage Stores the packet and forwards it by FIFO Principle to the destination by using destination address. The buffered output stage Stores the packet and forwards it by FIFO Principle to the destination port. After receiving packet third stage sends the Ack signal to the source If it sends the Negative Ack means again the source will resend the packet.

### 3.3 Desynchronized static round-robin (DSRR) connection pattern

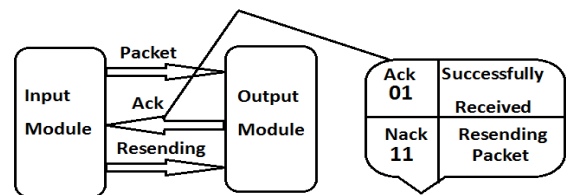
DSRR is run distributed and independently by each Input stage. Any input sequentially connects to all outputs in a round-robin manner; at each time slot, inputs map injectively to outputs. This can be achieved by setting a fully desynchronized initial Connection pattern input stage with DSRR connection scheme guarantees no cell contention in input stages when the fabric is non-blocking (i.e.,  $m \geq n$ ). This is because at each time slot, there is at most one cell arrives at the Input stage, and it is immediately transferred to an output stage according to the connection pattern. Cells arriving at the input stages are dispatched to different Central stages within a time slot.



**Fig 3.3: Desynchronized static round-robin (DSRR)**

### 3.4 Packet transmission

The buffer less input stage forwards the packet to the second depending on the destination address. The buffered central stage Stores the packet and forwards it by FIFO Principle to the destination by using destination address. The buffered output stage Stores the packet and forwards it by FIFO Principle to the destination port. After receiving packet third stage sends the Ack (01) signal to the source. If it sends the Negative Ack (11) means again the source will resend the packet.



**Fig 3.4: Packet transmission**

Because of packet switching, Successive packets in a message can be transmitted simultaneously on different links, reducing the end-to-end transmission delay. (This effect is called pipelining.) Due to the smaller size of packets compared to messages, packets are less likely to be rejected at the intermediate nodes due to storage capacity limitation at the switches. Both the probability of error and the error recovery time will be lower for packets since they are smaller. Once an error occurs, only the packet with the error needs to be retransmitted rather than the whole message. This leads to a more efficient use of the transmission bandwidth Messages are fragmented into packets that cannot exceed a maximum size. This leads to fairness in the network utilization, even when messages are long.

## 4. SIMULATION RESULTS

### 4.1 First stage switch with ID matching

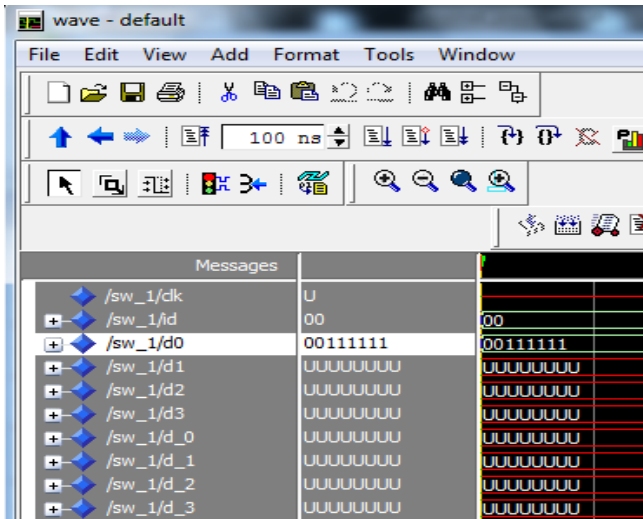


Fig 4.1: First stage switch with ID matching

The Fig 4.1 shows that the clock signals as high and switch1 id as 00. This matches with switch id so allows it. Then the first port of SW\_1/d0 sends the packet to third output port SW\_1/d3 out by sending 00111111. In this first 4 bit represents output address and next four bit represents packet data.

### 4.2 Router stage switch output

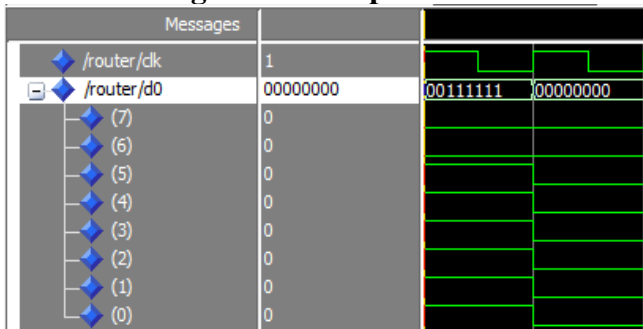


Fig 4.2.1: Packet transmission

Fig 4.2.1 shows that first port of SW\_1/d0 sends the packet data 1111 to the third output port SW\_1/d3 out by sending the destination address and data 00111111. In this first 4 bit represents destination address and next four bit represents packet data. This is the expanded view of each bit.

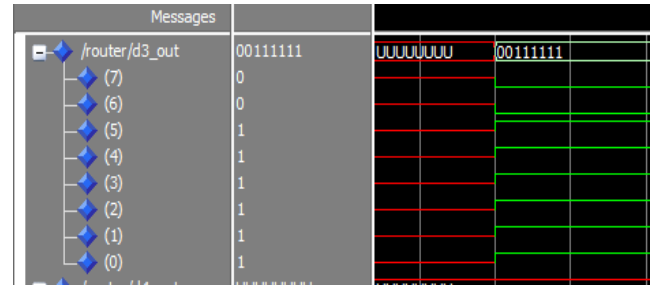


Fig 4.2.2: Packet Reception

Fig 4.2.2 shows the SW\_1/d3 out receives the packet 1111 Successfully

### 4.3 First stage data flow diagram

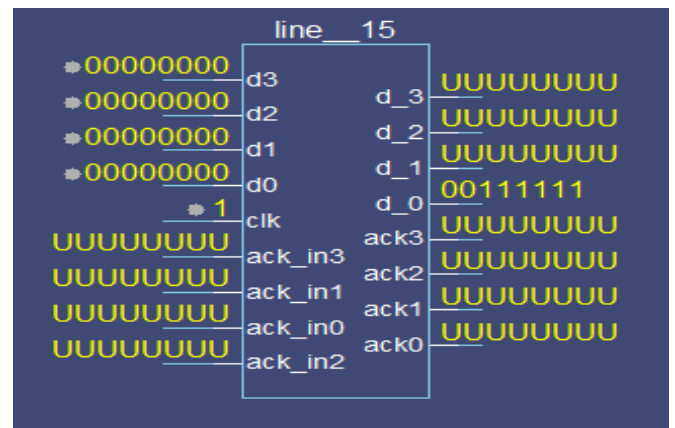


Fig 4.3: First stage data flow

Fig 4.3 shows the dataflow of First stage. Here the clock signal as high and first port of SW\_1/d0 sends the packet to third output port SW\_1/d3 out by sending 00111111. In this first 4 bit represents output address and next four bit represents packet data.

### 4.4 Router stage data flow diagram

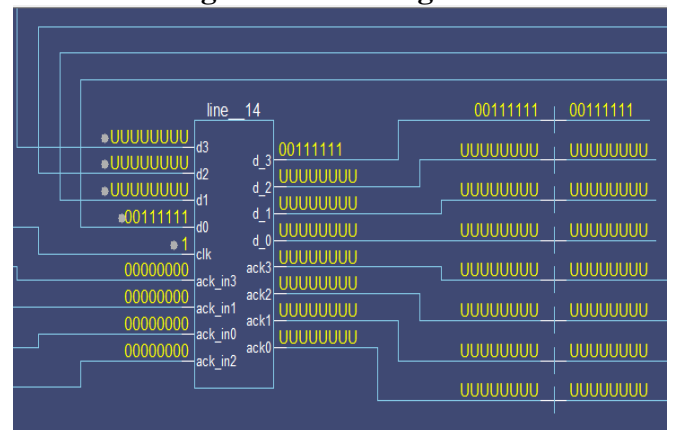


Fig 4.4: Router stage data flow

Fig 4.4 shows the dataflow of router stage. Here the clock signal as high and first port of SW\_1/d0 sends the packet to third output port SW\_1/d3 out by sending 00111111. In this first 4 bit represents output address and next four bit represents packet data. The final stage SW\_1/d3 out receives the packet 1111 Successfully.

### 4.5 Router stage wave output

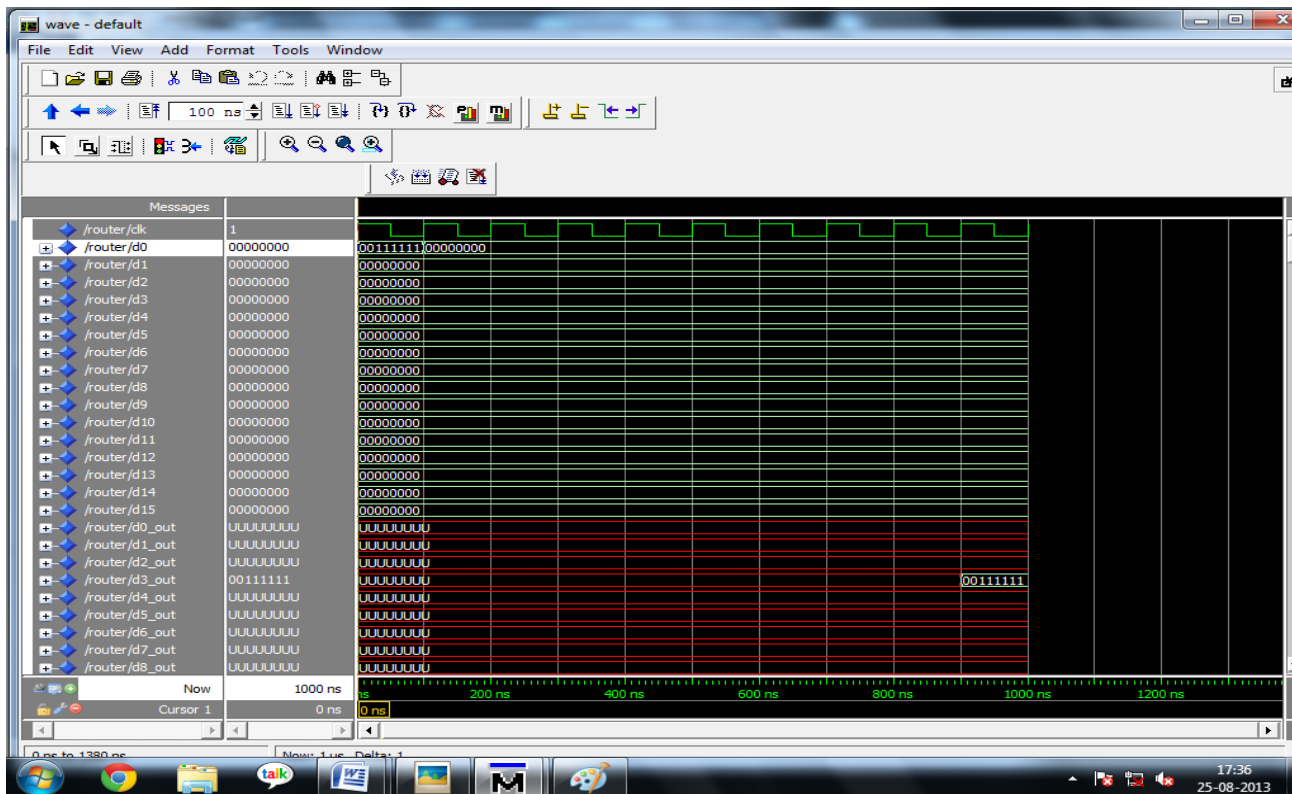


Fig 4.5: Router stage wave output

Fig 4.5 shows the router stage wave output here the first port of SW\_1/d0 sends the packet data 1111 to the third output port SW\_1/d3 out by sending the destination address and data

00111111. In this first 4 bit represents destination address and next four bit represents packet data. The final stage SW\_1/d3 out receives the packet 1111 Successfully

### 4.6 Router stage list output

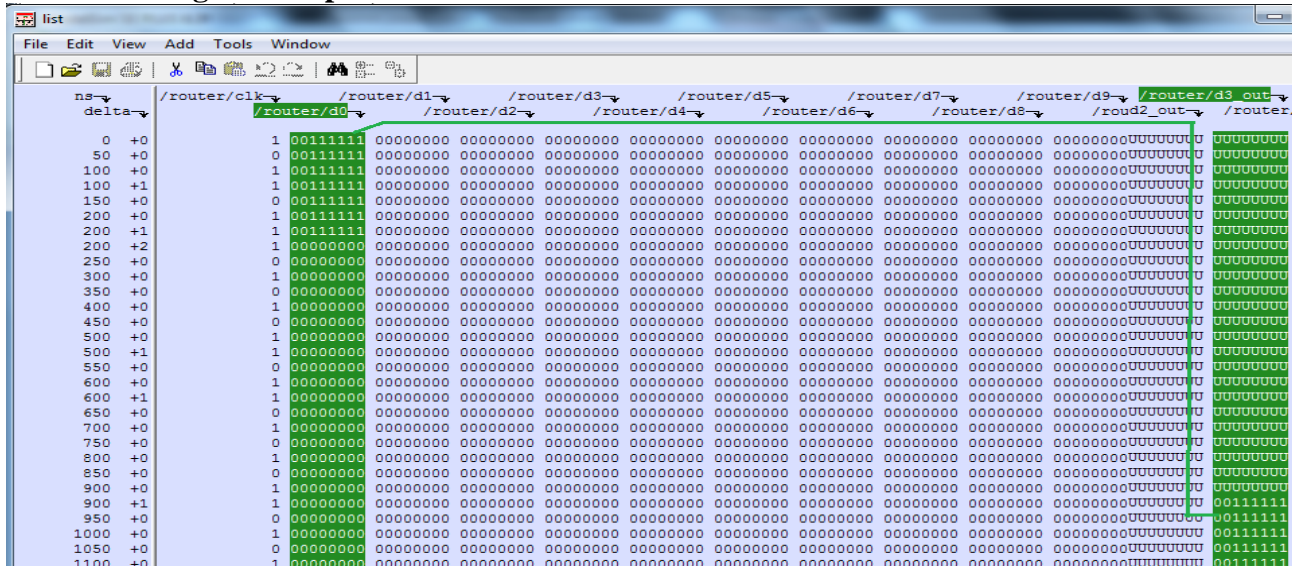
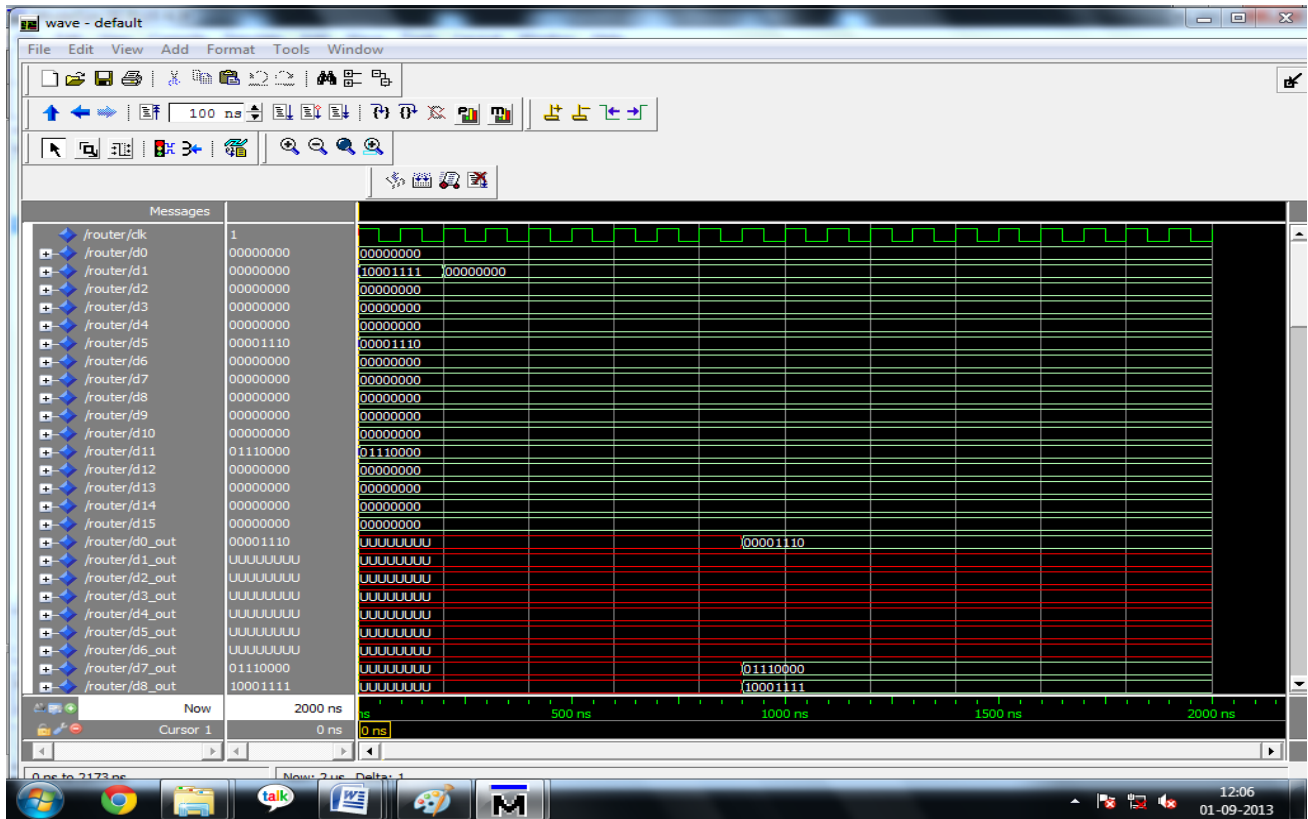


Fig 4.6: Router stage list output

Fig 4.5 shows the router stage list output here the final stage SW\_1/d3 out receives the packet 1111 Successfully from source .



#### 4.9 Router stage simultaneous packet transmission



**Fig 4.9: Router stage packet transmission**

Fig 4.8 shows the Router stage simultaneous packet transmission here router /d0 sends the packet 1111 to d8\_out, router/d5 sends the packet 1110 to d0\_out and router /d11 sends the packet 0000 to d7\_out. With the help of buffering all these packets are successfully received with contention free and improves efficiency.

#### 5. CONCLUSION

In this Paper, We have presented the output queuing with the middle stage buffered (OQMB) Clos Packet switching network architecture. This OQMB Clos Packet switching architecture is designed using buffer less input stage – buffered central stage – buffered output stage - Clos Packet switching network. This network architecture is designed using VHDL .After designing this architecture using VHDL codings are simulated using ModelSim 6.3. This architecture employs an ID matching with OQMB packet switching and desynchronize static round robin (DSRR) scheme to achieve

maximum throughput under any admissible traffic. By using the ID matching scheme the circuit is protected from unauthorized users. Because of packet switching, Successive packets in a message can be transmitted simultaneously on different links, reducing the end-to-end transmission delay. Due to the smaller size of packets compared to messages, packets are less likely to be rejected at the intermediate nodes due to storage capacity limitation at the switches. Both the probability of error and the error recovery time will be lower for packets since they are smaller. With the help of buffering all these packets are successfully received with contention free and improves efficiency. Our queuing analysis demonstrates that only small size buffers are needed in the central stage. Input modules with desynchronize static round robin (DSRR) scheme connection scheme guarantees no cell contention in input stages. As a result, the OQCB architecture can achieve very high performance, and high throughput under any admissible traffic.

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## 7. AUTHOR'S PROFILE

S.Rajeshwari was born in tamilnadu, India in 1989. She received her B.E degree from PET Engineering College, Vallioor, and Tamilnadu in 2010 and she is doing her M.E degree in University College of Engineering, Nagercoil.

R. Bharathi was born in tamilnadu; India in 1977. She received her B.E degree from NoorulIslam college of Engineering, Kanyakumari, Tamilnadu in 1998. And she received her M.E degree from Arulmigu Kalasalingam College of engineering, Tamilnadu in 2006 .She is working as an Assistant Professor in Department of ECE, University College of Engineering, Nagercoil.